Control Design of a PFC with Harmonic Mitigation Function for Small Hybrid AC/DC Buildings

Rafael Peña-Alzola, *Member, IEEE,* Marco Andrés Bianchi, *Student Member, IEEE,* and Martin Ordonez, *Member, IEEE*

***Abstract*—Unprecedented expansion of native DC powered equipment (LEDs, computers and consumer electronics) has increased commercial and residential DC electricity usage over the past decade. Thus, it is foreseeable that hybrid AC/DC buildings featuring both AC and DC infrastructures will coexist. A hybrid AC/DC building will involve an efficient centralized rectifier that supplies all the DC loads, while legacy AC loads will remain connected to the existing AC infrastructure. This paper explores the opportunity of harmonic mitigation at distribution level in small hybrid AC/DC building by using a centralized power factor corrector (PFC) with large bandwidth. The current reference generator for the harmonic mitigation function (HMF) is explained along with power considerations. The PFC uses a proportional resonant (PR) controller, instead of a PI controller, without requiring additional sensors in the rectifier. A computationally inexpensive implementation of the PLL is also proposed along with considerations on parameter selection. The proposals provide all the steps for the straightforward control design of the PFC+HMF with fast calculations. The HMF requires only software modifications in the PFC and one sensor to measure the non-linear load. Simulation and experiments validate the proposed procedures.**

***Index Terms*—Power factor correctors, proportional resonant controller, semibridgeless PFC, boost PFC, harmonics**

I. Introduction

THE increase in DC electricity usage is putting even more pressure on a century-old AC power infrastructure. In the present AC building as the one depicted in Fig. 1, DC loads such as LED lighting, compact fluorescent lamps, electric vehicles (EVs), and computers require individual AC/DC rectifiers that result in increased cost and lower efficiency. As more and more loads are native DC loads, a transition to DC buildings and houses is expected [1], [2]. In DC buildings and houses, an efficient centralized rectifier supplies all the DC loads. The advantages of replacing the unnecessary individual rectifiers with a centralized rectification include: higher efficiency, lower costs, higher reliability, smaller footprint, and better power quality.

It is foreseeable a long period of hybrid AC/DC buildings in which the AC and DC infrastructures coexist and complement each other [1]. This situation is depicted in Fig. 2, where the DC loads are connected directly to the new DC infrastructure and legacy AC loads are connected to the already existing infrastructure. As legacy AC loads normally comply with electrical regulations, the distribution system harmonics have reduced but further improvements can be achieved for congested areas. As well, power quality is deteriorating quickly with the increasing penetration of non-linear loads [3]. The increasing utilization of non-linear loads in today's homes is a growing concern for utility companies due to the degrading power quality [4]. To maintain good power quality, more strict regulations on the non-linear loads and development of

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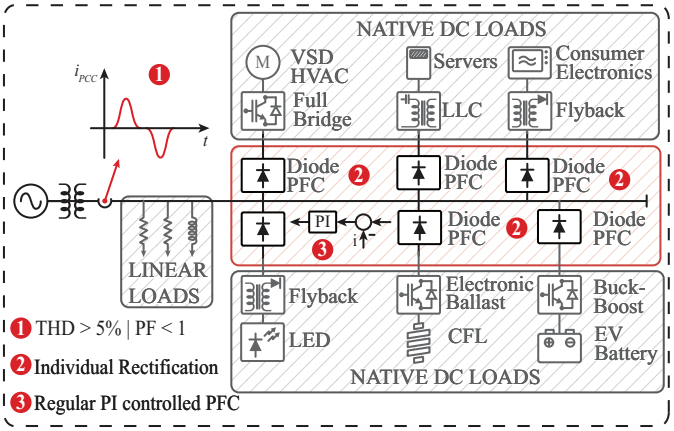

Fig. 1. Typical issues in traditional AC building including many native DC loads: low power quality (1) due to the presence of non-linear loads; lower total rectification efficiency due to individual rectification (2); PFC rectifiers mainly based on PI controller (3) that have limited sinusoidal tracking capabilities.

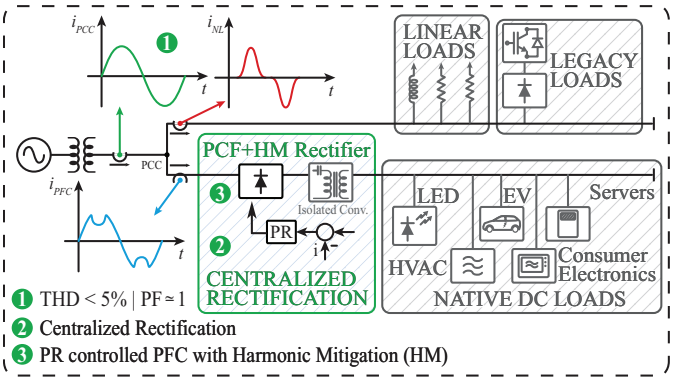

Fig. 2. Advantages of hybrid AC/DC building including the proposed PFC with harmonic mitigation function (HMF): 1) power quality of the building is increased through the HMF; 2) the centralized rectification scheme has the advantage of increasing the total conversion efficiency and reducing the overall cost; 3) the Proportional Resonant (PR) controller can track sinusoidal signals accurately.

means to compensate the distribution system harmonics are needed [3]. Unlike the industrial loads in a medium voltage network, the non-linear loads in the low-voltage distribution are highly distributed [3]. Lump harmonic compensation using passive filters or centralized active power filters at a few locations is difficult [5] and distributed compensation could be a better solution [6], [7]. Power converters of renewable energy systems (wind and solar) can be used for harmonic compensation [3], [4], using the available volt-ampere when not operating at full capacity. However, this solution is only possible where the renewable resource is available.

In North America, center-tapped transformers convert one distribution phase to a split-phase 120/240 V in small buildings (residential and light commercial) [8], [9]. The centralized rectifier in Fig. 2 comprises a single-phase PFCs followed by an isolated DC/DC converter. Single-phase PFCs rectify the input AC voltage with sinusoidal AC currents and unity power factor. The most well-known topologies for single phase PFCs are boost, bridgeless and semi-bridgeless [10], [11]. An elevated switching frequency (tens to hundreds kHz) enables filter size to be reduced and power density to be increased [12], [13], while improving the dynamic response of the converter. The isolated DC/DC stage (e.g. LLC resonant converter or phase shifted ZVS topology) [11] blocks the common mode voltage and provides the final DC output voltage. Despite the potential of single-phase PFCs to improve power quality, there are only a few references exploring the possibility of the single-phase PFC dealing with harmonics [14]–[16]. This is because the Harmonic Mitigation Function (HMF) requires active power transfer to the DC load as will be discussed in this paper. In [14], a technique was used for telecom parallel rectifiers combining PFCs with diode bridges. The PFCs compensate the harmonics generated by the diode bridges while supplying the load.

Considering the progressive and general transition to hybrid AC/DC buildings and the large bandwidth available in the centralized PFC, this paper explores the opportunity for harmonic mitigation in the distribution system. This useful function, conceptually depicted in Fig. 2, was not considered in any of the previous works on PFC described above. The paper presents the control design for a PFC with harmonic mitigation function (PFC+HMF). The proposed control design is based on three main subsystems: current reference generator for the HMF, PR controller for the current reference tracking, and efficient PLL implementation.

The proposed current reference generator for the HMF obtains information from measuring the non-linear current and determines the PFC current reference needed for mitigating the harmonics in the system. The operation is explained along with its limitations and power considerations.

The control loop for the proposed PFC+HMF uses a proportional resonant (PR) controller, which is discussed in detail, to effectively track the proposed HMF. PFCs usually employ PI controllers [17] that produce a phase delay when tracking a sinusoidal reference [18]. Controlling the grid current directly [19], [20] by using a proportional resonant controller (PR) enables tight tracking of sinusoidal signals at the resonance frequency with no phase error [21]. Parallel PR controllers [22]–[24] allow tracking references at multiple frequencies at the expense of increased computations. Considerations on the implementation of the PR controller were explained in [21], [24], [25], and tuning procedures in [18], [26], [27]. The proposed PFC+HMF uses a PR controller what guarantees fast and accurate tracking of the current reference without requiring additional sensors in the PFC. Considerations on discretization and parameter tuning of the PR controller are provided.

One more important element addressed in this paper is the PLL implementation for the PFC+HMF. Single-phase PFCs requires a PLL for synchronization with the voltage at the point of common coupling (PCC). PLLs based on adaptive filtering are now widely used; SOGI-PLL [28], [29] and the SOGI-FLL [28]. This paper proposes and computationally inexpensive implementation of the SOGI-PLL and parameter tuning considerations are also provided.

The elevated switching frequency puts high requirements for the DSP and efficient control algorithms should be proposed. The proposals in the paper provide all the steps for the straightforward control design of the PFC+HMF with fast calculations. The proposed HMF scheme allows moderate non-linear loads to be compensated at low cost, with only software modification and one current sensor for the non-linear load.

This paper is organized as follows: the current reference generator for the HMF in the hybrid AC/DC building is explained in Section II. Section III describes the utilization of PR controllers in PFC rectifiers. Section IV explains considerations on the implementation of the PR controller. Section V describes the efficient implementation of SOGI-PLL. Simulation and experimental results are shown in Section VI and VII respectively. Finally, Section VIII concludes the paper.

II. Harmonic Mitigation in Small Hybrid AC/DC Buildings using PFC

The proposed HMF in the small hybrid AC/DC building is constrained by the unidirectionality of the diodes in the PFC rectifier. Hence, the PFC current must have the same sign as the voltage.

A. Current reference generator for the harmonic mitigation function

In order to obtain the current reference for the HMF i^*_{PFC}, the non-linear load current i_{NL} is sensed. As the PFC rectifier is unidirectional, the necessary PFC current reference i^*_{PFC} added to the non-linear load current i_{NL} should result in a sinusoidal current waveform i_{PCC} at the PCC. For each fundamental semi-cycle $T_n/2$, the non-linear current i_{NL} is measured along with its phase angle ϕ_{NL}. The delimitation of each fundamental semi-cycle $T_n/2$ is implemented by synchronizing with the zero-crossing of the PLL output, which is a noise free signal that corresponds to the fundamental

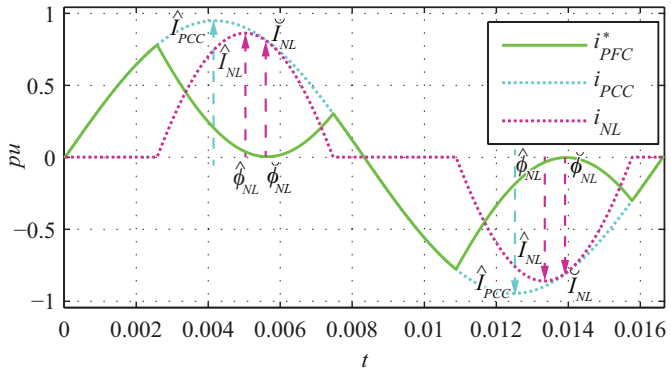

Fig. 3. Currents resulting from current reference generator for the HMF.

voltage. The PFC current reference needed to absorb the non-linear current is:

$$i^*_{PFC}(t) = \hat{I}_{PCC} \cdot \sin(\omega_n t) - i_{NL}(t) \tag{1}$$

with

$$\hat{I}_{PCC} = \breve{I}_{NL} / \sin(\breve{\phi}_{NL}) = \max_{t \in T_n/2} (i_{NL}/\sin(\phi_{NL})) \tag{2}$$

Thus, $\hat{I}_{PCC}$ corresponds to the largest value of the ratio $i_{NL}/\sin(\phi_{NL})$ for each semi-cycle, see Fig. 3. This corresponds to the tangent point, with amplitude $\breve{I}_{NL}$ and phase $\breve{\phi}_{NL}$. The PCC current will be sinusoidal with amplitude equal to $\hat{I}_{PCC}$ in phase with the PCC voltage $v_n = \sqrt{2} V_n \sin(\omega_n t)$, which is assumed to be perfectly sinusoidal for the sake of simplicity. It can be seen in Fig. 3 that $i^*_{PFC}(t)$ is positive for the positive PCC voltage (proportional to i_{PCC}), fulfilling the condition of unidirectionality in the PFC diodes.

B. Harmonic Composition Analysis

For the harmonic composition analysis it is assumed that the tangent point $\breve{I}_{NL}$ is close to the maximum point $\hat{I}_{NL}$ so $\hat{I}_{PCC} \approx \hat{I}_{NL}/\sin(\hat{\phi}_{NL})$, see Fig. 3. The harmonic composition of the non-linear current is as follows:

$$\begin{aligned} i_{NL}(t) &= \sum_{i=1}^{\infty} \sqrt{2} I_{NLi} \cdot \sin(i\omega_n t - \phi_{NLi}) \\ &= \sqrt{2} I_{NL1} \cdot \cos(\phi_{NL1}) \cdot \sin(\omega_n t) \\ &\quad - \sqrt{2} I_{NL1} \cdot \sin(\phi_{NL1}) \cdot \cos(\omega_n t) \\ &\quad + \sum_{i=2}^{\infty} \sqrt{2} I_{NLi} \cdot \sin(i\omega_n t - \phi_{NLi}) \end{aligned} \tag{3}$$

The first term of (3), fundamental current in phase with the PCC voltage, corresponds to the active power $P_{NL} = V_n I_{NL1} \cos(\phi_{NL1})$. The second term of (3), fundamental current in quadrature with the PCC voltage, corresponds to the reactive power $Q_{NL} = -V_n I_{NL1} \sin(\phi_{NL1})$. Finally, the last term of (3) corresponds to the harmonic current i_{NLh}.

Substituting (3) in (1), the harmonic composition of PFC rectifier current reference is as follows:

$$\begin{aligned} i^*_{PFC} &= \underbrace{\left(\hat{I}_{PCC} - \sqrt{2} I_{NL1} \cdot \cos(\phi_{NL1})\right)}_{\sqrt{2} I^*_{PFC1}} \cdot \sin(\omega_n t) \\ &\quad + \sqrt{2} I_{NL1} \sin(\phi_{NL1}) \cdot \cos(\omega_n t) \\ &\quad - \sum_{i=2}^{\infty} \sqrt{2} I_{NLi} \cdot \sin(i\omega_n t - \phi_{NLi}) \end{aligned} \tag{4}$$

The second term of (4), fundamental PFC current in quadrature with the PCC voltage, is to compensate the reactive power produced by the non-linear load (Q_{NL}) so the reactive power produced by the PFC is $Q^*_{PFC} = -Q_{NL}$. The third term of (4) cancels the harmonic currents produced by the non-linear load (i_{NLh}) so that the harmonic current produced by the PFC is $i^*_{PFCh} = -i_{NLh}$. These two cancellation terms are the usual ones in single phase active filters. However, the PFC rectifier, because of its unidirectionality, must consume active power $P_{PFC1} = V_n I^*_{PFC1}$ in order to perform the compensation. This requirement corresponds to the first term of (4), defined as $\sqrt{2} I^*_{PFC1}$, which is fundamental PFC current in phase with the PCC voltage. Substituting the definitions of the crest factor ($CF = I^{peak}/I^{rms}$) and the total THD of the load current, the required fundamental PFC current is:

$$\begin{aligned} I^*_{PFC1} &= \frac{\hat{I}_{PCC}}{\sqrt{2}} - I_{NL1} \cdot \cos(\phi_{NL1}) = \\ &= I_{NL1} \left(\frac{CF_{i_{NL}} \sqrt{1 + THD^2_{i_{NL}}}}{\sqrt{2} \cdot \sin(\hat{\phi}_{NL})} - \cos(\phi_{NL1}) \right) \end{aligned} \tag{5}$$

According to (5), the required current I^*_{PFC1} increases with the fundamental current, the harmonic content (CF and THD), and finally the displacement power factor ($DPF = \cos(\phi_{NL1})$) of the non-linear load. It is clear that this scheme only makes sense when the required active power P_{PFC1} is useful. The active power consumed by the PFC rectifier is determined by the closed loop control of the DC-link capacitor voltage. If the power requested by the PFC rectifier load is lower than the minimum power P_{PFC1}, the compensation scheme is not possible.

It is also clear that in order to permanently fulfill this condition the presence of permanently connected DC loads is necessary. Examples of permanently connected loads are fridges and HVAC for small residential buildings, and servers, showcase lights and parking lights for small commercial buildings. These loads maybe be smaller at night, but it is expected that the amount of harmonic current will also be smaller. This limitation is analogous to that of the power converters of renewable energy systems (wind and solar), which require not operating at full capacity in order to have available volt-ampere for harmonic compensation. The limitations in the HMF can be overcome by the low cost and widespread use of the proposed scheme. As with incentives to promote renewable energy systems, policies regarding the financial compensation for DC building owners who participate in the harmonic compensation

could be developed.

The proposed current reference generator for the HMF is fully consistent with the harmonic content analysis explained in [14], which uses the harmonic reference generator from [30]. This analysis considers symmetrical non-linear loads ($\hat{\phi}_{NL} \approx 90° - \phi_{NL1}$), which allows further simplification in (5) to obtain the value of the fundamental PFC current.

C. Stability considerations

It can be seen in (4) that the current reference to the PFC corresponds to the reactive power and all the harmonics of the non-linear load plus a fundamental component. The current reference generator for the HMF is a feedforward procedure that corresponds to the load detection method widely employed in shunt active power filters [31], [32]. This procedure is appropriate when the non-linear loads behave as current sources where the parallel inductance is much larger than the grid inductance [33]. In the shunt active power filter, the fundamental component is needed for compensating the converter losses. In the PFC, the fundamental component is required because of the PFC unidirectionality. Stability consideration for the load detection algorithm can be found in [33], [34].

Harmonic compensation in closed loop [35], [36] uses the grid current i_{PCC} as control variable. The slow DC-link voltage control generates the sinusoidal reference i^{ref}_{PCC}. The compensation is slow, but it is accurate [35] and has good stability characteristics [36]. In addition, the DC-link capacitors must be large enough to cope with the power variations in the non-linear load [36]. PFCs use electrolytic capacitors for DC-link and, thus, this requirement is not constraining. Fig. 6, explained later on, shows the block diagram for this approach in closed loop.

III. Use of proportional resonant controllers in PFC rectifiers

The PFC+HMF needs to be able to track the reference signal without phase error. This is achieved by the use of a PR controller, which resonant part allows the accurate tracking of the fundamental component of the current. This section describes the principle of operation of using a PR controller with the most well-known PFC topologies and the considerations that should be taken into account.

A. Boost PFC topology

The boost PFC topology is shown in Fig. 4. The current reference of the boost PFC rectifier is a signal proportional to the absolute value of the PCC voltage. This signal is obtained from the PLL synchronized to the grid PCC voltage. From the control perspective, the boost PFC can be seen as a regular boost DC/DC converter with variable input voltage and variable current reference. The input signal waveforms are the absolute value of sinusoidal functions. Fig. 4 highlights the semiconductors involved during the positive half of PCC

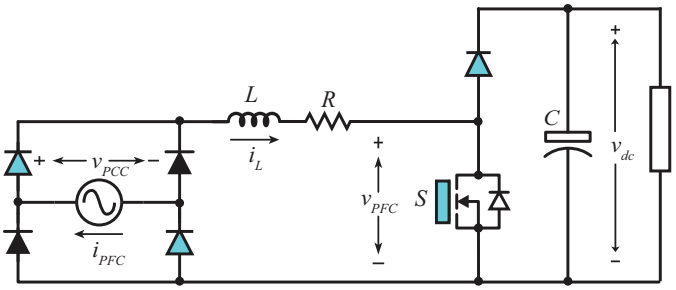

Fig. 4. Power factor correctors (PFC): boost topology

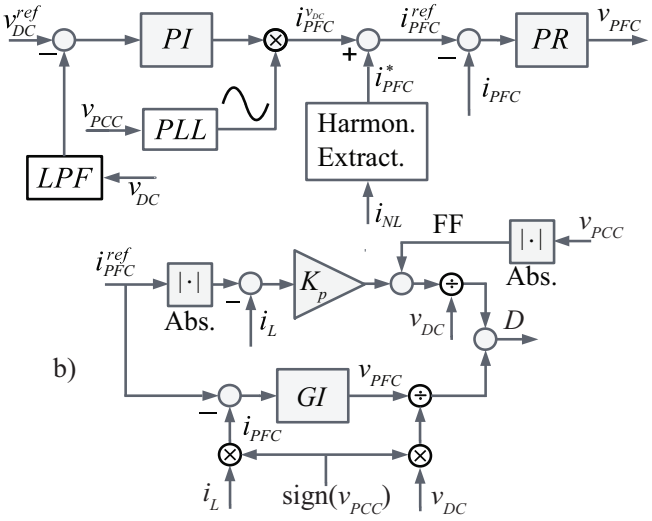

Fig. 5. a) Overall block diagram of the PFC with HMF. b) Detailed view of the PR implementation

voltage. In order to use a PR controller, the sinusoidal output current is directly controlled in the closed loop. For this purpose, the following transformation is used to obtain the sinusoidal output current i_{PFC} inferred from the inductor current and the PCC voltage:

$$i_{PFC} = i_L \cdot \text{sign}(v_{PCC}) \tag{6}$$

where i_L is the inductor current, v_{PCC} is the grid PCC voltage, and sign$(\cdot)$ is the sign function. The current reference is a sinusoidal waveform synchronized to the PCC voltage and limited to be:

$$\begin{aligned} 0 \le i^{ref}_{PFC} \le I^{max}_{PFC} \text{ for } v_{PCC} \ge 0 \\ -I^{max}_{PFC} \le i^{ref}_{PFC} < 0 \text{ for } v_{PCC} < 0 \end{aligned} \tag{7}$$

where I^{max}_{PFC} is the PFC converter current limit. These limits force the current to be positive when the PCC voltage is positive and vice versa. The output of the PFC boost converter v_{PFC} is related to the boost D_{cycle} duty cycle according to:

$$v_{PFC} = v_{DC} \cdot D_{cycle} \cdot \text{sign}(v_{PCC}) \tag{8}$$

with v_{DC} the DC-link voltage. This means that the boost PFC provides positive voltage v_{PFC} for positive PCC voltage v_{PCC} and vice versa.

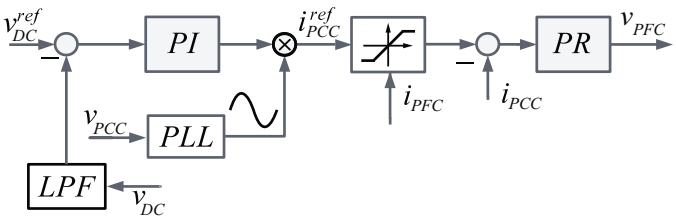

Fig. 6. Closed-loop approach for the HMF.

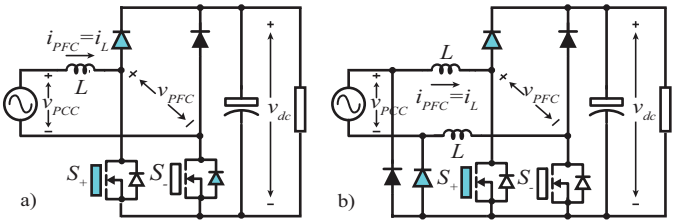

Fig. 7. Power factor correctors (PFC): a) bridgeless PFC and b) semi-bridgeless PFC.

Unlike previous approaches [19], [20], the proposed transformations require no additional sensors to infer the value of i_{PFC}. However, there is uncertainty in the current sign around the zero crossing due to the non-linear behavior of the real diodes. It is known that the low voltage around the zero crossing is a source of distortion in the PFC current depending on the PCC voltage, current and inductance [37], [38]. In order to reduce the effect of the misinterpretation in the current sign at the zero crossing, the proportional gain of the PR controller can be applied without the transformations (6)-(8) and with the current reference being a rectified sinusoidal as shown in Fig. 5b. In this form, the fast proportional action can correct potential errors caused by uncertainties. Comparing to the PI controller, the PR controller requires only one additional integrator as it can be seen in Fig. 8 (explained later on). In addition, the logic for selecting the proper voltage cycle (6)-(8) comprises only sign multiplications as it can be seen in Fig. 5b.

As depicted in Fig. 6, the closed loop approach of the controller employs i_{PCC} as the control variable. Since i_{PCC} is a measured sinusoidal variable transformation (6) is not necessary. In addition, it is difficult to protect the PFC converter as the current is not indirectly controlled. The current reference i_{PCC}^{ref} can be saturated to $\pm I_{PFC}^{max} + i_{NL}$ with $i_{NL} = i_{PCC} - i_{PFC}$ calculated from the measured i_{PCC} and (6).

When the PR controller is included in the PFC rectifier control, the overall block diagram, shown in Fig. 5a, is the same as that of a regular bidirectional grid-tie H-bridge [18]. This consists of two nested loops; the inner and faster for the PFC current i_{PFC} and the outer and slower for the DC-link voltage v_{DC}. In addition, the PFC rectifier must also produce the current reference for the HMF i_{PFC}^{*} explained in section II. Hence, the total current reference for the PR controller i_{PFC}^{ref} is the sum of the DC-link controller output $i_{PFC}^{v_{DC}}$ and the HMF current i_{PFC}^{*} as shown in Fig. 5a. The alternating power at twice the fundamental frequency and the harmonic power will reflect in the DC-link capacitor of the PFC rectifier as DC-voltage ripple. The DC-voltage should be low-pass filtered with a DC-voltage control bandwidth bellow twice the line frequency so as not to interference with the current loop. The HMF will only work when the DC-link voltage is properly regulated. For high and low values of DC-voltage, the compensation current reference should be progressively reduced.

B. Bridgeless and semi-bridgeless PFCs

Compared to the previous PFC boost topology, PFC topologies shown in Fig. 7, eliminates one diode from the line-current path reducing the conduction losses [10]. Because of the increasing pressure for better efficiencies, this bridgeless PFC topology is expected to be present in the AC/DC hybrid buildings. The topologies for the bridgeless PFC and the semi-bridgeless PFC [11] are shown in Fig. 7a and Fig. 7b respectively. Fig. 7a highlights the semiconductors involved during the positive semi-period of the PCC voltage in the bridgeless topology. The bridgeless topology can be viewed as a full bridge active rectifier, in which the upper switches have been removed because they are redundant when only unidirectional power flow is required. The current circulating through the converter inductor is the same as the grid current and a PR controller can be used to control it.

Fig. 7b highlights the semiconductors involved during the positive semi-cycle of the PCC voltage in the semi-bridgeless PFC. Two slow diodes have been added to clamp the output ground to the AC source terminals, and an additional inductor is needed for each half of the PCC voltage waveform. The resulting topology consists of two boost DC/DC converters, working alternatively for the positive and negative semi-cycle of the grid voltage waveform. From the control perspective, the alternating boost DC/DC converters of the semi-bridgeless PFC rectifier also have a variable input voltage, and the current reference is the absolute value of a sinusoidal waveform. In order to use PR controllers with the semi-bridgeless PFC, the previous transformations and limitations (6)-(8) must be applied to reconstruct the grid current from the inductor currents and the PCC voltage.

IV. Implementation of the PR controller

This section explains considerations on the discretization and proper tuning of the PR controller. The PR controller comprises two parts: a proportional gain and a generalized integrator (GI):

$$PR(s) = K_p + GI(s) = K_p + K_r \frac{2s}{s^2 + \omega_r^2} \qquad (9)$$

The GI has infinite gain at the resonant frequency $\pm\omega_r$, which enables any phase delay to be cancelled when tracking a sinusoidal signal.

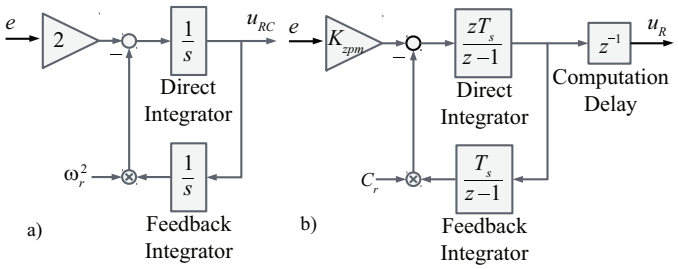

Fig. 8. a) Implementation of the resonant controllers using two integrators, b) proposed discretization.

A. Discretization

This section explains considerations on discretization to prevent mismatch in the resonance frequency between the continuous and discrete implementation of the PR controller. The GI part of the PR is usually implemented using two integrators, as shown in Fig. 8a. The Bilinear method with pre-warping (Tustin method) allows the characteristics of (9) at the resonant frequency to be preserved [39]. However, the use of the zero matching method allows one additional degree of freedom in the discretized equivalent that results in [25]:

$$GI(z) = K_{zpm}\frac{2(1-z^{-1})z^{-1}}{1-2z^{-1}\cos(\omega_r T_s)+z^{-2}} \tag{10}$$

The Fig. 8b shows the discrete implementation of the GI. In order to avoid an algebraic loop, [21] suggest to use forward Euler for the direct integrator and backward Euler for the feedback integrator. However, in the implementation of Fig. 8b uses backward Euler for the direct integrator, forward Euler for the feedback integrator, and incorporates the computation unit delay explicitly. This results in the same transfer function, and it is more convenient conceptually for automatic code generation from the simulation software. The code generation tool usually generates code for the control blocks and the computation delay results from the execution. The transfer function from direct discretization of both integrators is:

$$PR(z) = K_p + K_r\frac{2T_s(1-z^{-1})z^{-1}}{1+z^{-1}(C_r T_s^2-2)+z^{-2}} \tag{11}$$

The resonant frequency of the PR controllers is taken from the grid frequency calculated in the PLL [24], [40] to preserve the infinite gain at the resonant frequency. Considering that the grid frequency is always close to the rated grid frequency ω_n [18], it is proposed to use Taylor series around ω_n for $\cos\omega_r T_s$ in (10). This results in more accuracy for the same computational effort than using McLaurin series as was done in [24], [40]. Thus, the factor C_r in Fig. 8 is:

$$C_r = \frac{2}{T_s^2} - \frac{2}{T_s^2}\cos(T_s\omega_n) + \frac{2}{T_s}\sin(T_s\omega_n)(\omega_r-\omega_n) + \cos(T_s\omega_n)(\omega_r-\omega_n)^2 + \ldots \tag{12}$$

The gain K_{zpm} is selected to have the same value in the discrete and continuous domain for a critical frequency, usually DC $s = \omega j = 0$ [39]. In order to preserve the high gain characteristic around ω_r, the gain K_{zpm} is selected to have the same bandwidth (-3 dB) in the discrete equivalent as in the continuous system. The gain of the $GI(s)$ is -3 dB for the following frequency:

$$\omega_{-3\text{dB}} = \sqrt{\omega_n^2 + 4 \pm 4\sqrt{\frac{\omega_n^2}{2}+1}} \tag{13}$$

Therefore, $GI(z)$ at $z = e^{j\omega_{3\text{dB}}T_s}$ should have the same gain of -3 dB. Using the bilinear approximation $e^s \approx (1 + s/2)/(1 - s/2)$ and neglecting small second order terms, the gain K_{zpm} is selected as follows:

$$K_{zpm} \approx \frac{\omega_n T_s}{\sqrt{\omega_n^2+\sqrt{2}\omega_n}} \tag{14}$$

With these considerations the PR controller can be properly tuned to the grid frequency allowing the proper tracking of the fundamental component.

B. Parameter tuning

The HMF requires the proper tuning of the PR controller to attain a proper bandwidth for tracking the harmonic components. The proportional gain K_p of the PR controller determines the control bandwidth [21]. The GI has an effect only in the near range of the fundamental frequency [21], its effect is neglected for the rest of the frequency spectrum and only the proportional gain K_p is considered. The PWM and computation delays and the inductor resistance are also neglected and the plant is only $G_p(s) = 1/Ls$ with L the connection equivalent inductance. The closed loop system is as follows:

$$G_{cl} = \frac{K_p G_p(s)}{1+K_p G_p(s)} = \frac{1}{\frac{L}{K_p}s+1} \tag{15}$$

The bandwidth is $\omega_{bw} = 2\pi f_{bw} = K_p/L$ and must be selected well bellow the switching frequency. The proportional gain K_p for a bandwidth $f_{bw} \approx f_{sw}/10$ is:

$$K_p = \frac{2\pi L f_{sw}}{10} \tag{16}$$

This value is consistent with the suggested value of PI controllers in [41]. Considering the elevated switching frequencies (tens to hundreds kHz) the achieved bandwidth (kHz to tens of kHz) allows the proper tracking of the harmonic components in the HMF for the small hybrid AC/DC building.

In the following discussion, the integration time $T_r = K_p/K_r$ for the PR controller is defined as the ratio between the proportional and resonant gains. Assuming the same previous simplification, the transfer function relating the reference and the error is:

$$G_e(s) = \frac{e(s)}{y_{ref}(s)} = \frac{1}{1+\frac{PR(s)}{Ls}} \tag{17}$$

Considering as reference input a cosine step signal at the resonance frequency $y_{ref}(s) = s/(s^2+\omega_n^2)$, the tracking error is:

$$e_{approx}(s) = \frac{5T_s}{\pi\omega_r^2} \frac{s^2}{\frac{5T_s}{\pi\omega_r^2}s^3 + \frac{1}{\omega_r^2}s^2 + \left(\frac{2}{NT_s\omega_r^2} + \frac{5T_s}{\pi}\right)s + 1} \tag{18}$$

For the following derivations, the term s^3 is neglected for elevated switching frequencies and $2/(NT_s\omega_r^2) >> 5T_s/\pi$. The inverse Laplace transformation of (18) is a decaying exponential function multiplying sinusoidal functions. The decaying time constant and the initial value are respectively:

$$\tau = T_r \tag{19a}$$

$$e_{approx}(t=0) = -\frac{10}{\pi}\frac{T_s}{T_r} \tag{19b}$$

A conservative estimation of the settling time can be obtained by approximating the sinusoidal functions of the inverse Laplace transform of (18) to the unity. Therefore, as a simple decaying exponential with time constant with initial value (19),

$$e_{approx}(s) = -\frac{10T_s}{\pi}\frac{1}{T_r s + 1} \tag{20}$$

And the settling time (2%) is approximately:

$$t_{s2\%} = T_r \ln\left(\frac{500T_s}{\pi T_r}\right) \tag{21}$$

The settling time increases for increasing values of T_r, the estimation (21) increases for increasing values of T_r until it reaches a maximum. Therefore, the estimation (21) is valid for values of $T_r < 500T_s e^{-1}/\pi \approx 60T_s$, less than this maximum where the previous approximations do not hold anymore.

C. Stability

In the previous analysis, the PWM and computation delays and the inductor resistance were neglected. However, these parameters influence stability and should be considered. As the bandwidth was selected a decade lower than the switching frequency, the analysis can be safely done in the continuous domain. The transfer functions for the inductor, considering the resistance, and for the PWM and computation delays are respectively:

$$G_{RL}(s) = \frac{1}{Ls + R} \tag{22a}$$

$$G_{delay}(s) = \frac{1}{1.5T_s s + R} \tag{22b}$$

The PWM and computation delays, with duration a half and a full switching period respectively, are approximated as a first order system [41]. The open loop transfer function is $G_{cl}(s) = PR(s)G_{delay}(s)G_{RL}(s)$. The conditions for stability for the previous proportional gain (16) are obtained by applying the Routh-Hurwitz criterion to the denominator of the closed loop transfer function:

$$T_r > \frac{6L^2T_s\pi}{2L^2\pi + (10+3\pi)LRT_s + 15R^2T_s^2} \tag{23a}$$

$$T_r > \frac{6L^2T_s\pi}{2L^2\pi + (10+3\pi)LRT_s + 15R^2T_s^2 - 90LRT_s^3f_n^2\pi^2 - 60L^2f_n^2\pi^2T_s^2} \tag{23b}$$

It is clear that condition (23b) includes condition (23a) and both are satisfied for $T_r > 3T_s$. Taking into account this finding and (21), a proper value is:

$$T_r = 15T_s \tag{24}$$

This is ten times the time constant of $G_{delay}(s)$, as was proposed in [41] for PI controllers.

V. SOGI-PLL IMPLEMENTATION

The PLL enables the generation of the current reference signal and calculates the gri frequency what makes it an elemental subsystem of the PFC-HMF controller. This section explains the operation of the employed SOGI-PLL along with two algorithms that optimize the execution of the PLL. In this paper, the SOGI-PLL proposed in [29] and shown in Fig. 9 will be used for PCC voltage synchronization.

The SOGI-PLL consists of passing the PCC voltage through a bandpass and a low-pass filter. The filter is usually one SOGI section that enables the construction of a second order low-pass and a bandpass filter. The gain K is usually selected $\zeta = 0.707$ to result in a Butteworth filter. In this paper, it is proposed that K be selected to result in a Bessel filter, $\zeta = 0.866$, in order to better preserve the voltage waveform phase, as the Bessel filter has maximally linear phase response [42]. If the PCC voltage is very polluted, in [43] it is proposed to use the multiple SOGI sections to increase the harmonic attenuation. In such cases, it is proposed that the coefficients of the n SOGI sections will match a higher order ($2n$) Bessel filter in factored form, which can be found in [42].

The outputs of the bandpass and a low-pass filters result in two orthogonal components α and β, which are fed into a regular *dq*-PLL that calculates the grid frequency and phase (see Fig. 9). The procedure requires the application of a coordinate transformation given by,

$$v_{dq}^T = R(\theta_i)v_{\alpha\beta}^T = \begin{bmatrix} v_d' \\ qv_q' \end{bmatrix} = \begin{bmatrix} \cos\theta_i & \sin\theta_i \\ -\sin\theta_i & \cos\theta_i \end{bmatrix} \begin{bmatrix} v' \\ qv' \end{bmatrix} \tag{25}$$

The trigonometric operations in (25) make the algorithm computationally expensive. In order to reduce the computational burden two computationally efficient approaches are proposed:

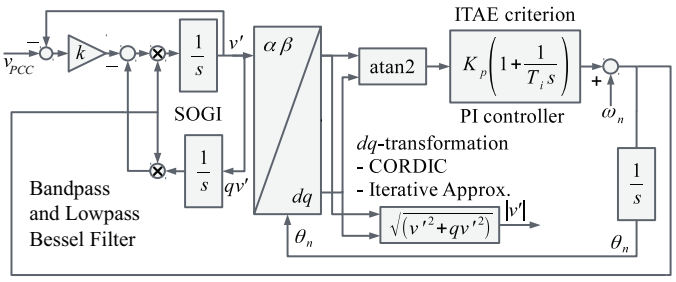

Fig. 9. Block diagram of the SOGI-PLL used for grid synchronization.

A. CORDIC algorithm

The CORDIC algorithm expresses the coordinate transformation matrix [44] in the following form:

$$R(\theta_i) = \frac{1}{\sqrt{1+\tan^2\theta}} \begin{bmatrix} 1 & \tan\theta_i \\ -\tan\theta_i & 1 \end{bmatrix} \tag{26}$$

In vectoring mode, the CORDIC algorithm selects angles $\gamma_i = \arctan(2^i)$ to rotate the vector v', qv' to x-axis. The operations $\tan(\gamma_i) = 2^i$ can be done with simple shifts in fixed-point hardware, see details in [45].

Hence, the CORDIC algorithm enables the calculation of the angle error $\arctan(qv'/v')$ in the PLL and the PCC voltage module $|v'|$ with low computational resources. The angle error is used in the PI controllers of the PLL, as it is shown in Fig. 9. The PCC voltage module $|v'|$ is necessary for the DC-link voltage control, in order to enable the proper working of the PFC rectifier at different grid voltage levels.

In addition, the module $|v'|$ value can be used to compensate the reactive power produced by the x-cap of the EMI filter. The usual remedy for this problem consists of delaying the current reference [46], and this problem worsens for light loads. Assuming that the voltage across the x-cap is approximately the PCC voltage, the consumed reactive power is $Q_x = v_{PCC}^2 C_x \omega_n$ with C_x the total capacitance of the x-caps. Therefore, a current component in phase with qv' and of module $|v'|C_x\omega_n$, both magnitudes estimated from the PLL, should be introduced to compensate the x-cap reactive power.

B. Iterative implementation

The phase angle is the output of an integrator fed by the PI controller output plus the feed-forward of the rated frequency, as shown in Fig. 9. Assuming Euler forward discretization for the integrator:

$$\theta_{i+1} = \theta_i + (\omega_n + u_{PIn})T_s \tag{27}$$

where ω_n refers to the rated frequency, which is fed-forward for fastest settling time, and u_{PIn} is the PI controller output, which is limited for antiwindup. Hence, the coordinate transformation is:

TABLE I
PARAMETERS FOR THE SIMULATIONS AND EXPERIMENTS.

Parameter	Symbol	Value
Rated AC voltage	V_n	120 V
Rated current	I_n	2.8 A
Rated frequency	f_n	60 Hz
Inductor inductance	L	0.550 mH
Inductor resistance	R	7 Ω
DC link voltage	v_{DC}	200 V
DC link capacitor	C_{DC}	560 µF
Sampling frequency	f_s	60 kHz
PWM frequency	f_{sw}	60 kHz

$$R(\theta_{i+1}) = R(\theta_i)R(\omega_n T_s)R(u_{PIn}T_s) \tag{28}$$

The matrix $R(\omega_n T_s)$ is fixed and can be pre-calculated. By limiting the output $u_{PIn} < \pm 0.75/T_s$, the coordinate transformation matrix can be approximated using Taylor series:

$$R(\theta) = \begin{bmatrix} 1-\frac{\theta^2}{2} & \theta \\ -\theta & 1-\frac{\theta^2}{2} \end{bmatrix} \tag{29}$$

with an accuracy less than 10% using far fewer operations. The limitation in the output u_{PIn} results in a slower response. Higher limits for u_{PIn} can be selected by using more Taylor terms in (29) for faster response at the expense of more computations. After calculating the *dq*-components of the PCC voltage, the angle error must be calculated by using the arctangent function that can be approximated as a division $\text{atan2}(v_q, v_d) \approx v_q/v_d$.

The double integrator (system type II) of the PLL allows the ramp angle reference to be followed without steady state error. The proportional gain and integration time are proposed to be tuned to get the optimum coefficients in the closed loop transfer function based on the ITAE criterion (damping factor $\zeta = 1.6$ [47]) for a ramp input:

$$K_p = 5.76 f_{bw} \approx \frac{43.2}{t_s} \tag{30a}$$

$$T_i = \frac{1.76}{f_{bw}} \approx \frac{t_s}{4.2} \tag{30b}$$

with t_s the settling time (1%), usually 100 ms for this type of PLL [18], and f_{bw} the bandwidth (-3 dB).

VI. SIMULATION RESULTS

Table I shows the parameters of PFC+HMF (boost topology) used in the simulations. The control blocks were modeled using Matlab/Simulink and the semiconductor devices using PLECS.

Fig. 10a compares the temporal response to the cosine step input when using a PR controller and a traditional PI controller. The controllers are enhanced by an input voltage feed-forward path. It is worth mentioning that back-calculation or conditional-integration, instead of limited integration, is needed as anti-windup mechanism in the PI controller. For

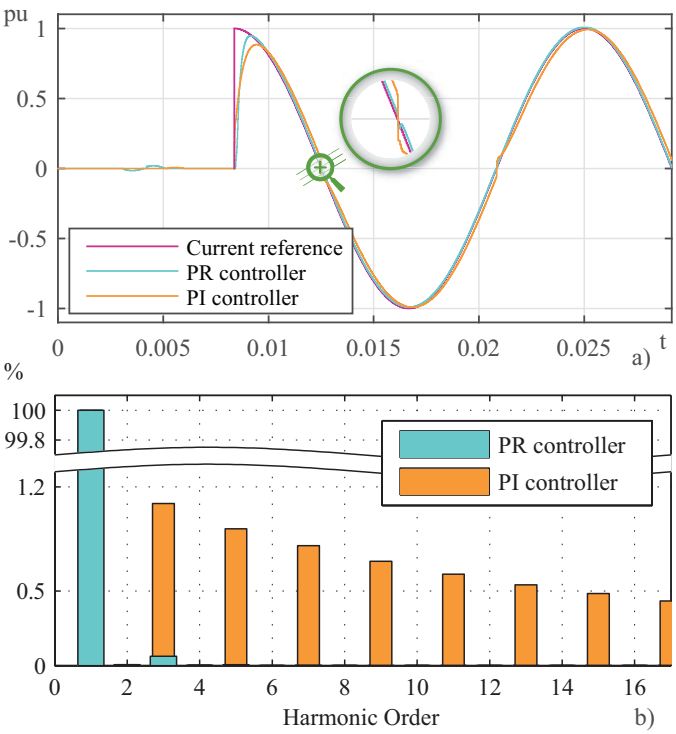

Fig. 10. Comparison between a) the cosine-step responses and b) low-frequency spectra of PR and PI controllers (simulation results) in the boost PFC current control. The PR controllers results in faster response, power factor closer to unity, and lower harmonic content.

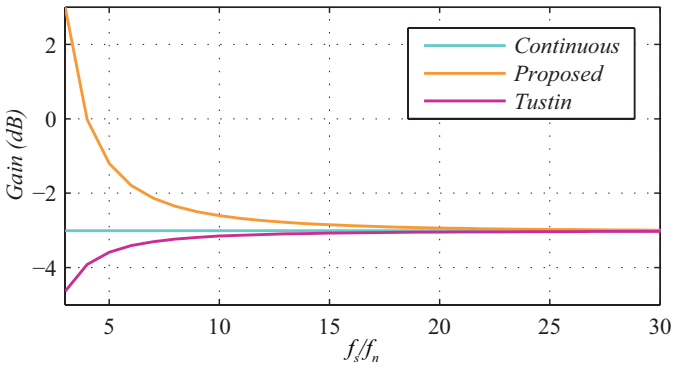

Fig. 11. Gain of the PR controller for the continuous case, the proposed zero pole matching, and Tustin with pre-warping. For moderate sampling frequencies, $7 < f_s/f_n < 20$, the proposed gain K_{zpm} guarantees a higher bandwidth in the discrete model.

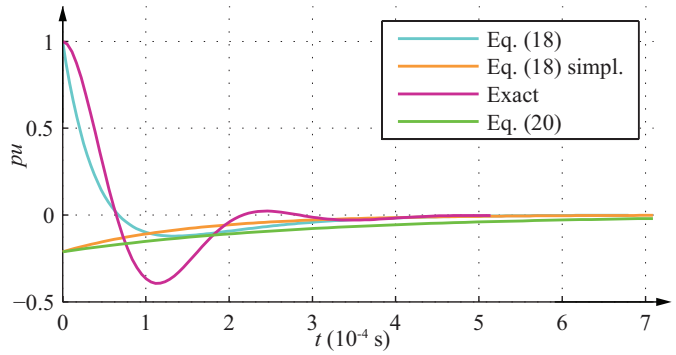

Fig. 12. Tracking error versus time of the different approximation for the cosine step input in the PR controller. Eq. (20) leads to a very conservative estimation for the settling time (21) that is simple to calculate and does not require simulations.

the PR controller, the transformations (6)-(8) are used to infer the grid current and the selected anti-windup mechanism is conditional-integration. Both controllers have the same proportional gain (16) with approximately the same bandwidth $f_{bw} \approx f_{sw}/10$. The integration time (24) is the same for both controllers, ten times the smallest time constant of the control plant $\tau = 1.5T_s$ [41], as explained in Subsection IV-B. It can be seen that the response when using the PR controller is faster. The PR controller allow to accurately track the sinusoidal reference with no delay resulting in better power factor. The small variations for the PR controller, before the cosine step input, are due to the proportional action at the zero crossing. Finally, the use of the PR controller results in less zero-crossing distortion as shown Fig. 10a, and this results in lower harmonic content as shown in Fig. 10b.

Fig. 11 shows the gain at $\omega_{-3\text{dB}}$ (13) for the continuous case and the discrete cases at different sampling frequencies f_s. The discrete cases are the proposed zero-pole mapping discretization with gain K_{zpm} according to (14) and the usual Tustin with pre-warping $K_{zpm} = \sin(T_s\omega_n)/\omega_n$. For low switching frequencies, $f_s/f_n < 7$, the proposed gain K_{zpm} results in overly large values and the Tustin gain in low values (and so narrower bandwidth). For these cases the gain K_{zpm} should be calculated numerically in order to preserve the same bandwidth in the continuous and discrete cases. For moderate sampling frequencies, $7 < f_s/f_n < 20$, the proposed gain K_{zpm} guarantees a higher bandwidth in the discrete model. For high sampling frequencies, $f_s/f_n > 20$, the differences between the three cases are indistinguishable as expected.

Fig. 12 compares the tracking error of the cosine step input when using a PR controller for the exact model, the approximation according to (18), the approximation (18) neglecting the third order term, and finally the approximation according to (20). The settling times (2%) for the different cases are 39 ms, 38 ms, 35 ms and 70 ms respectively. Hence, the model according to (18) is very accurate, even when neglecting the third order term. Because of the simplifications, the model according to (20) leads to a very conservative estimation (21), as stated in its derivation in Subsection IV-B, which is simple to calculate and does not require simulations.

Fig. 13 compares phase tracking of SOGI-PLL with and without the simplifications proposed in Subsection V. The PCC voltage is polluted with a 5$^{\text{th}}$ harmonic component (10% amplitude) and, after one cycle, there is a step increase in the PCC voltage frequency of 10%. It can be seen that the voltage phase is properly tracked by the SOGI-PLL with simplifications. As expected, the reduction in the number of computations increases the response time from 17.9 ms to 26 ms for 1% phase error.

The following Figs. 14-17 show the behavior of the overall systems, comprising the non-linear load and the PFC+HMF.

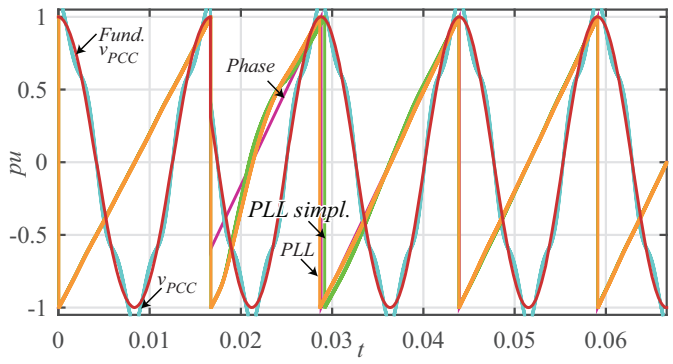

Fig. 13. Phase response of the SOGI-PLL with and without simplifications. The voltage phase is properly tracked by the SOGI-PLL with simplifications at the expense of the longer response time, from 17.9 ms to 26 ms for 1% phase error.

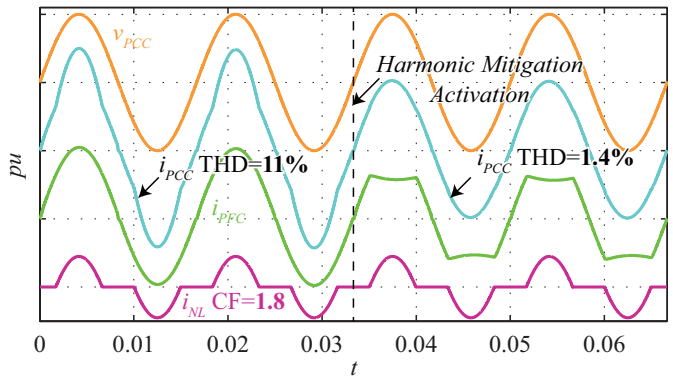

Fig. 14. Simulation results: activation of the HMF in the PFC. After the activation of the HMF, the THD of the PCC current decreases from 11% to 1.4% complying with norms.

For more clarity, as the DC-voltage loop results in slow dynamics, the simulations are conducted assuming constant DC-voltage and considering only the current control. In addition, the average output of the PFC magnitudes is shown, the switching ripple would be superimposed. Fig. 14 shows the activation of the HMF after two fundamental cycles. The non-linear load has a crest factor $CF = 1.8$ and the reference current $i_{PFC}^{v_{DC}}$ of the PFC+HMF (Fig. 5) is 100% the rated current. Before the activation of the HMF, the PCC current has an unacceptable $THD_{PCC} = 11\%$, which it is later reduced to $THD_{PCC} = 1.4\%$, fully complying with the harmonic injection norms. Fig. 15 shows the behavior of the PFC+HMF when the non-linear load starts. The reference current $i_{PFC}^{v_{DC}}$ of the PFC+HMF is 100% the rated current and, initially, the PCC current is sinusoidal with $THD_{PCC} = 0.5\%$. After the non-linear load begins, the HMF also begins. The THD of the PCC current is increased to $THD_{PCC} = 1.4\%$, fulfilling the norms with a wide margin.

Fig. 16 shows the behavior of the overall system for a step change in the reference current $i_{PFC}^{v_{DC}}$ of the PFC+HMF from 50% to 100% the rated current. Initially, the PCC current has a $THD_{PCC} = 4.1\%$ and, after the PFC+HMF load steps, it has a $THD_{PCC} = 1.4\%$. Fig. 17 shows the behavior of the PFC+HMF for a non-linear load with a displacement factor

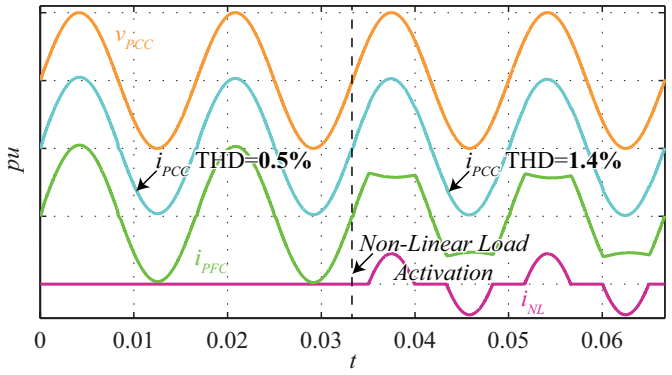

Fig. 15. Simulation results: overall system behavior upon the beginning of the non-linear load. Despite the non-linear load activation the THD remains lower than 5 % complying with the norms.

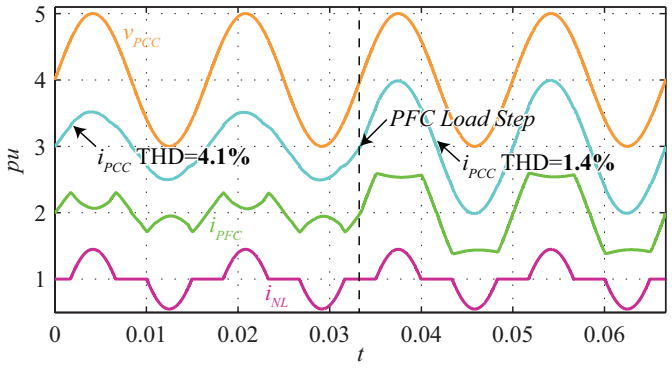

Fig. 16. Simulation results: overall system behaviour for a step change in the reference current $i_{PFC}^{v_{DC}}$ of the PFC+HMF. The increase in the PFC load increases the fundamental component of the PCC current leading to a lower THD.

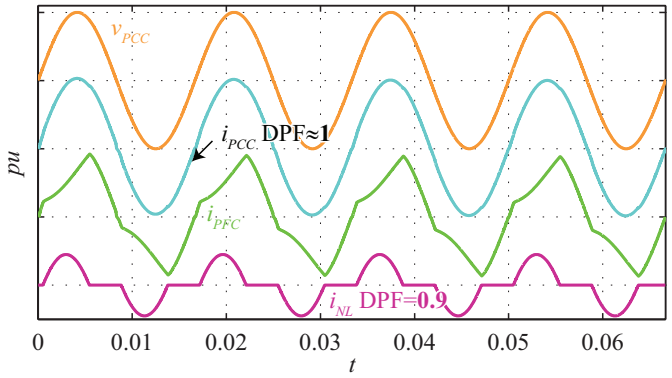

Fig. 17. Simulation results: PFC+HMF behavior when the non-linear load has displacement factor different from unity. The PFC+HMF is able to fully compensate the reactive power as the conditions explained in Section II are fulfilled.

of $DPF_{NL} = 0.9$. It can be seen that the PCC current is in phase with the PCC voltage, so that the $DPF_{PCC} \approx 1$. The PCC current has a $THD_{PCC} = 1.4\%$. Therefore, for this particular non-linear waveform, the PFC+HMF is able to fully compensate the reactive power as the conditions explained in Section II are fulfilled.

Fig. 18a shows the behavior of the PFC+HMF when the

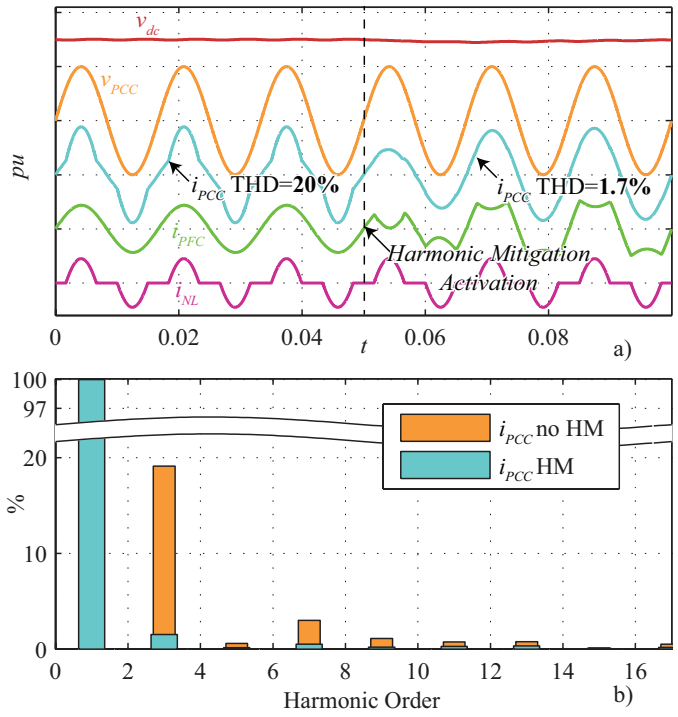

Fig. 18. Simulation results: a) PFC+HMF when the DC-voltage control loop is present. b) Low-frequency spectra of i_{PCC} without and with HMF. The THD of the PCC current is reduced from 20% to 1.7% similarly to the previous cases.

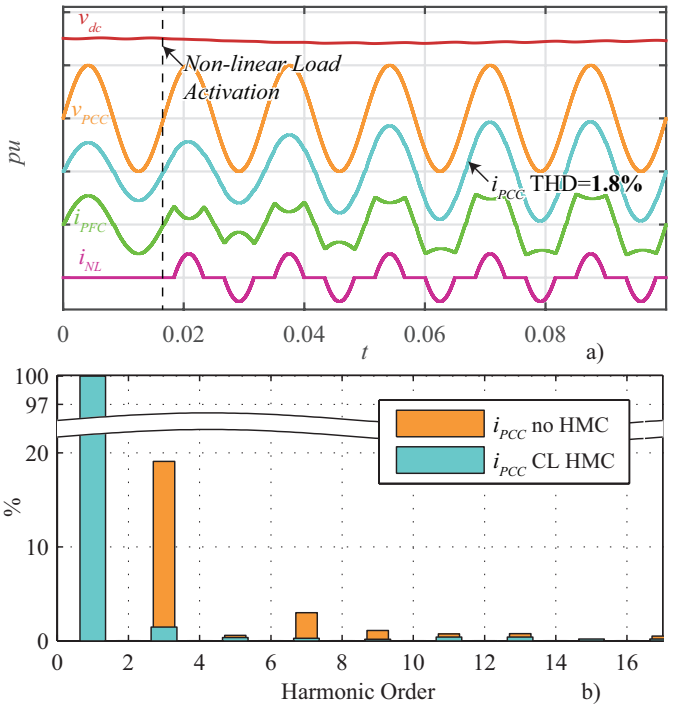

Fig. 19. Simulation results: a) PFC+HMF when the DC-voltage control loop is present for the closed-loop approach. b) Low-frequency spectra of i_{PCC} without and with HMF. The THD of the PCC current is reduced from 20% to 1.8% similarly to the previous cases.

DC-link voltage control loop is present. Without the HMF, there is a PCC current with $THD_{PCC} = 20\%$. The activation of the HMF begins after three line cycles, and the PCC current has $THD_{PCC} = 1.7\%$, a little higher than previously due to the presence of the DC-link voltage ripple. Fig. 18b shows the low-frequency spectra for the i_{PCC} with and without HMF. It can be seen that all the low-frequency harmonics were conveniently reduced. Finally, Fig. 19a shows the behavior of the PFC with the HMF in closed loop as explained in Subsection II-C. As expected the response is slower, it can be see it takes more cycles to achieve $THD_{PCC} = 1.8\%$ almost the same final as in the previous case. Fig. 19b shows the low-frequency spectra for the i_{PCC} with and without HMF in closed loop. For this case, all the low-frequency harmonics are also reduced.

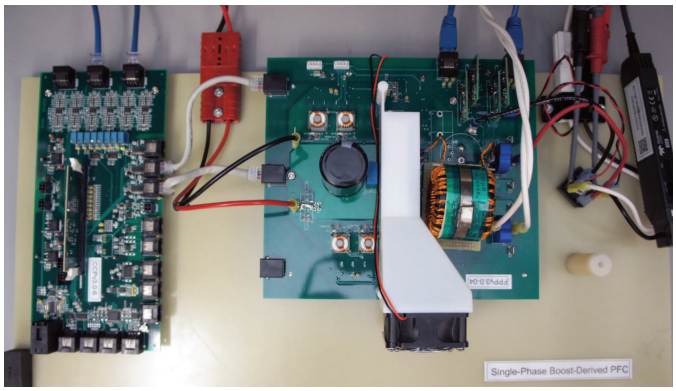

Fig. 20. Laboratory set-up for the experiments.

VII. Experimental Results

Fig. 20 shows the set-up used for the experiments. The parameters of the boost PFC+HMF are the same as those shown in Table I for the simulations. All the algorithms were performed using a DSP (C2000 family by Texas instruments), which was programmed in C.

Fig. 21a shows the response in the time domain to the sinusoidal reference when using the PR controller and Fig. 21b the low-frequency spectrum. Fig. 21 also shows a detailed view of the zero-crossing. The zero-crossing departs from Fig. 10 because of the unmodeled non-linearities. This results in an increased harmonic content, yet fulfilling the norms, especially in the third harmonic as it can be seen in Fig. 21b.

Figs. 22-28 show the same experiments as were performed in the previous simulations, see Fig. 14-18. The current ripple in the experiments is negligible because of an additional high-frequency filter in the prototype. The experimental results are in close agreement with the previous simulation results. Fig. 22 shows the overall system behavior upon the activation of the HMF. The non-linear load has a crest factor $CF = 1.8$ and the reference current $i_{PFC}^{v_{DC}}$ of the PFC+HMF, see Fig. 5, is 100% the rated current. Before the activation of the HMF, there was a $THD_{PCC} = 17.75\%$, which later was reduced to be $THD_{PCC} = 1.66\%$. Fig. 23 shows the behavior of the PFC+HMF, when the non-linear load starts. The PFC+HMF load is 100% the rated current and the PCC current presents a $THD_{PCC} = 2.25\%$ which is partially due to the zero-

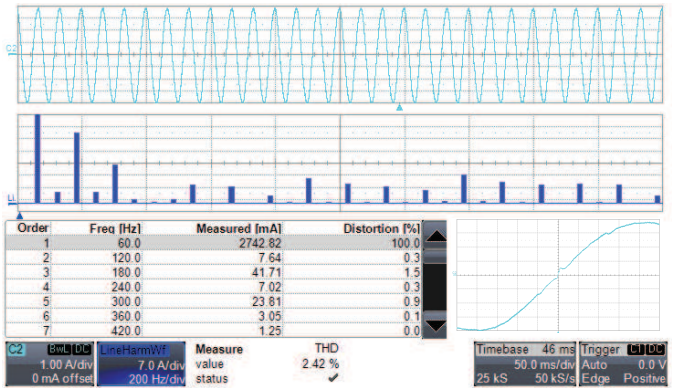

Fig. 21. Experimental results: Steady state response in the time domain to the sinusoidal reference when using the PR controller, detailed view of the zero-crossing distortion and low-frequency spectrum of the current.

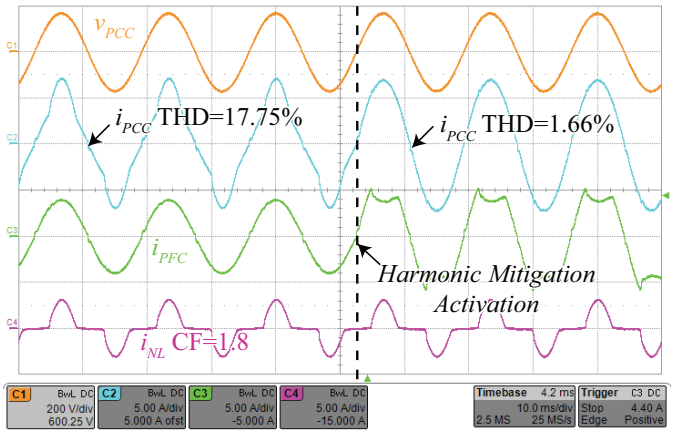

Fig. 22. Experimental results: activation of the HMF in the PFC. After the activation of the HMF, the THD of the PCC current decreases from 17.75% to 1.66% complying with norms and having results similar to the simulations.

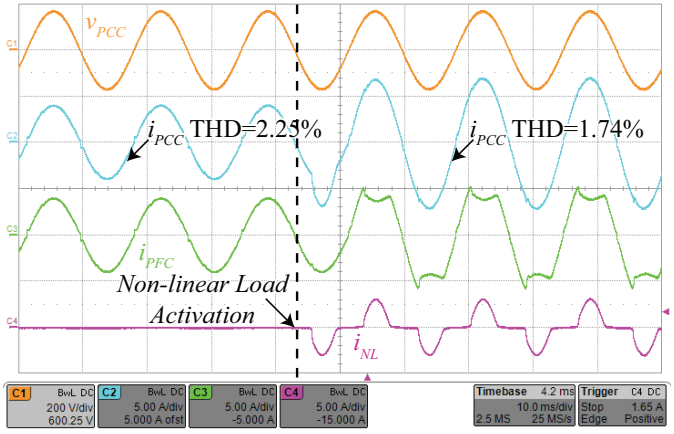

Fig. 23. Experimental results: overall system behavior upon the beginning of the non-linear load. Despite the non-linear load activation the THD remains lower than 5 % complying with the norms. The reduction in the THD is due to the increase in the fundamental component of the PCC current.

crossing distortion. After the non-linear load begins, the PCC current lowers the THD ($= 1.74\%$) due to the increase in the fundamental component.

Fig. 24 shows the transition for a step change in the reference current $i_{PFC}^{v_{DC}}$ of the PFC from 50% to 100% the rated current. Initially, the PCC current THD is $THD_{PCC} = 2.19\%$ and, after the PFC load step, it is $THD_{PCC} = 1.62\%$. Fig. 25 shows the HMF of the PFC in the face of a non-linear load with displacement factor different from unity. The PFC+HMF puts the PCC current in phase with the PCC voltage with $THD_{PCC} = 1.87\%$.

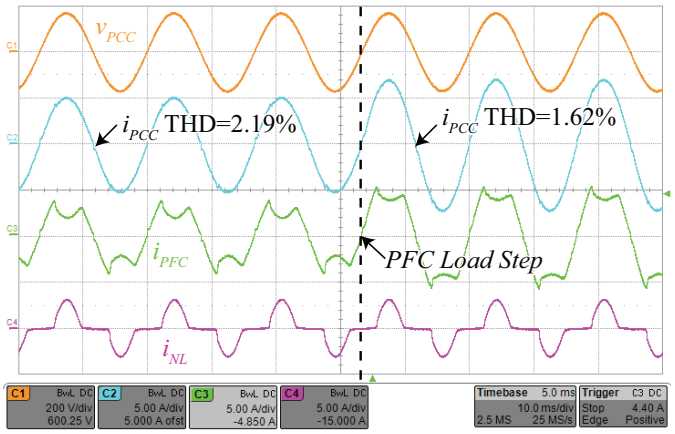

Fig. 24. Experimental results: overall system behaviour for a PFC+HMF load step. The increase in the PFC load increases the fundamental component of the PCC current leading to a lower THD.

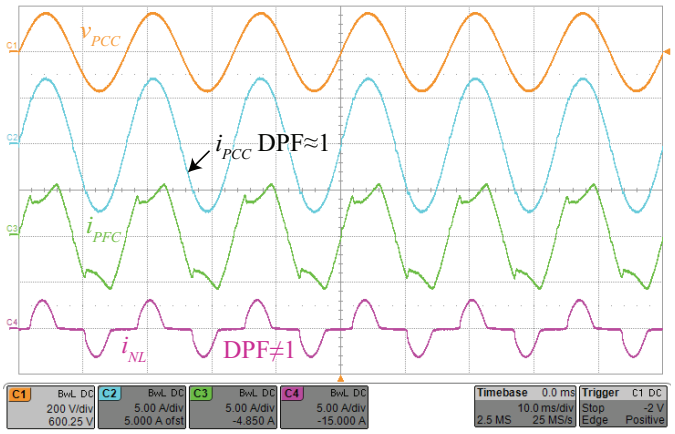

Fig. 25. Experimental results: PFC+HMF behavior when the non-linear load has displacement factor different from unity.

The low-frequency spectra of the grid current at the PCC i_{PCC} are shown in Figs. 26 and 27, for half and full power consumption in the PFC respectively. It can be seen that the HMF works in both cases with better THD for higher load as expected.

Finally, Fig. 28 shows the behavior of the PFC+HMF when the DC-link voltage control loop is present. The DC-voltage transient lasts longer than in the previous simulation because the PI controller of the DC-voltage in the prototype has a lower bandwidth, however this does not affect the performance of the HMF. Without the HMF, there is a PCC current with $THD_{PCC} = 24.7\%$. After activation of the HMF, the PCC current has $THD_{PCC} = 3.91\%$, which fulfills the norms, and which is higher than previously due to the presence of the DC-link voltage ripple.

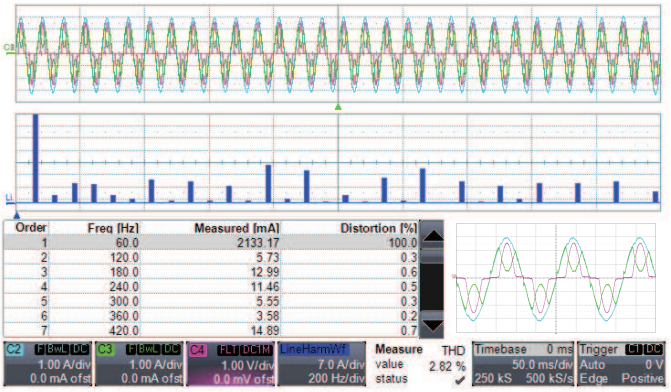

Fig. 26. Experimental results: Steady state response of currents i_{PFC}, i_{NL} and i_{PCC}. Low-frequency spectrum of the current i_{PCC} for low power.

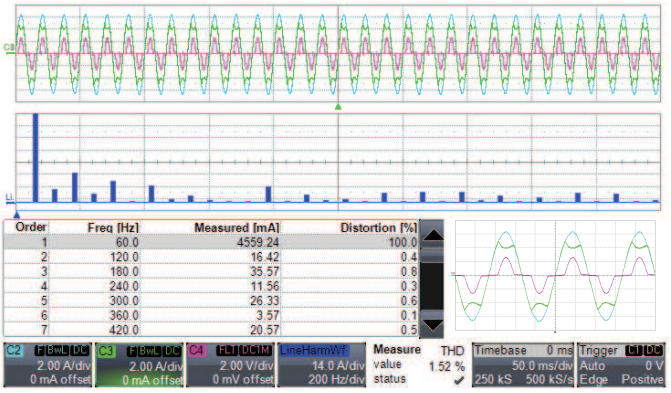

Fig. 27. Experimental results: Steady state response of currents i_{PFC}, i_{NL} and i_{PCC}. Low-frequency spectrum of the current i_{PCC} for full power.

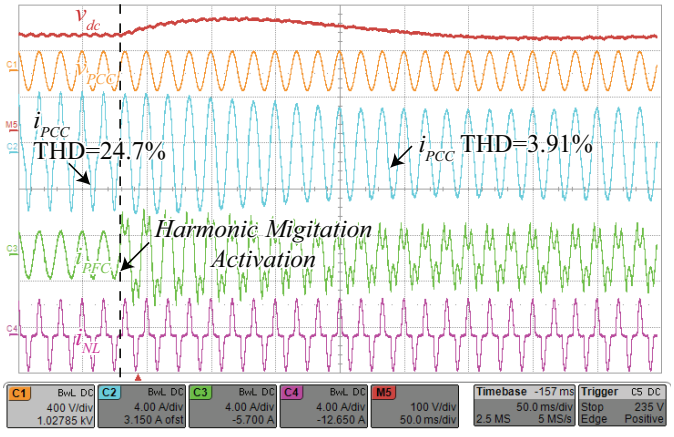

Fig. 28. Experimental results: PFC+HMF when the DC-voltage control loop is present.

VIII. Conclusion

The paper proposes the control design of a PFC with harmonic mitigation function for being employed in small hybrid AC/DC buildings. The proposed controller is comprised of a current reference generator, a PR controller, and a PLL. The current reference generator for the harmonic mitigation function was explained along with the limitations of the procedure. It was shown that, because of its unidirectionality, the single-phase PFC rectifier needs to consume active power for performing the HMF. The PFC rectifier used a PR controller by inferring the output current without needing additional sensors in the rectifier, which allowed proper tracking of the fundamental component. An efficient implementation for the SOGI-PLL that enables fast execution is presented. The paper provided full guidelines on obtaining all the necessary parameters for a computationally efficient control of the PFC+HMF. The experiments presented showed that the PFC+HMF is able to reduce the THD of the PCC current from $THD_{PCC} = 24.7\%$ due to a high crest factor load to $THD_{PCC} = 3.91\%$, complying with the norms. The proposed scheme utilizes the installed hardware and only requires software modification and the addition of a single external sensor to measure the non-linear load. Therefore, the proposed PFC+HMF presents an economically attractive option for reducing the harmonic production of small hybrid AC/DC buildings.

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