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# **Electrical Stress in High Voltage Capacitor Units**

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### **ABSTRACT**

Capacitor banks, power electronic as part OŤ within modern converters power systems, are vulnerable to failures which can cascade over time and which result from stresses placed on capacitor units from a power system. This study uses COMSOL Multiphysics<sup>®</sup> software to develop plots of electric field strength and evaluate regions of high electric field stress within simplistic capacitor modules. It finds that electric fields arise between adjacent elements, around foil edges, along the length of a draw lead included in the interleaved discrete-foil unit design. Moreover, as nonlinear voltage distributions arise in used to find voltage distributions for each foil in a unit, nonlinear, possibly due to stray capacitances with unevenly distributed too.

## SIMULATION AND RESULTS

#### Multislice: Electric potential (V) $\times 10^4$ 0.9 0.8 0.7 0.6 0.5 0.4 0.3 0.2 IVIIIIII 0.1 Z --¥



Figure 4. Voltage distribution in an interleaved foil unit DISCUSSION

Electrical circuit and electric currents interfaces are Voltage differences between adjacent foils (Table 2) are



**Figure 1**. Capacitor banks in an HVDC filter hall

### INTRODUCTION

Renewable connections, power factor correction, and HVDC links all use power electronics and capacitor banks. Two HVDC converter station capacitor banks are in Figure 1: each has an array of individual capacitor units which sit on racks at tiered voltages, and which are connected to support reactive power and to form part of tuned filters.

capacitor units, field stresses are shown to be as shown in Figure 4 and explored in Tables 1 and 2. An housing, which can in turn provoke unequal electric field stresses, which are illustrated in Figures 5 to 9.

	Foil Terminal Voltages (V)								
Winding	5	4	3	2	1	0			
5	1367.7	1010.8	701	402.18	171.34	0			
4	1367.7	1761.3	2153.2	2555.5	2932.4	3342.9			
3	5613	5151.1	4695.1	4232.4	3781.6	3342.9			
2	5613	6078.3	6548.6	7010.8	7461.1	7892.9			
1	10000	9575.3	9144.6	8730.1	8303.8	7892.9			
<b>Table 1.</b> Foil terminal voltages (aligned with Figure 4)									

Surface: Electric field norm (V/m) V/m  $2.09 \times 10^{6}$  $\times 10^{6}$ 1.5 0.5 ▼ 1.17×10<sup>-14</sup>

**Figure 5.** Field stress on a centrally bisecting cut plane



electrostatics interface uses these voltages to show field stresses between element terminals. Highest stresses occur at bushings and connections to internal elements, where the draw lead has notable influence on local electric fields, as visible with de-normalised colouring in Figures 8 and 9. Foil element edges and corners can be folded, but can also be designed with bend radius in mind to limit local field stress.

#### **Development Approach**



**Figure 10.** Simple approach with control flow support

COMSOL Multiphysics<sup>®</sup> is a powerful environment for multiphysics modelling. It even offers some control flow in creating a geometry: parameters and conditional statements are used for the geometry sequence in this study to improve its ease of development and readability; to allow various styles of model, and to let it be readily adapted and reconfigured. There is, however, only strict support for repetition in geometries (arrays) only), and no support for either of these forms of control flow in definitions, on which materials, mesh, and boundary conditions can all be based.



**Figure 2.** A capacitor model of 5 windings of 5 elements

Capacitor banks are susceptible to electrical stresses and are also enclosed. It can therefore be difficult to detect developing or incipient faults, which, if cause breakdown, can cultivate cascading failure [1]. To highlight locations where such faults might develop, this study employs a discrete foil capacitor model [2] (Figure 2 and with cut planes in Figure 3), of 5 elements in each of 5 series connected windings. It connects to a 10 kV voltage using circuit and electric currents interfaces, and has 3.9 relative permittivity dielectric.

**Figure 6.** Cut line field plots for YMin, YMid, and YMax Surface: Electric field norm (V/m)



**Figure 7.** Z5 cut plane of EF stresses through windings

#### Surface: Electric field norm (V/m)

# CONCLUSIONS

Electrical field stresses are found to be:

1. strongest around terminals: in connecting elements to bushings and where bushings meet module housing; 2. between adjacent windings, due to voltage variation; 3. shared disproportionately by elements due to nonlinear voltage distribution across element foils; 4. prominent at foil corners and edges, validating a practise of folding corners and edges in manufacture; 5. influenced by foil fold turn severity, which suggests bend radius might best be maximised where possible; 6. heightened where terminals separate to interleave; 7.affected by having a draw lead, which validates documented wisdom [1] in support of even winding number designs to avoid the need for one.

The narrowness of foil windings contributes to the electric field stresses within a unit. It might be possible to choose winding designs which achieve a similar capacitance with broader turns (increased turn radius). Such design trade-offs could reduce stress and prolong capacitor design life.



Figure 3. Position of cut lines on a module's Z axis



**Figure 8.** Draw lead influence on stresses near housing

	Foil Terminal Voltage Differences (V)							
Winding	5-4	4-3	3-2	2-1	1-0			
1	356.9	309.8	298.82	230.84	171.34			
2	393.6	391.9	402.3	376.9	410.5			
3	461.9	456	462.7	450.8	438.7			
4	465.3	470.3	462.2	450.3	431.8			
5	424.7	430.7	414.5	426.3	410.9			

**Table 2.** Foil terminal voltage differences

#### REFERENCES

[1] M. Ellis, D. J. Meisner, M. Thakur, "Innovative protection schemes for H configuration fuseless grounded shunt capacitor banks", pp. 449-458, 2012.

[2] W. J. Sarjeant, J. Zirnheld, F. W. MacDougall, "Capacitors", *IEEE Transactions on Plasma Science*, Vol. 26, No. 5, October 1998.

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