# High-Power Medium-Voltage Three-Phase ac-dc Buck-Boost Converter for Wind Energy Conversion Systems

Fahad Alsokhiry[1], Ibrahim Abdelsalam [2], Grain Philip Adam[3*], Yusuf Al-Turki [1]

[1] Electrical and Computer Engineering Department, King Abdulaziz University, Jeddah, Kingdom of Saudi Arabia
[2] Electrical and Control Department, College of Engineering & Technology, Arab Academy for Science, Technology & Maritime Transport, Cairo, Egypt
[3] Electronic and Electrical Engineering Department, University of Strathclyde, Glasgow, UK
Email: grain.adam@strath.ac.uk

**Abstract: This paper proposes three topologies of single-stage three-phase ac-dc buck-boost converters suitable for medium-voltage and high-power wind energy conversion systems (WECS). The proposed converters draw sinusoidal input currents with nearly unity power factor from wind generators over wide range of ac voltages and frequencies. The proposed converters reduce the voltage and current stresses on the self-commutated switching device compared to existing solutions; thus, promising for new generation of relatively cheap WECSs. The proposed converters operate in Discontinuous Condition Mode (DCM), with their ac terminals connected to three-phase generator with open ended windings, or to ac supply using three single-phase transformers with isolated windings at converter side. The validity of the proposed converters and its detailed theoretical analysis and discussions are confirmed using PSCAD/EMTDC simulations, and further corroborated by experimentations, considering different operating conditions.**

## Nomenclature

δ: Duty cycle.
$\delta_c$: Critical duty cycle
$\omega_g$: Generator speed
$\omega_{opt}$: Optimal speed
*CCM:* Continuous conduction mode
*DCM*: Dissentious conduction modes
$D_{BD1}$ to $D_{BD3}$ : Sub-converter blocking diodes
$D_{FW1}$ to $D_{FW3}$ : Sub-converter freewheeling diodes
$f_s$ *: S*witching frequency
$f$ : Supply fundamental frequency
$I_c$ : dc-link capacitor current
$I_{c\_avr}$ : Average dc-side capacitor current
$I_p$ : Peak fundamental supply current
$I^*_p$ : Reference peak fundamental supply current
$L_{dc1}$ to $L_{dc3}$ : dc-link inductances
$L_{dc\_slc}$ :Selected dc-link inductance for given circuit operation
$I_{La}$, $I_{Lb}$ , and $I_{Lc}$ : dc-link inductance current
$I_{Lmax\_a}$, $I_{Lmax\_b}$, and $I_{Lmax\_c}$ : Peak dc inductor currents
$i_{s1}$ to $i_{s6}$ : Currents in the switches of the sub-converters
$i_{ra}$ ,$i_{rb}$ ,and $i_{rc}$ : Fundamental component of the pre-filter input current
$i_{r\_rms}$ : Pre-filter input root mean square current
*MPPT* :Maximum power point tracking
*PI* : Proportional integral
*R* : Load resistance
$t_{xa}$, $t_{xb}$ and $t_{xc}$ Deplete times of the energy stored in the dc-link inductors
$T_s$ : Switching period
$V_{dc}$ : dc link voltage
$V_m$ : Peak of phase voltage
$v_{s(a)}$,$v_{s(b)}$, and $v_{s(c)}$ : Three-phase supply voltages
*WECS* : Wind energy conversion system
*ZCS* : Zero current switching

## 1 Introduction

Today ac-dc converters are widely used in many applications, ranging from power supplies for domestic apparatus to wind energy conversion systems [1-5]. The dc voltage is easily provided from ac voltage by using diode or thyristor rectifier; however, this approach leads to injection of significant current harmonics into the ac power supply, and suffers from low power factor. These problems are easily addressed by using self-commutated power converters that employ semiconductor devices with turn

on and off capability and can be controlled using high frequency pulse width modulation [6-13]. Significant efforts have been invested into the development of new generations of three-phase ac-dc converters that push the current and voltage harmonics far away from the power frequency range. This approach helps most of the existing ac-dc converters to meet the strict power quality regulations and offer the flexibilities needed in WECSs.

In recent years, a number of ac-dc converters have been proposed[14-17], for example, converter topology presented in [18-21] boosts the output voltage, but it requires additional circuitry to pre-charge the dc-side capacitors and to enable buck operation (step-up and step-down of dc voltage) [22]. Thus, the approach in [22] increases the cost and circuit complexity plus it suffers from control difficulties during transition between the boost and buck modes.

In [23-30], several ac-dc converters that offer buck-boost capability in a single stage have been proposed. The single-stage ac-dc buck-boost converter presented in [23] is attractive due to simplicity of its power circuit, which consists of a three-phase diode rectifier and conventional buck-boost converter. But its operation in continuous conduction mode (CCM) that necessitates the use of relatively large energy storage elements, and this increase its weight and size. Also, it draws sinusoidal currents from ac side at nearly unity power factor in a limited range, around the rated load. Additionally, the main downside of the ac-dc buck-boost converter in [23] are: it requires large ac-filters; and the worst-case voltage stress on the semiconductor switches is excessively high, and equals to the peak of line-to-line voltage imposed at the ac side of the rectifier plus the dc link voltage. The ac-dc buck-boost converter proposed in [24] uses four active switches, and requires only one control signal to drive these switches. The converter in [24] operates in DCM and injects high quality sinusoidal input currents into ac side, with high power factor, but the voltage stresses on the semiconductor switches remain prohibitively high. In [25], a buck-boost ac-dc converter that uses two semiconductors switches, and offers modest reduction in the worst-case voltage stress on semiconductor switches (to the peak of the phase ac voltage at converter ac side plus dc link voltage) was proposed. In reference [23], three topologies of single-stage ac-dc buck-boost converter were proposed. The first and second converter topologies predominantly share the same attributes and limitations of the converters presented in [23, 25], particularly, with regard to the quality of input currents and voltage stress on the semiconductor switches. While the third topology uses a single-phase ac-dc buck-boost converter proposed in [31] for each phase, and connects the dc outputs of the sub-converters in series. Thus, reduces the voltage stress per switch to phase voltage plus one third of the output dc voltage. But the current stress on the semiconductor switches increases. References [29, 30, 32] presented a three-phase single-stage buck-boost ac-dc converter that offers a stable dc output and injects sinusoidal currents into the ac grid with near unity power factor over the entire operating range (CCM and DCM). However, its main shortcomings are: large number of switching devices; and it inserts excessive number switching devices in conduction path, which may increase the semiconductor losses. Although the presented converter has exhibited relatively low efficiency (74%-87%), substantial improvement in the efficiency could be achieved, particularly, in high-power applications by restricting the switching frequency to less than 4 kHz and adoption of MOSFETs instead of IGBTs and ultra-fast recovery diodes throughout the circuit instead of rectifier diodes that suffer from significant recovery losses.

Two methods to reduce the current stresses on the semiconductor switches of the ac-dc buck-boost converter that operates under DCM have been investigated in [33]. This investigation shows that the parallel charging and discharging can successfully address the problem of high current stress when buck-boost converter operates in DCM. The cascaded buck boost converter proposed in [17, 34, 35] consists of two half-bridge (buck leg and boost leg) and intermediate inductance, it was originally proposed for use in electrical vehicle battery charger and PV applications. But this topology needs sophisticated controller to facilitate smooth transition between bucks and boost modes as suggested in [36, 37]. The ac-dc buck-boost converters proposed in [38-40] operate under discontinuous dc-link inductor current mode and inject sinusoidal currents into ac side with high power factors and reduced switching frequency. However the current stresses on some of the converter switches are much higher than the converter rated current.

This paper proposes three topologies of single-stage three-phase ac-dc buck-boost converters that operate at relatively low switching frequency (1kHz to 4kHz), and suitable for high-power medium-voltage applications, and capable of providing stable dc output voltage over full operating range, with controlled black-start and shutdown capabilities. Each of the proposed converters consists of three single-phase modules of non-inverting buck-boost converter shown in Fig. 1, with each module or sub-converter is rated at one-third of the total converter rated power. The basic theoretical analysis, design equations of the proposed converters are described and substantiated by simulations and experimentations.

## 2 Fundamentals of non-inverting ac-dc buck-boost converter

In module in Fig. 1, the switch $S_1$ and diode $D_{FW}$ are referred to as 'supply-side set', and the switch $S_2$ and diode $D_{bd}$ are termed 'load-side set'. A single gating signal is needed to turn the switches $S_1$ and $S_2$ on and off; however, the switches $S_1$ and $S_2$ require separate gate drives as they operate at different potential or insulation level relative to ground. The converter in Fig. 1 represents the basic building block of the proposed converters and it facilitates buck-boost operation without the aforementioned shortcomings. The converter in Fig. 1 is characterised by reduced voltage stress on the power electronics devices compared to the conventional buck-boost converter, where the maximum voltage stress per switching device is equal to the peak ac supply voltage plus the dc load voltage. During discharging mode (discharge of the dc side inductor as it supplies the load and charges the output capacitor $C_{dc}$), the Diode $D_{fw}$ conducts, and in this mode the supply voltage is separated from the load circuit, with the switch $S_1$ blocks the supply side voltage, and switch $S_2$ blocks the full dc load voltage.

Fig. 2(a), Fig. 3(a), and Fig. 3 (b) show the proposed single-stage ac-dc buck-boost converters. In topology 'A', the dc output terminals are series connected as shown in Fig. 2 (a); thus, reduces the voltage stress on the semiconductor switches. Topology 'B' in Fig. 3 (a) is abandoned because of the load-side power devices are exposed to extremely high current stress, which is equivalent to the discharge currents of the three dc side inductors. The topology 'C' solves the problem of topology 'B' by using three load-side power devices to share the total discharge currents due to parallel connection, see Fig. 3 (b). Additionally, the parallel connection of the sub-converters in Fig. 3 (b) reduces the discharge time and make the duty cycle operating range wider, and also allows the use of relatively large dc-side inductance while operating under DCM; thus, it reduces the current stress on the sub-converters' power electronic devices.

## 3 Three series connected single-phase ac-dc buck-boost converter (topology 'A')

### 3.1 Converter Structure

Fig. 2 (a) presents a three-phase ac-dc buck-boost converter that consists of three modules of single-phase ac-dc buck-boost converters, with their dc outputs connected in series (this converter will be referred to as topology 'A'). The proposed converter facilitates even sharing of the total dc link voltage between the three series connected modulates, with each module contributes and blocks one third of the total output power and dc link voltage respectively. The ac terminals of the diode bridge of each module of each phase-leg is connected to one phase of permanent magnet synchronous generator (PMSG) with open-ended windings as shown in Fig. 2 (a), or to three-phase transformer with isolated secondary windings (converter side). When topology 'A' operates in DCM, it guarantees sinusoidal input currents with nearly unity power factors over the entire operating range, and this is achievable using small ac filters. The voltage gain and the critical duty cycle $\delta_c$ that define the boundary between CCM and DCM operation of topology 'A' are [23].

$$Vdc = \frac{\sqrt{3}}{2}\delta V_m \sqrt{T_s R / L_{dc}} \quad (1)$$

$$\delta_c = 1 - 2\sqrt{3 L_{dc} f_s / R} \quad (2)$$

Where, $V_m$ is the peak of phase voltage, $V_{dc}$ is the dc link voltage, $T_s$ refers to switching period and $R$ is the load resistance.

The dc-side inductance is selected such as the converter operates in the boundary between CCM and DCM at its rated load. The equation used for selection of dc-side inductance ($L_{dc\_slc}$) is:

$$L_{dc\_slc} = \frac{1}{4} R T V_m^2 \Big/ \left(V_m + \frac{1}{3}V_0\right)^2 \quad (3)$$

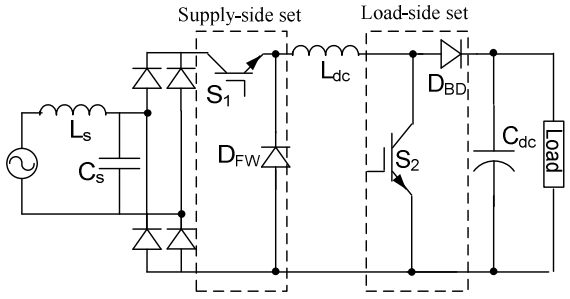



*Fig. 1.* ***Single-phase version of non-inverting buck-boost converter.***

### 3.2 Proposed controller

This section discusses the control strategy of the topology 'A', considering two operating scenarios:

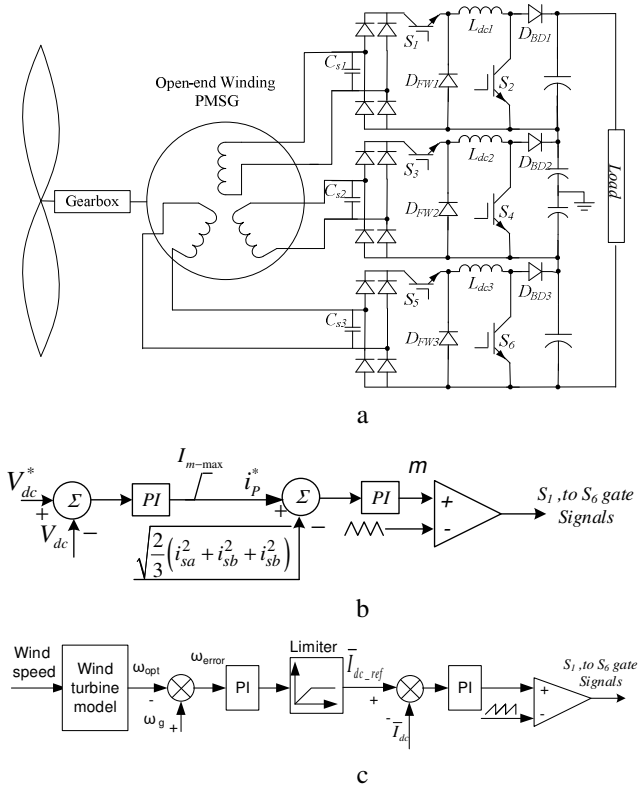
1- Topology ‘A’ ac side is connected to an ac supply with fixed ac voltage and frequency and its dc side is connected to a resistive dc load.

2- Topology ‘A’ ac side is connected to variable speed WECS that operates with maximum power tracking (MPPT) and its dc side connected to a fixed dc-bus voltage.

Fig. 2 (b) shows control system employed when topology ‘A’ feeds islanded dc load, and it consists of inner and outer control loops. The outer control loop regulates the total output dc voltage $V_{dc}$, in which the proportional-integral (PI) controller defines the desired peak fundamental supply current $I^*_p$ in order to achieve any desired dc output voltage $V_{dc}$. The added current limiter aims to protect converter from overload or overcurrent during abnormal operation. The inner control loop uses a simple PI controller to force the peak supply current to follow its reference and estimates the duty cycle $\delta$ of the switches $S_1$ to $S_6$.

When topology ‘A’ is employed in WECS, the control system is modified as in Fig. 2 (c), which incorporates wind turbine and drive train model and necessary parameters for calculation of optimal generator speed $\omega_{opt}$. A PI controller is used to calculate the reference average dc current $I_{dc\_ref}$ corresponding to maximum power point. The speed controller forces the measured generator speed to follow the optimal speed which is set by the MPPT controller. The functions of the inner current control loop are regulation of the average dc current $I_{dc}$ and synthesis of the duty cycle for the switches $S_1$ to $S_6$.

When the generator speed ($\omega_g$) exceeds the optimal speed ($\omega_{opt}$), the speed controller increases the dc current $I_{dc}$, which in turn increases the electromagnetic torque to slow down the turbine speed ($\omega_g$) as the delivered power to the dc side increases.




a

b

c

Fig. 2. Three series connected single-phase ac-dc buck-boost converter topology ‘A’ and its control system.
(a) Proposed three series connected single-phase ac-dc buck-boost converter (topology ‘A’), (b) controller for islanded operation, and (c) Controller for operation as part of WECS.

## 4 Three parallel connected single-phase ac-dc buck-boost converter topology ‘B’ and ‘C’

In circuit topologies ‘B’ and ‘C’, the three dc inductors are parallel connected during discharging, with the stored energy in these inductors are being transferred to the dc load, with sufficient speed and constant average current. This topology removes the sixth time line frequency ripples from the dc side; thus, allowing the use of small capacitance for dc side filtering. Moreover, the fast energy transfer allows the converter to use relatively large dc inductance while the converter remain operating in DCM, and this feature is beneficial as it reduces the peak charging currents and current stresses on the semiconductor devices.

### 4.1 Converter Structure Difference between Topology ‘B’ and ‘C’

Fig. 3 (a) and (b) show two versions of three-phase ac-dc buck-boost converters which are formed by parallel connection of dc terminals of single-phase ac-dc buck-boost converters, and these converters will be refer to as topologies ‘B’ and ‘C’.

Topology 'B' uses three dc inductors and one switches to realize boost functionality; but the major downside of this configuration is that the boost switch '$S_2$' in Fig. 3(a) suffers from extremely high current stress as it exposed to the total dc current. Whilst topology 'C' realizes both buck and boost functions on per phase basis, with the current stresses at boost stage are evenly distributed between the switches $S_2$, $S_4$ and $S_6$ and diodes $BD_1$, $BD_2$ and $BD_3$. Thus, the topology 'C' is easily extended to high power high currents applications, without the drawbacks of the topology 'B'.

Fundamentally, topologies 'B' and 'C' have the same operating modes. However, this paper abandons topology 'B' for the aforementioned reasons, and considers and favours DCM of topology C in more detailed on the ground of minimizing the size and weight of the passive components, and or the simplicity of gating all six active semiconductor switches using the same gating signal.

### 4.2 Circuit analysis and voltage equations

Exploiting the symmetry behaviour of three-phase supply voltage, the analysis of topology 'C' can be performed, considering time range $0°\leq\omega t\leq 60°$. The switching frequency $f_s$ is assumed to be much higher than the supply fundamental frequency $f$, and each switch period is assumed to be fixed, and the voltage drops in the series elements in the ac side are assumed to be sufficiently small and can be neglected.

#### 4.2.1 *Mode 1 ($0<t<\delta T$)*

This mode represents dc inductors charging mode, where the six switches are simultaneously turned on to energize the dc side inductors from the ac side. During this mode, the dc inductor currents increase as shown in Fig. 3(b), while the dc-side capacitor discharges as it supplies the dc load. With the three-phase supply voltages expressed as in (4), the dc inductor voltages and capacitor currents are derived as in (5) and (6) respectively.

$$\begin{aligned} v_{sa(t)} &= V_m \sin(\omega t) \\ v_{sb(t)} &= V_m \sin\left(\omega t - \tfrac{2}{3}\pi\right) \\ v_{sc(t)} &= V_m \sin\left(\omega t + \tfrac{2}{3}\pi\right) \end{aligned} \qquad (4)$$

$$\begin{aligned} V_{La} &= \left|v_{sa(tk)}\right| = L_{dc}\, dI_{La}/dt \\ V_{Lb} &= \left|v_{sb(tk)}\right| = L_{dc}\, dI_{Lb}/dt \\ V_{Lc} &= \left|v_{sc(tk)}\right| = L_{dc}\, dI_{Lc}/dt \end{aligned} \qquad (5)$$

$$i_c(t) = -V_{dc}/R \qquad (6)$$

Assuming constant phase currents during each switching period $T_s$, the peak dc inductor currents ($I_{Lmax\_a}$, $I_{Lmax\_b}$, and $I_{Lmax\_c}$) when the six switches are turned off (at $t=\delta T$) can be approximated by (7):

$$\begin{aligned} \mathrm{I}_{L\max\_a} &= \left|v_{sa(tk)}\right| / L_{dc} \times \delta T \\ \mathrm{I}_{L\max\_b} &= \left|v_{sb(tk)}\right| / L_{dc} \times \delta T \\ \mathrm{I}_{L\max\_c} &= \left|v_{sc(tk)}\right| / L_{dc} \times \delta T \end{aligned} \qquad (7)$$

In each switching period, the equivalent continuous current in the switches $S_1$ to $S_6$ and pre-filter input current are:

$$\left.\begin{aligned} i_{s1} = i_{s2} &= \tfrac{1}{2}\delta I_{L\max\_a} = \tfrac{1}{2}\delta^2 T V_m \left|\sin\omega t\right| / L \\ i_{s3} = i_{s4} &= \tfrac{1}{2}\delta I_{L\max\_b} = \tfrac{1}{2}\delta^2 T V_m \left|\sin\left(\omega t - \tfrac{2\pi}{3}\right)\right| / L \\ i_{s5} = i_{s6} &= \tfrac{1}{2}\delta I_{L\max\_c} = \tfrac{1}{2}\delta^2 T V_m \left|\sin\left(\omega t + \tfrac{2\pi}{3}\right)\right| / L \end{aligned}\right\} 0 \leq \omega t \leq \pi \quad (8)$$

$$\left.\begin{aligned} i_{ra} &= \tfrac{1}{2}\delta^2 T V_m \left|\sin\omega t\right| / L_{dc} \\ i_{rb} &= \tfrac{1}{2}\delta^2 T V_m \left|\sin\left(\omega t - \tfrac{2\pi}{3}\right)\right| / L_{dc} \\ i_{rc} &= \tfrac{1}{2}\delta^2 T V_m \left|\sin\left(\omega t - \tfrac{2\pi}{3}\right)\right| / L_{dc} \end{aligned}\right\} 0 \leq \omega t \leq 2\pi \qquad (9)$$

Equation (9) shows that the fundamental component of the pre-filter input current is sinusoidal and in-phase with the supply voltage, this reduces the size and simplifies the design of the ac-side L-C filters.

4.2.2 Mode *2 ($\delta T<t< t_{xb}$)*

This mode represents the period when all the six switches $S_1$ o $S_6$ are off, and the dc-side inductors are parallel connected as they supply the dc load and charge the dc filter capacitor, through the freewheeling diodes ($D_{FW1}$ to $D_{FW3}$) and blocking diodes($D_{BD1}$ to $D_{BD3}$), see Fig. 3(d). The voltage impressed across the dc inductors in this mode is equal to the load voltage, but with negative polarity. The dc inductors' voltages and currents, and dc capacitor current are:

$$V_{La}=V_{Lb}=V_{LC}=-V_{dc} \tag{10}$$

$$\begin{aligned}
&\delta T\le t\le t_{xa}: I_{La}(t)=\frac{-V_0}{L_{dc}}(t-\delta T)+\mathrm{I}_{Lmax_a}=\frac{-V_{dc}}{L_{dc}}(t-\delta T)+\frac{\left|v_{sa(tk)}\right|}{L_{dc}}\delta T\\
&\delta T\le t\le t_{xb}: I_{Lb}(t)=\frac{-V_0}{L_{dc}}(t-\delta T)+\mathrm{I}_{Lmax_b}=\frac{-V_{dc}}{L_{dc}}(t-\delta T)+\frac{\left|v_{sb(tk)}\right|}{L_{dc}}\delta T\\
&\delta T\le t\le t_{xc}: I_{Lc}(t)=\frac{-V_0}{L_{dc}}(t-\delta T)+\mathrm{I}_{Lmax_c}=\frac{-V_{dc}}{L_{dc}}(t-\delta T)+\frac{\left|v_{sc(tk)}\right|}{L_{dc}}\delta T
\end{aligned} \tag{11}$$

$$I_C = I_{La} + I_{Lb} + I_{Lc} - I_0 \tag{12}$$

Where $t_{xa}$, $t_{xb}$ and $t_{xc}$ are the times take to deplete the energy stored in each dc inductor in Mode#1; $t_{xa}$, $t_{xb}$ and $t_{xc}$ can be calculated by equating each sub-equation in (11) to zero.

$$\begin{aligned}
t_{xa} &= \frac{\left|v_{sa(tk)}\right|}{V_{dc}}\delta T\\
t_{xb} &= \frac{\left|v_{sb(tk)}\right|}{V_{dc}}\delta T\\
t_{xc} &= \frac{\left|v_{sc(tk)}\right|}{V_{dc}}\delta T
\end{aligned} \tag{13}$$

4.2.3 *Mode 3($t_{xb}\le t\le T$):*

In this mode, the energy stored in the dc inductors is fully exhausted before the next switching period; thus, the dc-side inductor currents and voltages are zero, and dc link capacitor current is:

$$i_C(t) = -\frac{V_{dc}}{R} \tag{14}$$

By considering the three intervals, the average capacitor current during one switching cycle is:

$$\overline{I_c} = \frac{1}{T_s}\left(\int_0^{\delta T_s} I_C dt + \int_{\delta T_s}^{\delta T_s+t_{xa}} I_{La} dt + \int_{\delta T_s}^{\delta T_s+t_{xb}} I_{Lb} dt + \int_{\delta T_s}^{\delta T_s+t_{xc}} I_{Lc} dt + \int_{\delta T_s+t_{xc}}^{T_s} I_C dt\right) \tag{15}$$

$$\overline{I_c} = \frac{3\delta^2 T V_m^2}{4L_{dc}V_{dc}} - \frac{V_{dc}}{R} \tag{16}$$

Since the symmetrical characteristics of the three-phase supply at $0°\le\omega t\le 60°$, the average dc-side capacitor current can calculated as:

$$I_{c\_av} = \frac{3}{\pi}\int_0^{\frac{\pi}{3}}\left[\frac{3\delta^2 T V_m^2}{4L_{dc}V_{dc}} - \frac{V_{dc}}{R}\right] d\omega t \tag{17}$$

$$I_{c\_av} = 3\left(\frac{T\delta^2 V_m^2}{4L_{dc}V_{dc}} - \frac{V_{dc}}{3R}\right) \tag{18}$$

During steady-state, the average capacitor current is zero; thus, the converter dc output voltage can be calculated as:

$$V_{dc} = \delta V_m\sqrt{\frac{3RT}{4L_{dc}}} \tag{19}$$

For a given dc-side inductance, the critical duty cycle $\delta_c$ that defines the boundary between CCM and DCM can be calculated be setting $T=t_{on}+t_{xb,}$ and $|v_{sb(tk)}|=V_m$ for $0°\le\omega t\le 60°$. From (13) and (19), $\delta_c$ is:

$$\delta_c = 1 - \frac{2\sqrt{3}}{3}\sqrt{\frac{L_{dc}}{RT}} \quad (20)$$

Equations (19) and (20) can be used to select the required dc-side inductance to ensure the proposed converter operates in the boundary between CCM and DCM as:

$$L_{dc\_slc} = \frac{3RTV_m^2}{2(V_m + V_{dc})^2} \quad (21)$$

The following equation can be used to calculate the root mean square current at the input of the rectifier stage:

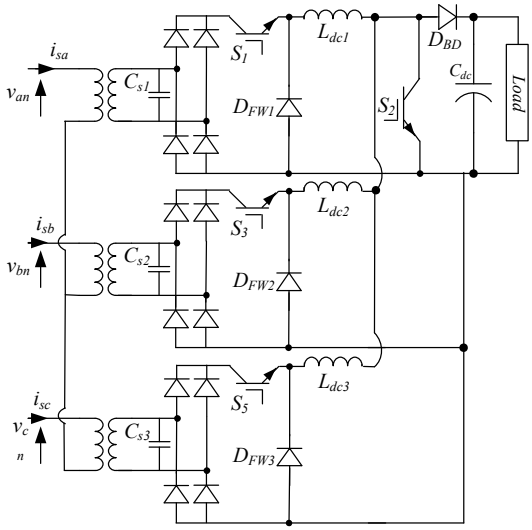
$$i_{r\_rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} \frac{\delta^4 T^2 V_m^2 \sin^2(\omega t)}{4L^2} d\omega t} = \frac{\delta^2 T V_m}{2\sqrt{2}L} \quad (22)$$

If the proposed converter is connected to a fixed dc-bus voltage, the power balance equation ($P_{dc}$=$P_{ac}$) can be used to derive the relationship between the ac side current and dc current and switches duty cycles as follow:

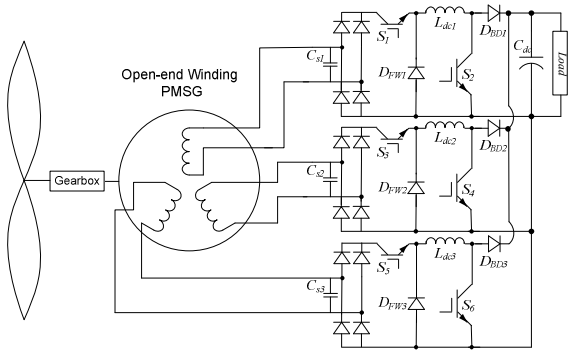
$$3 i_r v_s \cos(\theta) = V_{dc} I_{dc} \quad (23)$$

Since the proposed converter input currents are in phase with the supply voltages, $\theta$=0, by substituting equation (22) in (23), yields:

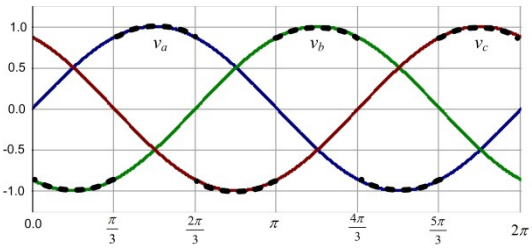
$$I_{dc} = \frac{3}{4}\frac{\delta^2 T V_m^2}{L V_{dc}} \quad (24)$$



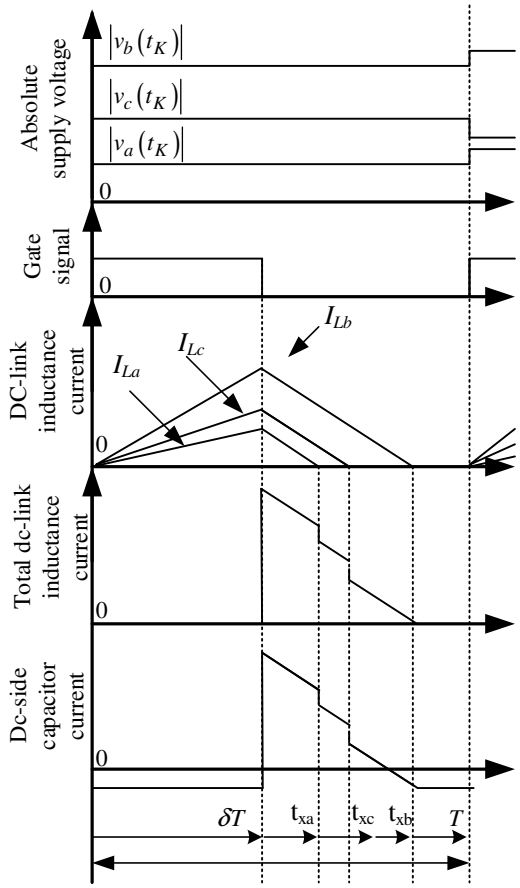

A




B




C




D

Fig. 3. Three parallel connected single-phase ac-dc buck-boost converter topology ‘B’ and ‘C’.
(a) Topology ‘B’ with three supply sets and one load set feeding a dc load; (b) topology ‘C’ with three supply side sets and three load-side sets; (c) depiction of three-phase ac side voltages; and (d) current waveforms during one switching period, considering time interval $0 \leq \omega t \leq 60°$.

## 5 Simulation results

This section assesses the viability of topologies ‘A’ and ‘C’, assuming their ac sides are connected to PMSG based variable speed WECS with open ended windings. To examine the steady-state and dynamic performance of the topologies ‘A’ and ‘C’, the wind speed is assumed to vary from 6.0m/s, 12.5m/s and 10 m/s, with each wind speed is applied for 5s time interval. The system simulation parameters are listed in Table 1, while of the proposed converters’ parameters are shown in Table 2.

Throughout this paper (simulations and experiments), the dc-side inductances are designed such that at rated power the proposed converter operates at the boundary between CCM and DCM (trade-offs between size and weight of passive elements and current stresses in the semiconductor switches). However, to avoid the unintended operation in CCM, it is a good practice to consider a countermeasure at design stage such as a safety margin, which can be realized by deliberate underestimation of the dc-side inductance by small margin $\Delta L_{dc}$ to guarantee operation in DCM over the full operating range.

Table 1 Wind turbine and PMSG parameters.

| Wind turbine parameters | |
|---|---|
| Rated power | 1.1MW |
| Rated wind speed | 12.5m/s |
| Cut-in wind speed | 4m/s |
| Cut-out wind speed | 25m/s |
| Rotor Radius | 24m |
| Rotor area | 1808m$^2$ |
| Gearbox ratio | 1:10 |
| **PMSG Parameters** | |
| Rated power | 1.1 MVA |
| Rated speed | 380 rpm |
| Rated voltage | 3.3 kV |
| Direct-axis inductance | 5.5 mH |
| Quadrature-axis inductance | 5.5 mH |
| Mutual inductance coefficient | 1 mH |
| Number of poles | 6 |

Table 2 Simulation parameters of the ac-dc buck-boost converters (topology 'A', and 'C').

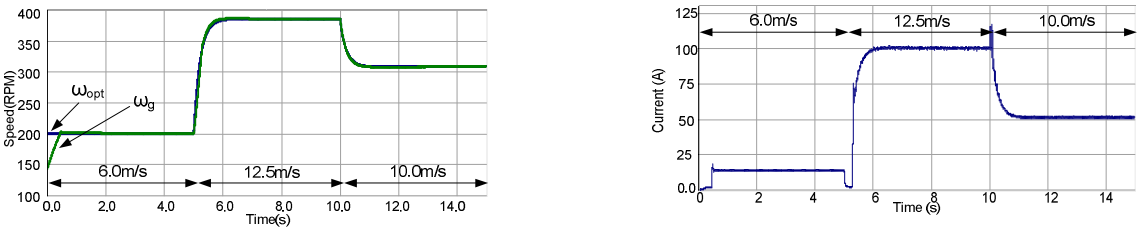
| | Three series connected single-phase ac-dc buck-boost converter | Three parallel connected single-phase ac-dc buck-boost converter |
|---|---|---|
| Rated power | 1MW | 1MW |
| Supply voltage | 3.3kV L-L | 3.3kV L-L |
| Supply Frequency | 50Hz | 50Hz |
| Switching frequency | 2.4kHz | 2.4kHz |
| Transformer rated power | Three single-phase transformers 0.35MVA | Three single-phase transformers 0.35MVA |
| Transformer rated voltage | Three single-phase transformers 1.9/1.9kV | Three single-phase transformers 1.9/1.9kV |
| AC-side C-filter | 3× 50μF(170kVAr) | 3× 50μF(170kVAr) |
| DC-side L-filter | 3× 700μH | 3× 950μH |
| DC-side C-filter | 3× 1000 μF | 1000μF |

### 5.1 Topology 'A' of the proposed ac-dc buck-boost converter

The simulations waveforms for the topology 'A' in Fig. 2(a) when its dc side is connected to 10 kV dc bus and ac side to PMSG are presented in Fig. 4 and Fig. 5.

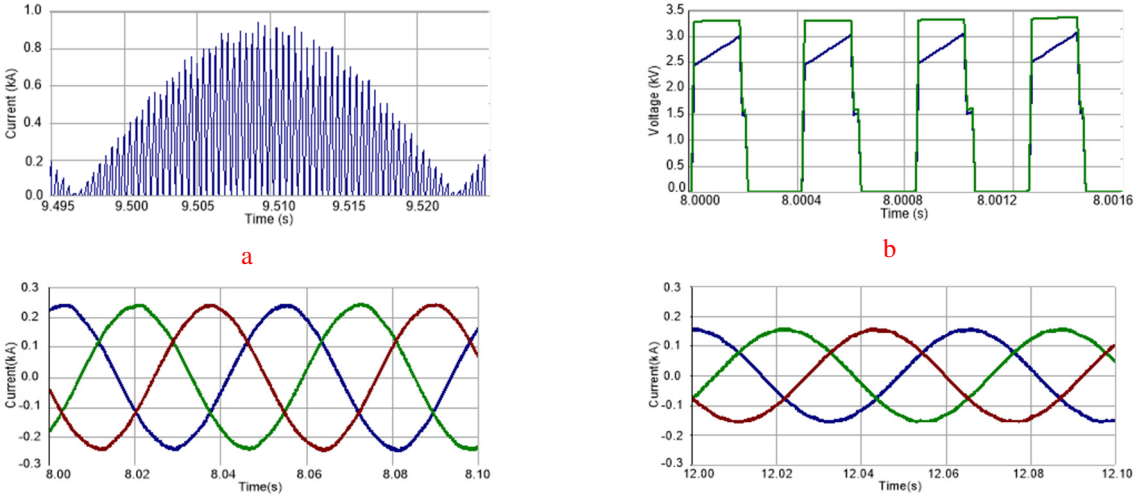
Fig. 4 (a) shows that with the basic controller in Fig. 2 (c), the generator speed tracks the optimal speed as wind speed varies as outlined earlier. Also, the dc bus current increases and decreases as the power varies with the wind speed, see Fig. 4 (b).

The plots for the dc side inductor current in Fig. 5(a) show that the topology 'A' converter operates at boundary between CCM and DCM, and this confirms validity of the theoretical equation (3). The traces for the voltage stresses on the power electronic switches in Fig. 5(b) indicate that the voltage stress across the switch '$S_1$' is determined by the peak of the ac voltage that the PMSG imposes at the ac terminal of the diode bridge, particularly, the voltage across the ac filter capacitor, while the voltage stress across the switch '$S_2$' represents one third of the dc bus voltage as articulated earlier. Fig. 5(c) and (d) display the three-phase ac currents being drawn from the PMSG at two wind speeds, 12.5m/s and 10m/s respectively. These plots show that the three-phase currents the topology 'A' draws from the PMSG remain sinusoidal as wind speed and ac side frequency vary.




a b

Fig. 4. Simulation waveforms that illustrate the basic performance of topology 'A' with emphasis on WECS application a) Generator speed superimposed on the optimal speed, and (b) dc-bus current.



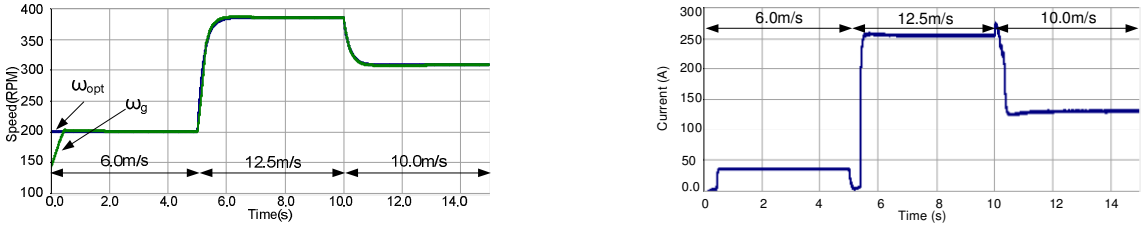

a b c d

Fig. 5. Simulation waveforms that illustrate the basic performance of topology 'A' with focus on current and voltage stresses and quality of ac side current waveforms

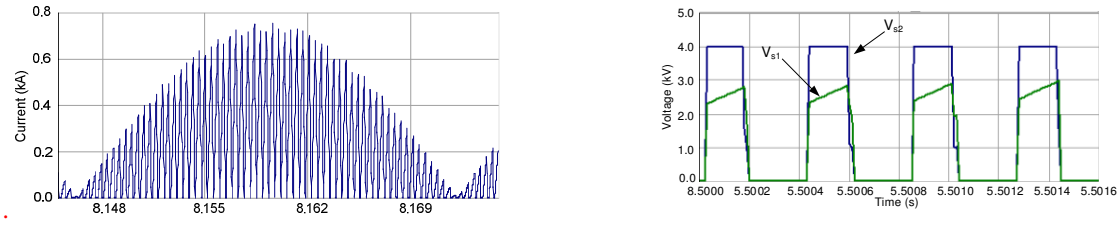
(a) dc-link inductor current, b) voltage stresses across the switches $S_1$ and $S_2$, (c) generator current at 12.5m/s wind speed, and (d) generator current at 10m/s wind speed.

### 5.2 Topology 'C' of the proposed ac-dc buck-boost converter

The ac side of the topology 'C' converter shown in Fig. 3(b) is connected to a variable speed WECS and its dc output is connected to a 4kV dc bus, and simulation waveforms for this illustrative case are summarised in Fig. 6. Fig. 6(a) shows that the manipulation of the topology 'C' using the same basic control employed with topology 'A' has allowed the wind generator to track the optimal speed as wind speed varies. Fig. 6(b) shows the dc bus (load) current increases and decreases as the generated power varies with the wind speed. The dc-side inductor current in Fig. 6(c) indicates that the topology 'C' operates in the boundary of CCM and DCM as topology 'A', and this confirms the validity of equation (21) which defines the critical value of the dc side inductance that ensures operation at the boundary of CCM and DCM. The traces for the voltage stress on the power electronics switches in Fig. 6(d) indicate that maximum voltage stress on switch '$S_1$' of the topology 'C' is the same as that of the topology 'A' and it is equal to the peak of the phase voltage that the PMSG imposes at the converter ac side, while the voltage across the switch '$S_2$' of topology 'C' is equal to the dc bus voltage. This indicates the suitability of topology 'C' for high-power applications with relatively low dc voltage and high current, benefiting from the current sharing of the sub-converters.




a b




c d

Fig. 6. Simulation waveforms that illustrate the basic performance of topology 'C' in WECS systems. (a) generator speed and optimal speed, (b) dc-bus current, (c) dc-link inductor current, (d) voltage stress across the switches $S_1$ and $S_2$.

## 5.2 Approximate semiconductor loss estimates

As stated earlier, the choice of operation of the proposed converter at the boundary between CCM and DCM is driven by the trade-offs between size and weight of passive elements, and current stresses in the semiconductor devices. Since the average current when converter operates in DCM is the same as that in CCM for the same power transfer, the conduction losses are expected to be the same. However, the total switching loss when converter operates in DCM may differ from that of the CCM for the same power transfer. This is because in the DCM the switching devices such as $S_1$ and $S_2$ experience significantly high currents at turn-off corresponding to the peaks of the dc side inductor currents, and zero current at turn-on. In contrary, in CCM, the switching devices $S_1$ and $S_2$ experience lower but non-zero current at both turn-on and turn-off, thus, incur switching losses at turn-on and turn-off.

For quantification of the potential sacrifice in the efficiency of the proposed converters due to the aforementioned, the efficiencies of 1MW converter based on topology 'C' with 4kV dc link voltage when it is operating in CCM and at the boundary between CCM and DCM are calculated. In efficiency calculations, the switch $S_1$ is formed by one 4.5kV, 800A IGBT (T0800TB45E) which is corresponding to 60% device utilization, $S_2$ is formed by series connection of two 4.5kV, 800A IGBT (T0800TB45E) to be able to block the full dc link voltage (42% device utilization), and the diodes $D_{FW}$ and $D_{BD}$ are formed by one and two series connected 4.5kV, 765A fast recovery diodes (E0660NC45C) respectively. The on-state resistance and threshold voltage drop of the 4.5kV IGBT and diodes above are:

IGBT (T0800TB45E): $R_T$=2.74mΩ and $V_{T0}$=1.71V.

Diode (E0660NC45C): $R_D$=2.236 mΩ and $V_{D0}$=2.0V.

The switching loss per IGBT is calculated based on linear approximation of the turn-off and turn-on energy losses per pulse as:

Turn-off energy ($E_{off}$): $E_{off} = 1.2 + 0.006(I_{off} - 200)$ (25)

Turn-on energy ($E_{on}$): $E_{on} = 1.05 + 0.005(I_{on} - 200)$ (26)

With the assumption of 2.4kHz switching frequency, negligence of diodes recovery losses, and the fast recovery diodes are employed at both $D_{FW}$ and $D_{BD}$ and in the diode rectifier bridge, the on-state (conduction) and switching losses and approximate efficiencies of topology 'C' are computed as displayed in Table 3 and Table 4 for DCM and CCM operation respectively. In this paper, the on-state and switching losses are computed using the methods described in [41-43].

Table 3 and Table 4 show that the computed semiconductor losses when 1MWconverter based on topology 'C' operates in DCM differ marginally from that obtained with CCM. The marginal differences observed in the semiconductor losses and efficiencies of the topology 'C' when it operates in DCM and CCM could be explained with the aid of the plots in Fig. 7 and Fig. 8 that display the dc load current superimposed on the dc inductor current and current in the switch $S_1$. As anticipated, for the same dc load current and power transfer, the currents in the dc inductor and switch S1 when topology 'C' operates in DCM are higher than when it is operating in CCM, see Fig. 7 and Fig. 8. However, the DCM exhibits attractive feature of near zero current switching (ZCS) at turn-on of $S_1$ and $S_2$, which entails practically zero switching losses at $S_1$ and $S_2$ during turn-on. In contrary, although CCM exhibits lower peak currents, the switches $S_1$ and $S_2$ incur switching losses at turn-on and turn-off.

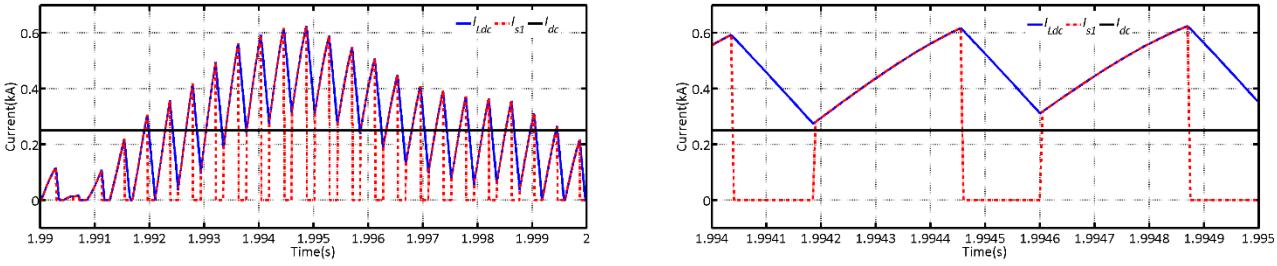
Notice that both DCM and CCM incur identical on-state losses for the same power transfer as the average currents in the didoes and switches $S_1$ and $S_2$ are the same as that in CCM.

Table 3: Approximate efficiency of topology ‘C’ when it is rated at 1MW and operates in DCM and at the boundary between CCM and DCM at rated power

| | Semiconductor losses | | | |
|---|---|---|---|---|
| Operating condition | Conduction | Switching | Total semiconductor loss | Efficiency |
| P=0.64MW | 5.4kW | 16.2kW | 21.6kW | 96.63% |
| P=1MW | 8.6 | 25.9 | 34.5kW | 96.55% |

Table 4: Approximate efficiency of topology ‘C’ when it is rated at 1MW and operates in CCM

| | Semiconductor losses | | | |
|---|---|---|---|---|
| Operating condition | Conduction | Switching | Total semiconductor loss | Efficiency |
| P=0.64MW | 5.4kW | 14.3kW | 19.7kW | 96.9% |
| P=1MW | 8.6 | 24.3 | 32.9kW | 96.7% |

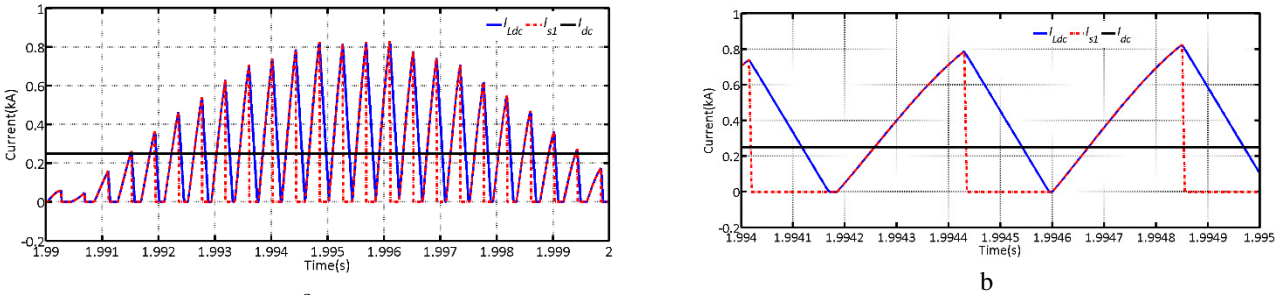



a b

Fig. 7: Simulation waveforms when topology ‘C’ is applied to high-power applications and operates in CCM.

(a) Inductor current superimposed on the dc link current and current of the switch $S_1$.

(b) Detailed view of the inductor currents superimposed on the dc link current and current of the switch $S_1$.




a b

Fig. 8: Simulation waveforms when topology ‘C’ is applied to high-power applications and operates in DCM.

(a) Inductor current superimposed on the dc link current and current of the switch $S_1$.

(b) Detailed view of the inductor currents superimposed on the dc link current and current of the switch $S_1$.

For completeness, detailed semiconductor losses and efficiencies of topology A in DCM and CCM are presented in Table 5 and Table 6. The semiconductor losses of the topology A are computed at two operating points of 640kW and 1MW when it generates dc voltage of 12kV, in which each sub-converter contributes 4kV. The dc output voltage of 12kV (4kV per sub-converter) is selected to ensure that the switching devices’ utilizations in topology A remain the same as that of the topology C. In this way, the same expressions for the turn-on and turn-off energies in (25) and (26) can be used for calculations of switching losses of topology A. The results in Table 5 and Table 6 show that the topology A exhibits the lowest semiconductor losses (highest efficiencies) when it operates in DCM, while it shows marginally the highest semiconductor losses (lowest efficiencies) when it operates in CCM. The main differences observed are: the topology A incurs the lowest and highest switching losses in DCM and CCM.

Table 5: Approximate efficiency of topology ‘A’ when it is rated at 1MW and operates in DCM and at the boundary between CCM and DCM at rated power

| | Semiconductor losses | | | |
|---|---|---|---|---|
| Operating condition | Conduction | Switching | Total semiconductor loss | Efficiency |
| P=0.64MW | 5.4kW | 11.7kW | 17.1kW | 97.32% |
| P=1MW | 9.95kW | 16.2kW | 26.15kW | 97.38% |

Table 6: Approximate efficiency of topology ‘A’ when it is rated at 1MW and operates in CCM

| | Semiconductor losses | | | |
|---|---|---|---|---|
| Operating condition | Conduction | Switching | Total semiconductor loss | Efficiency |
| P=0.64MW | 5.6kW | 21.2kW | 26.8kW | 95.8% |
| P=1MW | 9.95kW | 30.8kW | 40.75kW | 95.9% |

5.3 Proposed ac-dc buck-boost converter as a front-end of grid tied neutral-point clamped voltage source converter

This section uses series type ac-dc converter, topology ‘A’, as an example to demonstrate the capacity of any of the proposed ac-dc buck-boost converters to operate as a front-end (generator side) converter of a back-to-back system with a voltage or current source converters as grid side converter. However, three-level neutral-point clamped voltage source converter (3L-NPC-VSC) is adopted in this illustration. The simulation parameters of the topology ‘A’ displayed in Table 2 are adopted in this illustrative example. The rated parameters of the 3L-NPC-VSC are: rated dc link voltage is 10kV; rated ac voltage (line-to-line) is 6.6kV; and interfacing transformer of the grid side converter is rated at 1MVA and 6.6kV/6.6kV with 0.1 pu leakage reactance. The ac grid is represented by a 6.6kV voltage source with SCR=10 and X/R=10 and 50Hz nominal frequency. The 3L-NPC-VSC that acts as grid side converter in Fig. 9 regulates the dc link voltage of the back-to-back system at 10kV and reactive power exchange with the ac grid at zero, while the front-end buck-boost ac-dc converter tracks the maximum power point as illustrated earlier.

Fig. 10 presents selected simulation waveforms when the topology ‘A’ converter which acts as a front-end converter of the back-to-back energy conversion system displayed in Fig. 9 tracks the maximum power point as wind speed varies as shown Fig. 10(a) and (b). The plot in Fig. 10(c) shows that the grid side 3L-NPC-VSC manages to regulate the dc link voltage at 10kV, with small and short duration drifts at the instances active power changes. Fig. 10(d) and (e) show that the dc inductor current and voltage stresses across the switches S1 and S2 remain similar to those presented earlier when the proposed ac-dc converters were connected to stiff dc grid, and in line with the expectations as envisioned initially during the inception of the proposed converters. The traces in Fig. 10(f), (g) and (h) indicate that both the front and back end converters present high quality sinusoidal currents to the wind generators and ac grids.

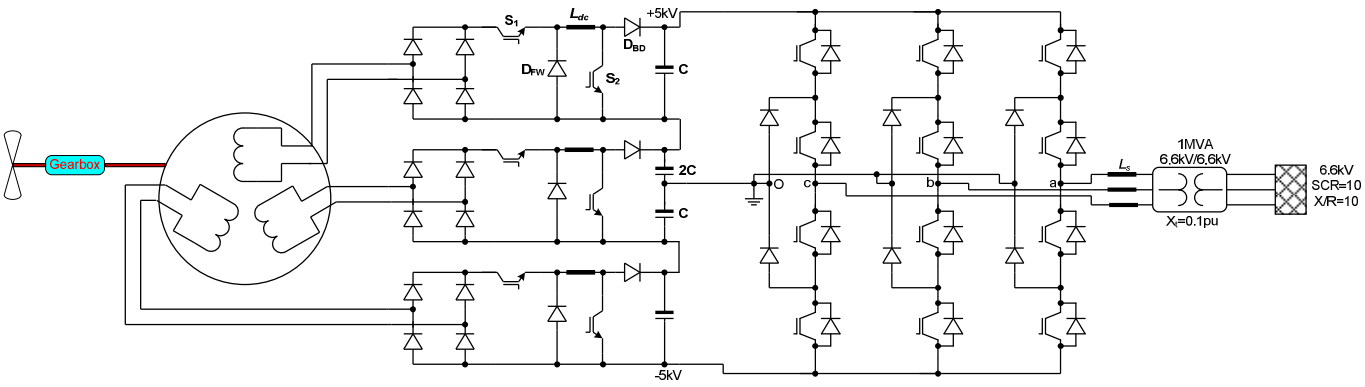
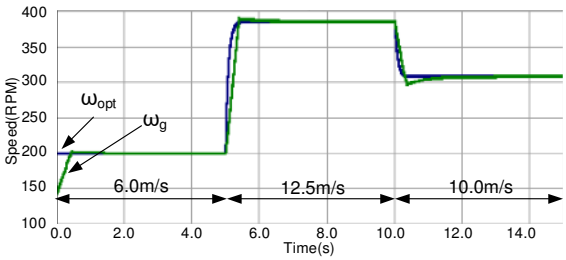
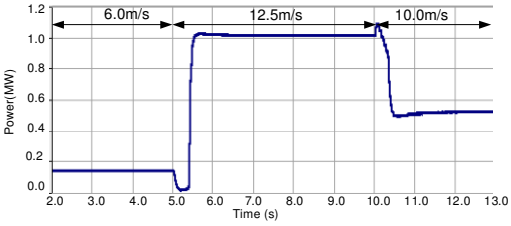


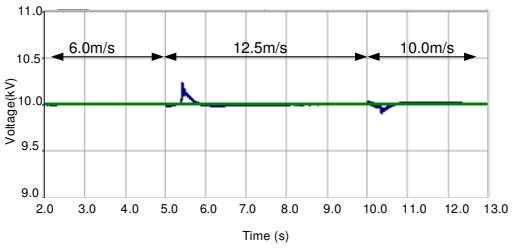

Fig. 9: Back-to-back arrangement in which the topology ‘A’ of the proposed ac-dc buck-boost converters interfaces the wind generator into the dc link of the grid side 3L-NPC -VSC



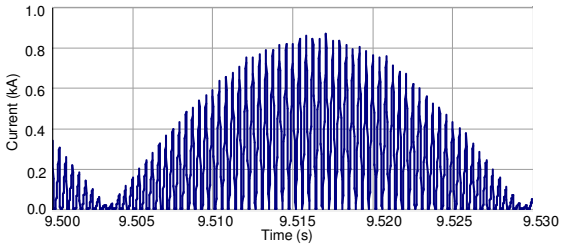

a) Generator speed superimposed on the optimal reference speed



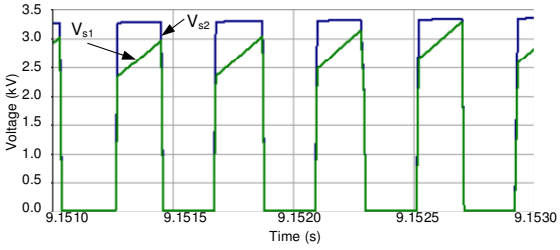

b) Active power that the 3L-NPC-VSC injects into ac grid



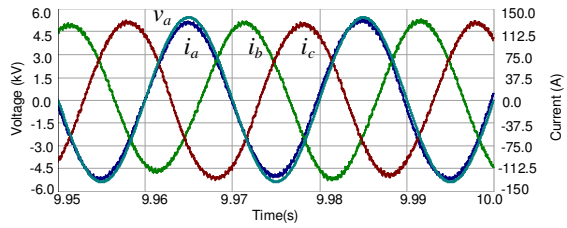

c) 3L-NPC-VSC input dc voltage.



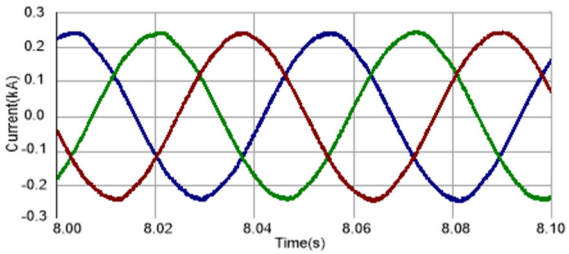

d) Sample current in the dc inductor of the upper sub-converter, measured when wind speed is 12.5 m/s



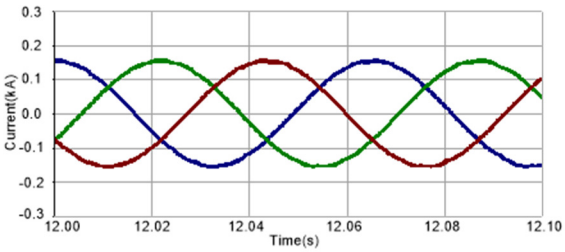

e) Voltage stresses across the semicondcutor swicthes $S_1$ and $S_2$ measured during wind speed is 12.5m/s




f) Three-phase currents that the 3L-NPC-VSC injects into ac grid superimposed on phase 'a' voltage at point of common coupling




g) Three-phase currents the topology 'A' of the proposed ac-dc buck-boost draws from the wind generator when wind speed is 12.5m/s.




h) Three-phase currents the topology 'A' of the proposed ac-dc buck-boost draws from the wind generator when wind speed is 10m/s.

Fig. 10: Simulation waveforms illustrate the performance of the proposed ac-dc buck-boost as a front-end converter that interfaces the wind generation into the dc link of the grid side (back-end) 3L-NPC-VSC

5.4 High-level comparison of the proposed ac-dc buck-boost converter and other proposed three-phase ac-dc buck-boost converter.

Table 7 presents high a level comparison of the proposed converters and similar alternative topologies from the open literature. All the selected converters have sinusoidal input currents with nearly unity power factor, and with operating frequency can be reduced for operation at high-power and medium-voltage applications. Observe from Table 7 that converter in [44] have the lowest number of semiconductor devices, and capable of operating low switching frequencies such as 1.2kHz. However, it suffers from high voltage stress on some of the semiconductor devices, and this represents a major limitation in high-power medium-voltage applications. The converter in [25] operates under input capacitor discontinuous voltage mode (DVM), and this makes the ac-side capacitive filters to exacerbate voltage stresses on the dc side semiconductor devices. The ac-dc buck-boost converter in [45] offers zero current switching (ZCS) by using quasi-resonant (QR); but operation at variable switching frequency may

limit its applications in high-power medium-voltage. The topology in [30] places excessive number of semiconductor devices in conduction path, which will decrease the overall system efficacy. The topology in [46] operates under DCM which increases the current stresses in the semiconductor devices, and also its switching devices suffer from high voltage stresses. From this comparison it can be seen that each ac-dc buck-boost converter topology has its strong and weak points, and this offers opportunity for design compromise.

Table 7 : High-level comparison between topologies A and C and alternative ac/dc buck-boost converters

| | Topology 'A' | Topology 'C' | Proposal in [44] | Proposal in [25] | Proposal in [45] | Proposal in [30] | Proposal in [46] |
|---|---|---|---|---|---|---|---|
| Operating mode | DCM | DCM | CCM | DVM | QR | CCM | DCM |
| No. of semiconductor devices | 18 Diodes 6 Switches | 18 Diodes 6 Switches | 7 Diodes 1 Switches | 8 Diodes 2 Switches | 8 Diodes 2 Switches | 24 Diodes 6 Switches | 16 Diodes 1 Switches |
| No. of dc side passive compoents | 3 Inductors 3 Capacitors | 3 Inductors 1 Capacitors | Indicate:1 1 Capacitors | Indicate:1 1 Capacitors | 3 Inductors 3 Capacitors | 6 Inductors 1 Capacitors | 6 Inductors 2 Capacitors |
| Voltage stress in the switching devices | low | Low | High | High | High | Low | High |
| Current stress in the switching devices | High | Medium | Low | Low | High | Low | High |
| Operating switching frequency | 2.4kHz | 2.4kHz | 1.2kHz | 25kHz | 20 to 55kHz | 40kHz | 100kHz |

## 6 Experimental results

This section uses 1.5kW prototypes of the topologies 'A' and 'C' to experimentally confirm their practicality. The parameters of these experimental test rigs are list in Table 8 and Table 9. Because of the absence of PMSG, the ac side of both topologies 'A' and 'C' are connected to a 50Hz ac supply instead of PMSG, with their dc side were connected to resistive loads. Fig. 11 shows the picture of the experimental test rig of the proposed converter when it is configured as topology 'C'.

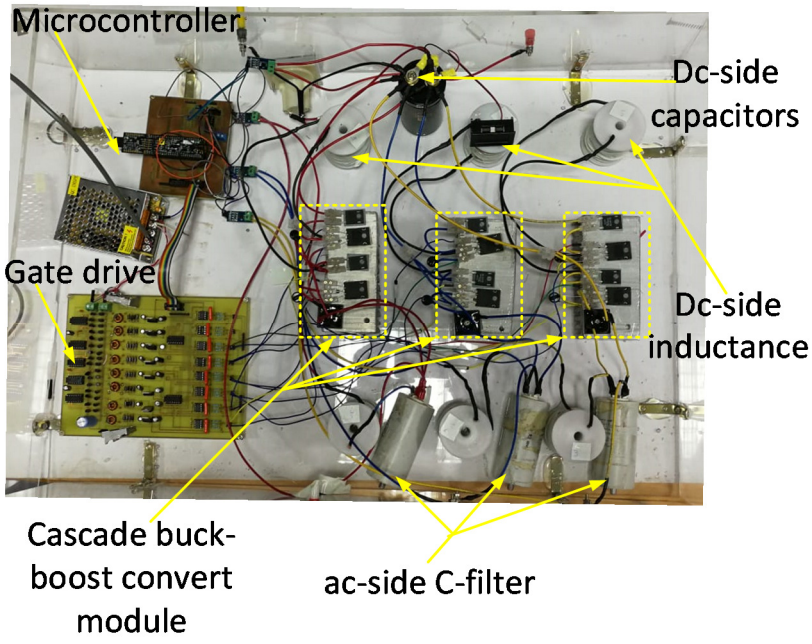



Fig. 11: Picture of the experimental test rig

Table 8: additional experimental details.

| | |
|---|---|
| DC inductors | Air core type |
| Multi-winding transformer | 8kVA, 440V/220V (rated line-to-line) |

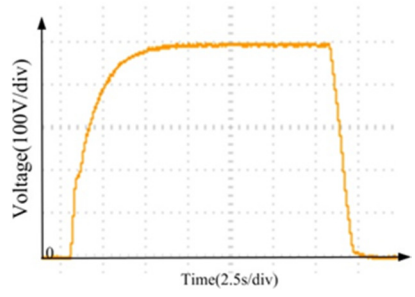
| | |
|---|---|
| Switches $S_1$ and $S_2$ | 1200V, 30A IGBT (IKW15T120FKSA1) |
| Diode rectifier bridge | 1000V, 50A bridge GBPC3504 |
| Diodes DFW and DBD | 600V, 30A ultra-fast recovery diode RURG3060 |

Table 9 Experimental setup parameters

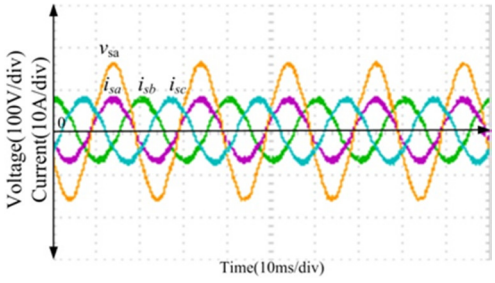
| Parameter | Topology 'A' | Topology 'C' |
|---|---|---|
| Supply voltage | $110V_{L\_N}$ | $110V_{L\_N}$ |
| Converter rated power | 1.5kW | 1.5kW |
| Converter rated switching frequency | 2.4kHz | 2.4kHz |
| Transformer rated power | 8kVA | 8kVA |
| Transformer rated voltage | $440/220V_{L\text{-}L}$ | $440/220V_{L\text{-}L}$ |
| ac-side capacitance | 50μF | 50μF |
| dc-side inductance | 560 μH | 1.2mH |
| dc-side capacitance | Three 2200 μF | 2200 μF |
| Load resistance | 180Ω | 90Ω |

6.1 Three series connected single-phase ac-dc buck-boost converter (Topology 'A)

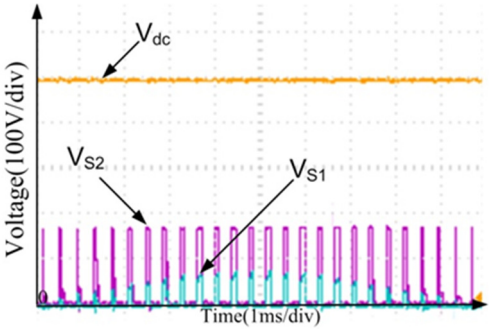
The experimental results of topology 'A' are shown in Fig. 12 . Fig. 12(a) shows that the topology 'A' offers controlled dc voltage ramp-up from 0 to 500V, and ramp-down from 500V to 0, which resemble the boost and buck capabilities, and stable dc output voltage. The plots in Fig. 12(b) shows that the topology 'A' injects sinusoidal current waveforms into ac side, with unity power factor. Samples of the voltage waveforms across the switches '$S_1$' and '$S_2$' of the upper module or sub-converter in Fig. 12(c) and (d) confirm the claim of reduced voltage stress on the self-commutated semiconductor switches. The maximum voltage stress on the switch '$S_1$' is equal to the peak of the supply voltage between the line to neutral (55 √2=77V). On the other hand, the maximum voltage stress across the switch '$S_2$' is equal to $⅓V_{dc}$ ($500V/3=166V$). The sample trace of the current in the dc-side inductor in Fig. 12(e) confirms that at rated power (1.5kW), the topology 'A' operates at the boundaries between DCM and CCM as articulated during sizing of the passive elements and simulation section. Additionally, the plot in Fig. 12(e) shows that the high boost ratio of the topology 'A' increases the current stresses in the switching devices of the individual sub-converters, and this must be considered as part of engineering trade-offs.



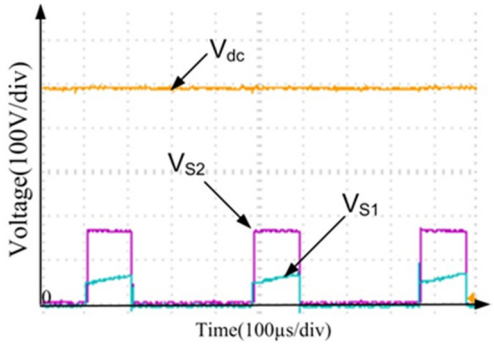

a



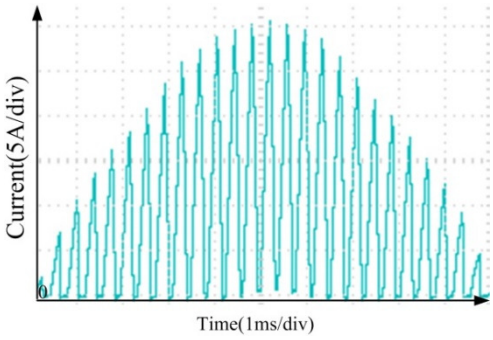

b




c



d

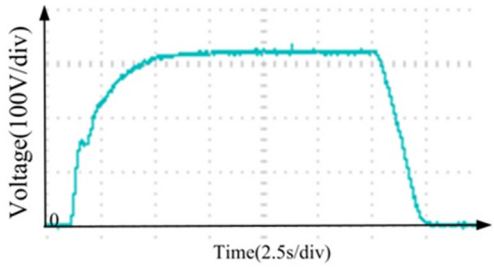



e

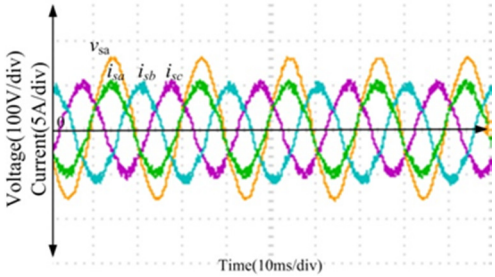
Fig. 12. Experimental results that illustrate the performance of topology 'A'.
(a) dc output voltage, (b) phase 'a' voltage and three-phase supply currents, (c) voltage stresses across the switches $S_1$ and $S_2$ overlaid on the dc-output voltage, (d) detailed view of the voltage stresses across the switches $S_1$ and $S_2$, and (e) dc-side inductor current

6.2 6.2 Three parallel connected single-phase ac-dc buck-boost converter (Topology 'C')

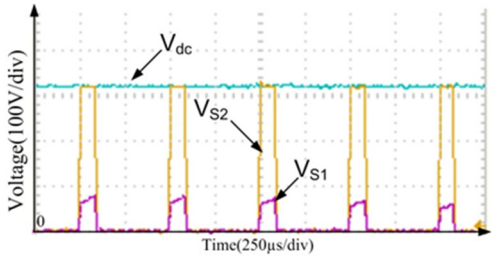
This section presents experimental verification of topology 'C' and its parameters are listed in Table 9. The experimental results of the topology 'C' are shown in *Fig. 13*. The trace for the dc output voltage in *Fig. 13* (a) shows that the topology 'C' offers boost and buck capabilities, which are demonstrated with the gradual and controlled dc output voltage ramp up from 0 to 320V and ramped down from 320V to 0. *Fig. 13*(b) shows that the topology 'C' injects sinusoidal current waveforms into ac side, with unity power factor. The sample voltage stress across the switch $S_1$ and $S_2$ in *Fig. 13*(c) shows that the switch $S_1$ blocks maximum voltage stress equal to the peak of the supply voltage ($55\sqrt{2}$=77V), while the switch $S_2$ experiences voltage stress equal to the dc output dc voltage. The current waveform in the dc side inductor of the topology 'C' in *Fig. 13*(d) confirms that it operates at the boundaries between the CCM and DCM. The plots for current waveforms in blocking diodes of the three sub-converters ($I_{BD1}$, $I_{BD2}$ and $I_{BD3}$) and in the dc-side capacitor current ($I_{C\_dc}$), zoomed over one switching period are shown in *Fig. 13* (e). These plots confirm that each sub-converter contributes to the total load current and to charging of the dc-side capacitors through the blocking diodes of the sub-converters, with the dc-side capacitor current equals to $I_{BD1}+ I_{BD2}+ I_{BD3}-I_{dc,}$ as discussed above in section 4.



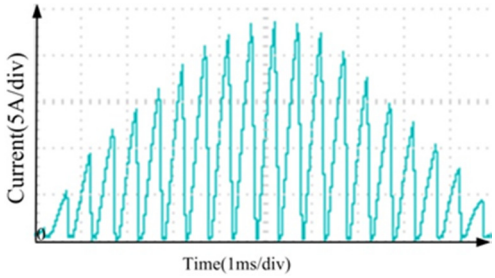

a



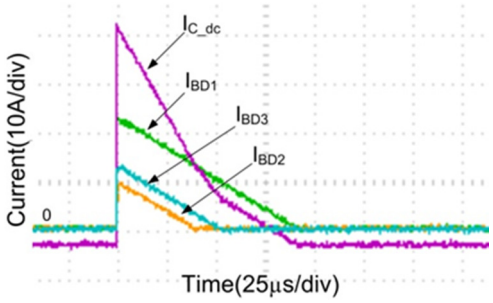

b




c




d




e

Fig. 13. Experimental results that illustrate the performance of topology 'C'.
(a) dc output voltage, (b) three-phase supply currents and phase 'a' voltage, (c) voltage stresses across the switches $S_1$ and $S_2$ superimposed on the dc-output voltage, (d) dc-side inductor current, and (e) blocking diodes' currents ($I_{BD1}$, $I_{BD2}$ and $I_{BD3}$) overlaid on the dc-side capacitor current ($I_{C\_dc}$).

### 6.3 Experimental estimates of power losses

The overall efficiencies of the topologies 'A' and 'C' are calculated by subtracting the dc power ($P_{dc}$) at load terminal from the three-phase powers($P_{ac}$) measured at point of common coupling in ac grid side, i.e., $\eta = P_{dc}/P_{ac} \times 100\%$. So, the calculated efficiency includes the transformer losses and losses in the parasitic resistances of dc inductors and equivalent series resistance of the capacitors.

It has been established that both topologies A and C have almost the same efficiencies of 76.5% and 89.9% at two different operating points, 1137W and 1388W output powers respectively. The relatively low experimental efficiencies obtained are due to the loss calculation method that includes additional losses besides the semiconductor losses (such as the losses in the interfacing transformer, equivalent series resistance of the capacitors and inductors); low utilization of the semiconductor devices (as the experimental operating points are significantly far from the devices rated currents and voltages, especially, in topology A ); and the use of low cost rectifier diodes at the diode bridges. In effort to justify that the low efficiencies obtained from the scaled down experimental test rigs are due to factors described above, the estimates of semiconductor losses based on scaled-down simulations of topologies A and B, in which the semiconductor parameters are extracted from the datasheets of the devices employed in the experimental test-rig are given as follows (losses in capacitors' ESRs and inductors are not considered):

**Topology A**: The total semiconductor loss of the topology A when it outputs 1388W at 500V dc is 201.75W, of which 170W on-state losses and 31.75W switching losses. Under this operating condition, the computed efficiency of topology A is 87.45%.

**Topology C**: The total semiconductor loss of the topology C when it outputs 1137W at 320V dc is 157.6W, of which 131W on-state losses and 25.8W switching losses. Under this operating condition, the estimated efficiency of topology C is 87.8%.

The above experimental and simulation results confirm that the efficiencies of the scaled down systems tend to be much lower than that of the full-scale systems. Also, these results show that the experimental efficiency of the scaled down version of topology 'A' differs significantly from that obtained using simulation, while the difference is relatively small between simulation and experimental efficiencies of the scaled down versions of the topology C. The significant differences observed between simulation and experimental efficiencies of topology 'A' could be attributed to the relative contribution of the ESRs of the capacitors and internal resistances of the dc inductances to the overall power losses of the experimental test rig (recall that the current paths within the internal circuit of the topology A differ from that of the topology C).

## 7 Conclusion

This paper has proposed three topologies for three-phase ac-dc buck-boost converters. Among the proposed converters, topologies 'A' and 'C' offer a buck-boost capability in single-stage, with reduced voltage stresses on the power electronics switches, while injecting sinusoidal currents into ac side. DCM operation of the proposed converters were preferred over CCM to reduce the size and weight of energy storage elements such as capacitors and inductors. Theoretical analysis and discussions of the three proposed converter topologies, and simulations and experimental results of topologies 'A' and 'C' reveal that the converter topology 'A' is well-suited for medium-voltage operation as its semiconductor switches withstand lower voltage stresses than topology 'C'. The topology 'C' is well suited for high-power applications with relative low dc voltages and high dc currents as the load side sets are exposed to lower current stresses than those of topology 'A' (lower ends of medium-voltage). Therefore, it can be concluded that the proposed ac-dc buck-boost converters offer promising design trade-offs for medium-voltage wind energy conversion systems.

## 8 Acknowledgments

This project was funded by the Deanship of Scientific Research (DSR) at King Abdulaziz University, Jeddah, under grant no. (**RG-39-135-23**). The authors, therefore, acknowledge with thanks DSR For technical and financial support.

## 9 References

[1] I. Abdelsalam, G. P. Adam, D. Holliday, and B. W. Williams, "Modified back-to-back current source converter and its application to wind energy conversion systems," *IET Power Electronics,* vol. 8, no. 1, pp. 103-111, 2014.

[2] M. I. Marei, I. Abdallah, and H. Ashour, "Transformerless uninterruptible power supply with reduced power device count," *Electric Power Components and Systems,* vol. 39, no. 11, pp. 1097-1116, 2011.

[3] U. R. Reddy and B. L. Narasimharaju, "Single-stage electrolytic capacitor less non-inverting buck-boost PFC based AC-DC ripple free LED driver," *IET Power Electronics,* vol. 10, no. 1, pp. 38-46, 2017.

[4] D. Wu, G. Calderon-Lopez, and A. J. Forsyth, "Discontinuous conduction/current mode analysis of dual interleaved buck and boost converters with interphase transformer," *IET Power Electronics,* vol. 9, no. 1, pp. 31-41, 2016.

[5] Y. Wang, S. Zhang, Y. Guan, X. Liu, and D. Xu, "Single-stage QR AC/DC converter based on buck-boost and flyback circuits," *IET Power Electronics,* vol. 10, no. 1, pp. 103-111, 2017.

[6] M. H. Rashid, *Power Electronics: Circuits, Devices, and Applications*. Pearson/Prentice Hall, 2004.

[7] C. L. Shen and P. C. Chiu, "Buck-boost-flyback integrated converter with single switch to achieve high voltage gain for PV or fuel-cell applications," *IET Power Electronics,* vol. 9, no. 6, pp. 1228-1237, 2016.

[8] D. Debnath and K. Chatterjee, "Maximising power yield in a transformerless single-phase grid connected inverter servicing two separate photovoltaic panels," *IET Renewable Power Generation,* vol. 10, no. 8, pp. 1087-1095, 2016.

[9] X. Zhou, J. Xu, X. Chen, and S. Zhong, "Soft-switching step-up/down DC/DC converter with bipolar outputs," *Electronics Letters,* vol. 52, no. 16, pp. 1404-1406, 2016.

[10] S. Li, K. W. E. Cheng, Y. Ye, and Z. Shi, "Wide input and wide output topology analysis for tapped-inductor converters with consideration of parasitic elements," *IET Power Electronics,* vol. 9, no. 9, pp. 1952-1961, 2016.

[11] A. Darwish, A. Massoud, D. Holliday, S. Ahmed, and B. Williams, "Generation, performance evaluation and control design of single-phase differential-mode buck-boost current-source inverters," *IET Renewable Power Generation,* vol. 10, no. 7, pp. 916-927, 2016.

[12] T. Sreekanth, N. Lakshminarasamma, and M. K. Mishra, "Coupled inductor-based single-stage high gain DC/AC buck-boost inverter," *IET Power Electronics,* vol. 9, no. 8, pp. 1590-1599, 2016.

[13] M. Esteki, E. Adib, H. Farzanehfard, and S. A. Arshadi, "Auxiliary circuit for zero-voltage-transition interleaved pulse-width modulation buck converter," *IET Power Electronics,* vol. 9, no. 3, pp. 568-575, 2016.

[14] M. He, F. Zhang, J. Xu, P. Yang, and T. Yan, "High-efficiency two-switch tri-state buck-boost power factor correction converter with fast dynamic response and low-inductor current ripple," *IET Power Electronics,* vol. 6, no. 8, pp. 1544-1554, 2013.

[15] C. Urayai and G. A. J. Amaratunga, "Electronic load interface for improving PV dual-converter system operational margin," *IET Renewable Power Generation,* vol. 7, no. 1, pp. 10-17, 2013.

[16] J. M. Kwon, K. T. Kim, and B. H. Kwon, "Instant voltage compensator based on a three-leg converter," *IET Power Electronics,* vol. 6, no. 8, pp. 1618-1625, 2013.

[17] M. Badawy, A. Ahmed, Y. Sozer, and P. Yi, "Active THD reduction strategy for grid connected EV charging stations," in *2013 IEEE Energytech*, 2013, pp. 1-5.

[18] H. M. Suryawanshi, M. R. Ramteke, K. L. Thakre, and V. B. Borghate, "Unity-Power-Factor Operation of Three-Phase AC-DC Soft Switched Converter Based On Boost Active Clamp

Topology in Modular Approach," *Power Electronics, IEEE Transactions on,* vol. 23, no. 1, pp. 229-236, 2008.

[19] A. Koran, T. LaBella, and L. Jih-sheng, "High Efficiency Photovoltaic Source Simulator with Fast Response Time for Solar Power Conditioning Systems Evaluation," *Power Electronics, IEEE Transactions on,* vol. 29, no. 3, pp. 1285-1297, 2014.

[20] K. Yao, Q. Meng, Y. Bo, and W. Hu, "Three-Phase Single-Switch DCM Boost PFC Converter with Optimum Utilization Control of Switching Cycles," *Industrial Electronics, IEEE Transactions on,* vol. PP, no. 99, pp. 1-1, 2015.

[21] Y. Xia, K. H. Ahmed, and B. W. Williams, "A New Maximum Power Point Tracking Technique for Permanent Magnet Synchronous Generator Based Wind Energy Conversion System," *Power Electronics, IEEE Transactions on,* vol. 26, no. 12, pp. 3609-3620, 2011.

[22] A. El Aroudi, M. Orabi, R. Haroun, and L. Martinez-Salamero, "Asymptotic Slow-Scale Stability Boundary of PFC AC-DC Power Converters: Theoretical Prediction and Experimental Validation," *Industrial Electronics, IEEE Transactions on,* vol. 58, no. 8, pp. 3448-3460, 2011.

[23] I. Abdelsalam, G. P. Adam, D. Holliday, and B. W. Williams, "Single-stage ac–dc buck–boost converter for medium-voltage high-power applications," *IET Renewable Power Generation,* 2015.

[24] Y. Lung-Sheng, L. Tsorng-Juu, and C. Jiann-Fuh, "Analysis and Design of a Novel Three-Phase AC-DC Buck-Boost Converter," *Power Electronics, IEEE Transactions on,* vol. 23, no. 2, pp. 707-714, 2008.

[25] D. S. Wijeratne and G. Moschopoulos, "A Novel Three-Phase Buck-Boost AC-DC Converter," *Power Electronics, IEEE Transactions on,* vol. 29, no. 3, pp. 1331-1343, 2014.

[26] A. Hajizadeh, A. H. Shahirinia, N. Namjoo, and D. C. Yu, "Self-tuning indirect adaptive control of non-inverting buck-boost converter," *IET Power Electronics,* vol. 8, no. 11, pp. 2299-2306, 2015.

[27] C. Yang, X. I. E. S, L. Mao, and Z. Zhang, "Efficiency improvement on two-switch buck-boost converter with coupled inductor for high-voltage applications," *IET Power Electronics,* vol. 7, no. 11, pp. 2846-2856, 2014.

[28] M. R. Banaei, H. Ardi, and A. Farakhor, "Analysis and implementation of a new single-switch buck-boost dc/dc converter," *IET Power Electronics,* vol. 7, no. 7, pp. 1906-1914, 2014.

[29] A. R. Borges and I. Barbi, "A single stage buck-boost three-phase rectifier with high power factor operating in continuous conduction mode (CCM)," in *2011 IEEE International Symposium of Circuits and Systems (ISCAS)*, 2011, pp. 2777-2780.

[30] A. R. Borges and I. Barbi, "Three-phase single stage AC-DC Buck-Boost converter operating in Buck and Boost modes," in *XI Brazilian Power Electronics Conference*, 2011, pp. 176-182.

[31] I. Abdelsalam, G. P. Adam, D. Holliday, and B. W. Williams, "Single-stage, single-phase, ac–dc buck–boost converter for low-voltage applications," *IET Power Electronics,* vol. 7, no. 10, pp. 2496-2505, 2014.

[32] A. R. Borges and I. Barbi, "Study of a single stage buck-boost three-phase rectifier with high power factor operating in discontinuous conduction mode (DCM)," in *2009 Brazilian Power Electronics Conference*, 2009, pp. 870-877.

[33] I. Abdelsalam, G. Adam, D. Holliday, and B. Williams, "An improved single-phase AC-DC buck-boost converter operating in a discontinuous conduction mode," 2016.

[34] A. Ahmed, M. A. Khan, M. Badawy, Y. Sozer, and I. Husain, "Performance analysis of bi-directional DC-DC converters for electric vehicles and charging infrastructure," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 1401-1408.

[35] R. S. Weissbach and K. M. Torres, "A noninverting buck-boost converter with reduced components using a microcontroller," in *Proceedings. IEEE SoutheastCon 2001 (Cat. No.01CH37208)*, 2001, pp. 79-84.

[36] Y. M. Chen, Y. L. Chen, and C. W. Chen, "Progressive smooth transition for four-switch buck-boost converter in photovoltaic applications," in *2011 IEEE Energy Conversion Congress and Exposition*, 2011, pp. 3620-3625.

[37] L. Callegaro, M. Ciobotaru, D. J. Pagano, E. Turano, and J. E. Fletcher, "A Simple Smooth Transition Technique for the Non-Inverting Buck-Boost Converter," *IEEE Transactions on Power Electronics,* vol. PP, no. 99, pp. 1-1, 2017.

[38] C. Jingquan, D. Maksimovic, and R. W. Erickson, "Analysis and design of a low-stress buck-boost converter in universal-input PFC applications," *IEEE Transactions on Power Electronics,* vol. 21, no. 2, pp. 320-329, 2006.

[39] S. Singh, B. Singh, G. Bhuvaneswari, and V. Bist, "A Power Quality Improved Bridgeless Converter-Based Computer Power Supply," *IEEE Transactions on Industry Applications,* vol. 52, no. 5, pp. 4385-4394, 2016.

[40] V. Bist and B. Singh, "An Adjustable-Speed PFC Bridgeless Buck–Boost Converter-Fed BLDC Motor Drive," *IEEE transactions on industrial electronics,* vol. 61, no. 6, pp. 2665-2677, 2014.

[41] J. W. Kolar, H. Ertl, and F. C. Zach, "Influence of the modulation method on the conduction and switching losses of a PWM converter system," *Industry Applications, IEEE Transactions on,* vol. 27, no. 6, pp. 1063-1075, 1991.

[42] Y. Zhang1, G. P. Adam2, T.C.Lim, S. J. Finney, and a. B. W. Williams, "Voltage Source Converter in High Voltage Applications: Multilevel versus Two-level Converters," in *IET, the 9th International Conference on AC and DC Power Transmission*, London, UK, 2010.

[43] C. Oates and C. Davidson, "A comparison of two methods of estimating losses in the Modular Multi-Level Converter," in *Proceedings of the 2011-14th European Conference on Power Electronics and Applications (EPE 2011)*, 2011, pp. 1-10.

[44] I. Abdelsalam, G. P. Adam, D. Holliday, and B. W. Williams, "Three-phase ac–dc buck–boost converter with a reduced number of switches," *IET Renewable Power Generation,* vol. 9, no. 5, pp. 494-502, 2015.

[45] D. Wijeratne, G. Moschopoulos, and M. Narimani, "Analysis and design of a three-phase buck-boost quasi-resonant reduced switch rectifier," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 2000-2007.

[46] L. Congwei, C. Jianyun, S. Xudong, and W. Sanmin, "Single-switch step-up/down three-phase rectifier with sinusoidal input current," in *Conference Record of the 2004 IEEE Industry Applications Conference, 2004. 39th IAS Annual Meeting.*, 2004, vol. 1, pp. 1-481.