

On the Qubit Routing Problem

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Abstract

We introduce a new architecture-agnostic methodology for mapping abstract quantum circuits to realistic quantum computing devices with restricted qubit connectivity, as implemented by Cambridge Quantum Computing's `t|ket>` compiler. We present empirical results showing the effectiveness of this method in terms of reducing two-qubit gate depth and two-qubit gate count, compared to other implementations.

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1 Introduction

There is a significant gap between the theoretical literature on quantum algorithms and the way that quantum computers are implemented. The simple and popular *quantum circuit model* presents the quantum computer as a finite number of qubits upon which quantum gates act; see Fig. 1 for an example. Typically gates act on one or two-qubits at a time, and the circuit model allows multi-qubit gates to act on any qubits without restriction. However, in realistic hardware the qubits are typically laid out in a fixed two or three dimensional topology where gates may only be applied between neighbouring qubits. In order for a circuit to be executed on such hardware, it must be modified to ensure that whenever two-qubits are required to interact, they are adjacent in memory. This is a serious departure from the von Neumann architecture of classical computers, where operations may involve data at distant locations in memory without penalty.



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We refer to the task of modifying a circuit to conform to the memory layout of a specific quantum computer as the *qubit routing problem*. When non-adjacent qubits are required to interact we can insert additional SWAP gates to exchange a qubit with a neighbour, moving it closer to its desired partner. In general many – or even all – of the qubits may need to be swapped, making this problem non-trivial. Since quantum algorithms are usually designed without reference to the connectivity constraints of any particular hardware, a solution to the routing problem is required before a quantum circuit can be executed. Therefore qubit routing forms a necessary stage of any compiler for quantum software. Current quantum computers – the so-called NISQ¹ devices – impose additional constraints. Their short coherence times and relatively low fidelity gates require that the circuit depth and the total number of gates are both as low as possible. As routing generally introduces extra gates into a circuit, increasing its size and depth, it is crucial that the circuit does not grow too much, or its performance will be compromised.

The general case of the routing problem, also called the qubit allocation problem, is known to be infeasible. The sub-problem of assigning logical qubits to physical ones is equivalent to sub-graph isomorphism [14], while determining the optimal swaps between assignments is equivalent to token-swapping [19] which is at least NP-hard [3] and possibly PSPACE-complete [10]. Siraichi et al. [14] propose an exact dynamic programming method (with complexity exponential in the number of qubits) and a heuristic method which approximates it well, at least on the small (5 qubit) circuits considered. Zulehner et al. [20] propose an algorithm based on depth partitioning and A* search which is specialised to the architectures of IBM devices [1]. Other approaches take advantage of the restricted topology typically found in quantum memories such as linear nearest neighbour [7] or hypercubic [4] which rely on classical sorting networks; see Appendix A for a discussion of this approach. Lower bound results for routing are presented by Herbert [5].

In this paper we describe the solution to the routing problem implemented in `t|ket`, a platform-independent compiler developed by Cambridge Quantum Computing Ltd². The heuristic method in `t|ket` matches or beats the results of other circuit mapping systems in terms of depth and total gate count of the compiled circuit, and has much reduced run time allowing larger circuits to be routed.

Aside from qubit routing, `t|ket` also provides translation from general circuits to any particular hardware-supported gate set, a variety of advanced circuit optimisation routines, and support for most of the major quantum software frameworks. These will be described in future papers. Compilation through `t|ket` guarantees hardware compatibility and minimises the depth and gate count of the final circuit across a range of hardware and software platforms.

In Section 2 we formalise the problem and present an example instance. In Section 3 we describe the method used by `t|ket` to solve the problem. In Section 4 we describe some of the architectures on which we tested the algorithm and in Section 5 we present empirical results of `t|ket`'s performance, both in terms of scaling and in comparison to other compiler software. Full tables of results are provided in the Appendix.

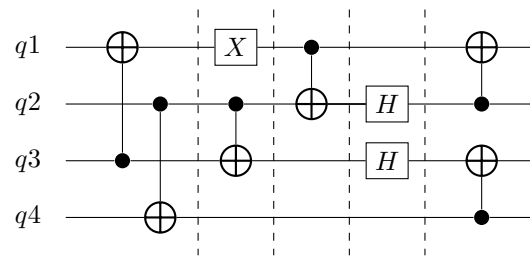
2 The Routing Problem

We represent a quantum computer as a graph where nodes are physical qubits and edges are the allowed two-qubit interactions³. Since the circuit model assumes we can realise a two-qubit gate between any pair of qubits, it is equivalent to the complete graph (Fig. 2a).

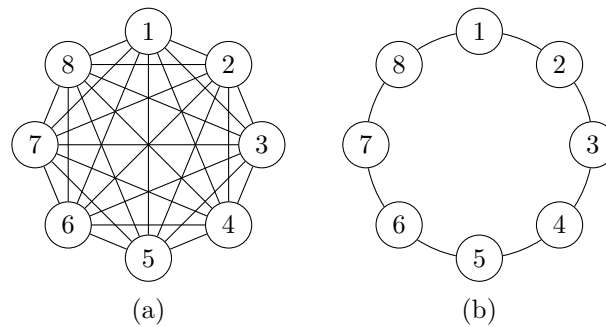
¹ “Noisy intermediate-scale quantum” devices; see [13] for a survey.

² `t|ket` is available as a python module from <https://pypi.org/project/pytket/>.

³ We don't consider architectures with multi-qubit interactions involving more than two-qubits.



■ **Figure 1** Example of a quantum circuit containing one and two-qubit gates acting on four qubits, $q1$, $q2$, $q3$ and $q4$. This circuit has five timesteps, each with gates acting on disjoint sets of qubits.



■ **Figure 2** Nodes in the graph represent physical qubits and edges are the allowed interactions. (a) The circuit model assumes all-to-all communication between qubits, *i.e.* a complete graph and (b) a physically realistic one-dimensional nearest neighbour cyclic graph, the ring.

Realistic qubit architectures are connectivity limited: for instance, in most superconducting platforms the qubit interaction graph must be planar; ion traps present more flexibility, but are still not fully connected. For now we will use the ring graph (Fig. 2b) as a simple example. Given such a restricted graph, our goal is to emulate the complete graph with minimal additional cost.

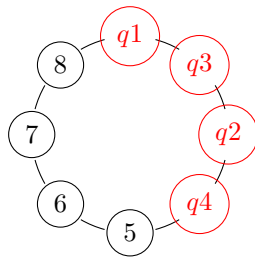
From this point of view, the routing problem can be stated as follows. Given (i) an arbitrary quantum circuit and (ii) a connected graph specifying the allowed qubit interactions, we must produce a new quantum circuit which is equivalent to the input circuit, but uses only those interactions permitted by the specification graph. Provided the device has at least as many qubits as the input circuit then a solution always exists; our objective is to minimise the size of the output circuit.

2.1 Example: Routing on a Ring

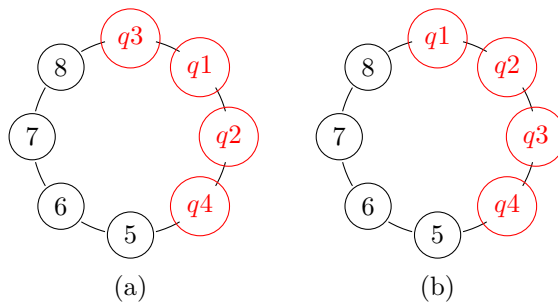
Let’s consider the problem of routing the circuit shown in Fig. 1 on the ring graph of Fig. 2(b). The first step is to divide the circuit into *timesteps*, also called *slices*. Loosely speaking, a timestep consists of a subcircuit where the gates act on disjoint sets of qubits and could in principle all be performed simultaneously (see Section 3.1 for a precise definition). The single qubit gates have no bearing on the routing problem so can be ignored, and thus a timestep can be reduced to a set of qubit pairs that are required to interact via some two-qubit gate.

Next, the logical qubits of the circuit must be mapped to the nodes of the graph. For our example a reasonable initial mapping is $q1 \rightarrow 1$, $q3 \rightarrow 2$, $q2 \rightarrow 3$, $q4 \rightarrow 4$ as shown in Fig. 3. This has the advantage that the qubits which interact in the first timestep are adjacent in the graph, and the same for the second timestep.

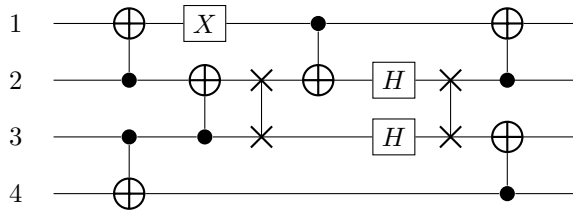
5:4 On the Qubit Routing Problem



■ **Figure 3** An initial mapping of logical qubits to nodes. Highlighted nodes are labelled with the mapped qubit.



■ **Figure 4** (a) Qubit mapping to nodes if $q1$ and $q3$ swap positions. (b) Qubit mapping to nodes if $q2$ and $q3$ swap positions.



■ **Figure 5** Quantum circuit in Fig. 1 mapped to architecture graph of Fig. 2b.

However at the third timestep our luck has run out: the CNOT gate between $q1$ and $q2$ is not possible in the current configuration. We must add SWAP gates to exchange logical qubits to enable the desired two-qubit interactions. In the example there are two candidates: swapping nodes 1 and 3, or swapping nodes 2 and 3, yielding the configurations shown in Fig. 4. Looking ahead to the final slice – slice 4 has no two-qubit gates so can be ignored – we see that $q3$ and $q4$ will need to interact. In configuration (a) these qubits are distance 3 apart, and hence two additional swaps will be needed to bring them together. In configuration (b) however they are already adjacent. As we want to minimise the number of additional elements to our circuit we choose to swap nodes 2 and 3 to yield the final circuit shown in Fig. 5.

While this was a tiny example we can see in microcosm all the key elements of the problem: the need to find a mapping of qubits to nodes; the notion of distance between qubits at the next timestep; and the need to compute the permutation of the nodes to enable the next timestep. It should be clear even from this small example that as the size of the circuit increases the number of candidate swaps increases dramatically. Further, if we have

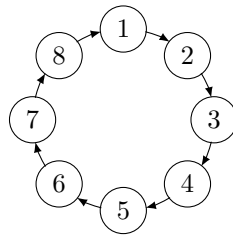
to swap several pairs of qubits at the same time, improving the situation for one pair may worsen the situation for another pair. There is a clear arbitrage to apply to bring all the pairs together as soon as possible.

In the worst case $\mathcal{O}(n^2)$ swaps suffice to get from any n -node configuration to any other [19], although for sufficiently regular graphs much better is possible [4]. A recent lower bound result states that the minimum number of swaps is $\mathcal{O}(\log n)$ in the worst case [5], which is achieved by the cyclic butterfly network [4].

Our goal is to optimise the circuit globally so finding optimal mappings between timesteps is not sufficient. It is necessary to evaluate candidate mappings across multiple timesteps; this is the core of the `t|ket` routing algorithm.

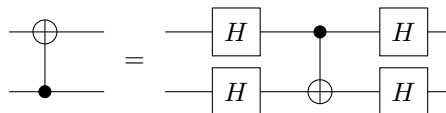
2.2 SWAP Synthesis and Routing

In the preceding section we described the routing problem in terms of inserting SWAP gates into the circuit. However not all device technologies offer SWAP as a primitive operation. Superconducting devices, for example, typically offer a single two-qubit interaction from which all other gates, including the SWAP, must be constructed. As a further complication, these interactions may be asymmetric. For example, in some IBM devices [1], the two-qubit interaction is a CNOT where one qubit is always the control and the other always the target. The graph representing the machine is therefore directed, as shown in Fig. 6, where the direction indicates the orientation of the gate.



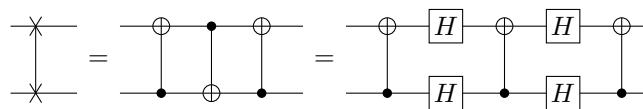
■ **Figure 6** Architecture with one-way connectivity constraint.

This complication is easily removed by the usual trick of inserting Hadamard gates, as in Fig. 7. Hence the swap gate can be implemented by three (unidirectional) CNOTs and four Hadamards, as in Fig. 8.

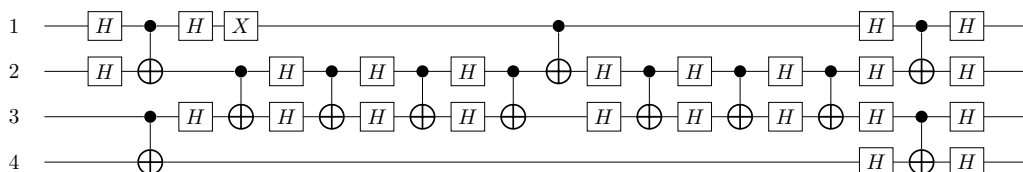


■ **Figure 7** Inverting a CNOT gate for a directed graph.

Consider running our routed quantum circuit on the directed architecture of Fig. 6. As this graph constrains the direction of interactions, the quantum circuit we produced is no longer valid. We account for this using the inversion in Fig. 7, producing the circuit shown in Fig. 9. Many simplifications are possible on the resulting circuit, but care must be taken to ensure that the simplified circuit is still conformant to the architecture digraph.



■ **Figure 8** Representation of a SWAP gate in terms of three consecutive CNOT and its inverted representation for a directed graph.



■ **Figure 9** Quantum circuit in Fig. 1 routed for architecture graph in Fig. 6.

3 The $t|\text{ket}\rangle$ Routing Procedure

The routing algorithm implemented in $t|\text{ket}\rangle$ guarantees compilation of any quantum circuit to any architecture, represented as simple connected graph. It is therefore completely hardware agnostic. The algorithm proceeds in four stages: decomposing the input circuit into timesteps; determining an initial placement; routing across timesteps; and a final clean-up phase.

3.1 Slicing the Circuit Into Timesteps

Before routing we partition the quantum circuit into timesteps. The circuit structure provides a natural partial ordering of the gates; thus a greedy algorithm starting from inputs can divide the input circuit into “vertical” partitions of gates which can be executed simultaneously. We simply traverse the circuit adding the qubits involved in a two-qubit gate to the current timestep. Since only multi-qubit interactions (such as CNOT or CZ gates) constrain the problem, single-qubit gates can be ignored⁴. If a gate requires a qubit already used in the previous timestep, a new timestep is created. This procedure is repeated until all gates are assigned to a timestep. A timestep thus consists of a set of disjoint pairs of (logical) qubits which represent gates scheduled for simultaneous execution.

Applying this method to the example from Fig. 1 would yield the following timesteps.

$$\begin{aligned} 1 &\mapsto \{ (q1, q3), (q2, q4) \} \\ 2 &\mapsto \{ (q2, q3) \} \\ 3 &\mapsto \{ (q1, q2), (q3, q4) \} \\ 4 &\mapsto \{ (q1, q2) \} \end{aligned}$$

Note, that this is not the same as the illustrative slicing shown in Fig. 1!

The *density* of a timestep is a measure of the number of simultaneous gates executed. For an n -qubit architecture with single and two-qubit gates, the density is

$$d = \frac{\#\text{two-qubit gates}}{\lfloor \frac{n}{2} \rfloor}.$$

⁴ More accurately: while the single-qubit gates can be ignored for the purposes of routing, they must be retained for circuit generation; for clarity we ignore them for now.

Note that $d = 1$ where every qubit is involved in a two-qubit gate in this timestep; a timestep is *sparse* when its density is close to zero. In principle, the density could be constrained to make routing easier. In practice this seems to make little difference, and we use this quantity only for the analysis in Section 5.1.

3.2 Initial Mapping

For the routing algorithm to proceed we require an initial mapping of logical qubits (referred to as qubits) and physical qubits (referred to as nodes). In `t|ket` a simple but surprisingly effective procedure is used.

We iterate over the timesteps to construct a graph whose vertices are qubits. At timestep n we add the edge (q, q') to the graph if (i) this pair is present in the timestep and (ii) both qubits q and q' have degree less than 2 in the current graph. Each connected component of the resulting graph is necessarily either a line or a ring; the rings are broken by removing an arbitrarily chosen edge.

Disconnected qubits in this graph correspond either to qubits which never interact at all, or to those whose first interaction is with a qubit whose first two interactions are with others. These disconnected qubits are not included in the initial placement at all; they are added later in the routing procedure.

We then select a subgraph of the architecture with high average degree and low diameter to start from. If the architecture is Hamiltonian connected – all the common architectures are⁵ – then it is possible to map the qubit graph to the architecture as one long line starting from a high degree vertex within this subgraph, and greedily choosing the highest degree available neighbour. This ensures that most of the gates in the first two timesteps can be applied without any swaps; the only exceptions are those gates corresponding to the edges removed when breaking rings.

If the initial mapping cannot be completed as one long line, then the line is split and mapped as several line segments.

3.3 Routing

The routing algorithm iteratively constructs a new circuit which conforms to the desired architecture, taking the sliced circuit and the current mapping of qubits to nodes as input.

The algorithm compares the current timestep of the input circuit to the current qubit mapping. If a gate in the current timestep requires a qubit which has not yet been mapped, it is allocated to the nearest available node to its partner. All gates which can be performed in the current mapping – all single-qubit gates and those two-qubit gates whose operands are adjacent – are immediately removed from the timestep and added to the output circuit. If this exhausts the current timestep, we advance to the next; otherwise SWAPs must be added.

We define a distance vector $d(s, m)$ which approximates the number of SWAPs needed to make timestep s executable in the mapping m ; these vectors are ordered pointwise. Let s_0 denote the current timestep, s_1 for its successor, and so on, and write $\sigma \bullet m$ to indicate the action of swap σ upon the mapping m . We compute a sequence of sets of candidate SWAPs as follows:

$$\begin{aligned}\Sigma_0 &= \text{swaps}(s_0) \\ \Sigma_{t+1} &= \arg \min_{\sigma \in \Sigma_t} d(s_t, \sigma \bullet m)\end{aligned}$$

⁵ See Section. 4 and Refs. [18, 8].

where $\text{swaps}(s_0)$ denotes all the pertinent swaps available at the initial timestep. The sequence terminates either when $|\Sigma_t| = 1$ or after a predefined cutoff. The selected SWAP is added to the circuit and the mapping is updated accordingly. We now return to the start and continue until the entire input circuit has been consumed.

The pointwise ordering of the distance vectors employed by $\mathbf{t}|\text{ket}\rangle$ is strict in the sense that $d(s, m) > d(s, \sigma \bullet m)$ implies that for *all* pairs of qubits (q, q') in s , the longest of the shortest paths between any two paired qubits in $s \bullet m$ is not longer than the longest of the shortest paths in m . In other words, the diameter of the subgraph composed of all pairs of qubits (q, q') in s should decrease strictly under the action of swap σ on the mapping m . In consequence, in some highly symmetric configurations, the algorithm sometimes gets stuck, failing to find any candidate swap. We employ two strategies to overcome this. The first is to attempt the process again with pairs of disjoint swaps instead of individual ones. If this also fails then we resort to brute force: a pair of maximally distant qubits in the current timestep are brought together using a sequence of swaps along their shortest connecting path. This guarantees at least one gate may be performed, and disrupts the symmetry of the configuration, hopefully allowing the algorithm to escape from the bad configuration.

Remark

In practice there is no need to slice the circuit in advance, and in fact better results are achieved by computing the timesteps dynamically during routing. The “next slice” is recomputed immediately after each update of the mapping, avoiding any unnecessary sequentialisation.

3.4 SWAP Synthesis and Clean-Up

If the target hardware does not support SWAP as a primitive operation, after the circuit has been routed the SWAPs in the routed circuit must be replaced with hardware appropriate gates, as per Section 2.2. While we assume that the input circuit was already well-optimised before routing, it is usually possible to remove some of the additional gates which are inserted during this process in a final clean-up pass.

The essential criterion here is that any changes to the circuit must respect the existing routing. This can be guaranteed by using any set of rewrite rules between one- and two-qubit circuits. The routing procedure will not insert SWAPs immediately before a two-qubit gate on the same two qubits, but it may do so afterwards, so the possibility to, for example, cancel consecutive CNOT gates exists. However such cancellation rules are the only “true” two-qubit rewrites which can be applied. In addition, $\mathbf{t}|\text{ket}\rangle$ uses a small set of rewrites for fusing single-qubit gates, and commuting single qubit gates past two-qubit gates. The particular rewrite rules vary according to supported gates of the hardware.

4 Graph Representation of Quantum Computers

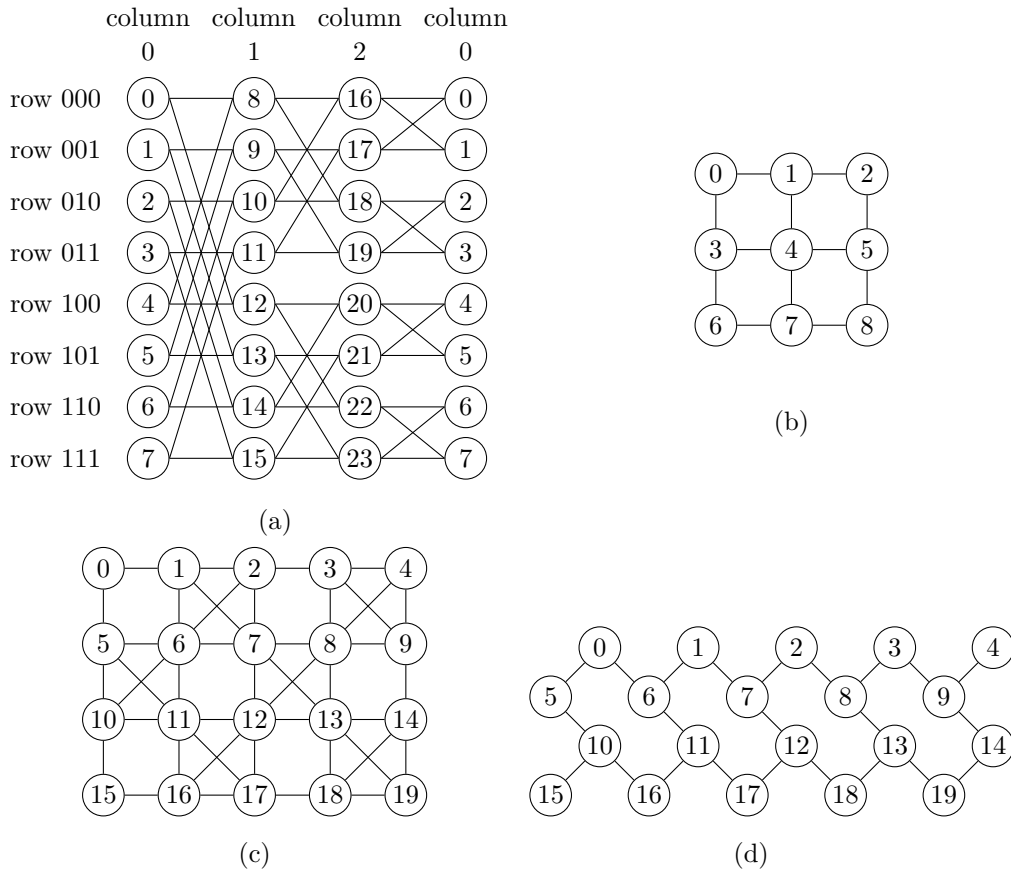
We represent the architecture of a given quantum computer as a simple connected graph, directed or undirected. We now list some specific architecture graphs used in this work.

1. *The ring*, Fig. 2(b). A one-dimensional cyclic graph where each node is connected to its two nearest neighbors.
2. *The cyclic butterfly*, Fig. 10(a). A non-planar graph with $n = r \times 2^r$ nodes. Each node is denoted by a pair (w, i) where w is r -bit sequence corresponding to one of the 2^r rows and i represents the column. Two nodes (w, i) and (v, j) are connected if $j \equiv i + 1 [r]$

and if $w = v$ or w and v have only one bit difference at position i , hence the connectivity is equal to 4 for any node, see Ref. [4].

3. *The square grid*, Fig. 10(b). A two-dimensional graph with a square shape where nodes are connected to their four neighbors except at the edges where there can be only two or three neighbors.
4. *The IBM Q 20 Tokyo*, Fig. 10(c). The graph supporting the 20-qubit processor produced by IBM is a two-dimensional graph with 20 nodes, it is rectangular with some extra connectivity, see Ref. [1].
5. *The Rigetti 19Q-Acorn*, Fig. 10(d). The graph supporting the quantum processor produced by Rigetti is a two-dimensional graph with 20 nodes, see Ref. [15].

In Appendix A Table 3 we present the basic properties of these graphs such as their degree and diameter, and the depth overhead of classical sorting algorithms on these graphs.



■ **Figure 10** (a) a cyclic butterfly graph with $n = 3 \times 2^3$ nodes (the first column is represented twice to improve the readability of the connectivity), (b) a 2-dimensional square grid with $n = 3^2$ nodes, (c) the IBM Q 20 Tokyo chip (Ref. [1]). and (d) the Rigetti 19Q-Acorn chip (Ref. [15]). The edges represent the allowed interactions between qubits.

5 Results

The current generation of quantum computers, the NISQ devices [13], are characterised by small numbers of qubits and shallow circuit depths. In this setting constant factors are more important than asymptotic analysis, so we present two sets of empirical results on the performance of `t|ket)`'s routing algorithm. In the first set of results we evaluate the scaling behaviour on synthetic inputs of increasing size. In the second we compare the performance of `t|ket)` against competing compiler implementations on a set of realistic circuits. Note that while the `t|ket)` algorithm is very efficient, we report on the quality of the results rather than the time or memory requirements.

5.1 Scaling

The routing algorithm described in Section 3 can handle circuits of arbitrary depth, and architectures corresponding to any connected graph. We now evaluate how increasing the circuit depth, as well as the size and connectivity of the architecture graph influence the depth of the routed circuit.

As described above, routing adds SWAP gates to the circuit, increasing both its total gate count and the depth of the circuit. Since the total gate count depends on the particular gate set supported by the architecture, we will consider only the increase in circuit depth here. Therefore a reasonable figure of merit is the depth ratio:

$$R = \frac{\text{number of output timesteps}}{\text{number of input timesteps}},$$

where timesteps are computed as described in Section 3.1. We define the mean depth *overhead* as

$$N = \text{number of output timesteps} - \text{number of input timesteps}.$$

For a fair comparison to classical sorting algorithms, we consider that a SWAP gate counts as only one additional gate rather than, for example, three when decomposed into CNOT gates, and hence will induce at most one additional timestep.

5.1.1 Scaling With Depth

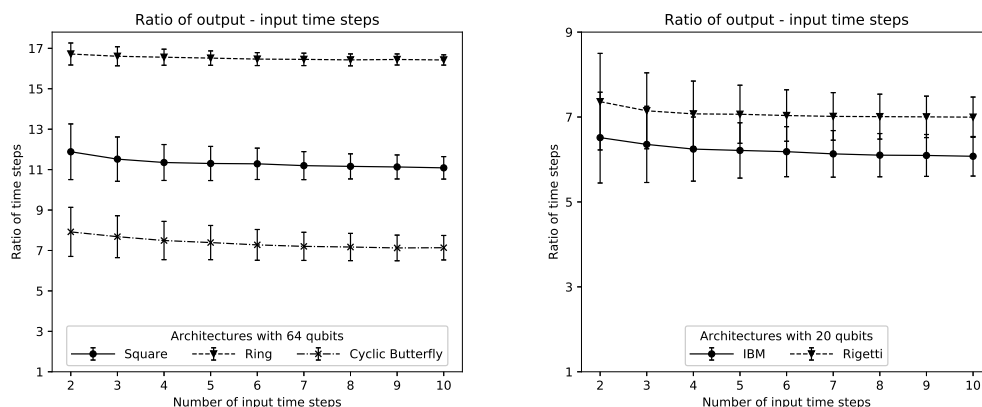
To assess the performance of `t|ket)` with respect to increasingly deep circuits we perform the following protocol for each of the selected architectures.

- We randomly generate 1000 circuits of density $d = 1$ and t initial timesteps for $t \in [2, 10]$. Note that requiring $d = 1$ implies there are no single-qubit gates in the circuit.
- Use `t|ket)` to route the circuit on the chosen architecture.
- Compute R for the routed circuit.

We tested using the following five architectures:

- a ring of size $r = 64$;
- a square grid of size $r^2 = 64$;
- a cyclic butterfly of size $r2^r = 64$;
- the IBM Q 20 Tokyo ($n = 20$);
- the Rigetti 19Q-Acorn⁶ ($n = 20$).

⁶ The Rigetti Acorn has only 20 qubits, but due a manufacturing defect which only 19 are *usable*. This is not relevant to our tests [12].



■ **Figure 11** Multiple timesteps measurement and architecture comparison. The mean and standard deviation of the ratio R are represented. The left plot overlaps results for the ring, square grid and cyclic butterfly for 64 nodes. The right plot overlaps results for IBM and Rigetti architectures with 20 nodes. Results generated with random initial (dense) circuits with density equal to unity.

The number of nodes for the ring, square grid and cyclic butterfly architectures is chosen for fair comparison and similarly for the IBM and the Rigetti cases. To eliminate sampling bias, a single set of 64-qubit circuits was generated for all the $n = 64$ architectures, and similarly for the $n = 20$ architectures.

Figure 11 represents the mean and standard deviation of the ratio R for the graphs. The ratio R is approximately constant and the effect of circuit depth is dominated by the influence of the architecture's connectivity. This ratio seems to converge for circuits of depth greater than 5 and we report in Table 2 the values of R obtained for the largest number of input timesteps. While the ratios obtained seem rather large, it is worth remembering that $d = 1$ circuits are the worst case for routing.

5.1.2 Scaling With Architecture Size

To evaluate the scaling with respect to the size of the architecture we consider single-timestep random quantum circuits of varying density, which are routed on architectures of increasing size. Initial qubit mapping is disabled for these tests so that only the routing procedure is evaluated. While this is an important part of the algorithm, in this case we are interested in the scaling, to which the initial mapping only provides an initial offset.

- For each architecture of size n generate $10n$ random circuits of depth one, for each $d \in \{0.5, 0.67, 1.0\}$.
- Generate a random initial mapping of qubits on the architecture.
- Route the timestep using $t|\text{ket}\rangle$, using the given mapping.
- Compute N for the routed circuit.

The following architectures were evaluated:

- Rings of size $r \in [10, 200]$
- Square grids of size r^2 , $r \in [3, 13]$
- Cyclic butterflies of size $r2^r$, $r \in [2, 6]$.

The results are shown in Fig. 12 and the best fit parameters are given in Table 1. The prior results for the ring and square grid are determined with a regression in log-log space

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■ **Table 1** Scaling of the depth overhead with architecture size for single-timestep random circuits.

Graph	$d = 0.5$	$d = 0.67$	$d = 1.0$
Ring	$0.2451 \times n$	$0.2451 \times n$	$0.2451 \times n$
Square	$0.5501 \times n^{0.55}$	$0.8050 \times n^{0.56}$	$0.8991 \times n^{0.58}$
Cyclic Butterfly	$0.3496 \times \log(n)^{1.85}$	$0.3002 \times \log(n)^{2.05}$	$0.1510 \times \log(n)^{2.72}$

■ **Table 2** Summary of our scaling results for dense circuits ($d = 1$).

Graph	Depth overhead N for single-timestep circuits	Ratio output - input timesteps R
Ring	$0.2451 \times n^{1.00}$	16.42 ± 0.25 ($n = 64$)
Square grid	$0.8991 \times n^{0.58}$	11.09 ± 0.56 ($n = 64$)
Cyclic butterfly	$0.1510 \times \log(n)^{2.72}$	7.14 ± 0.61 ($n = 64$)
Rigetti 19Q-Acorn	\emptyset	7.00 ± 0.47
IBM Q 20 Tokyo	\emptyset	6.08 ± 0.47

and the cyclic butterfly in log - log(log) space (represented in the insets for $d = 1$). In each case we see that the overhead appears to grow with the diameter of the graph, although with an exponent that varies (slightly) with the density.

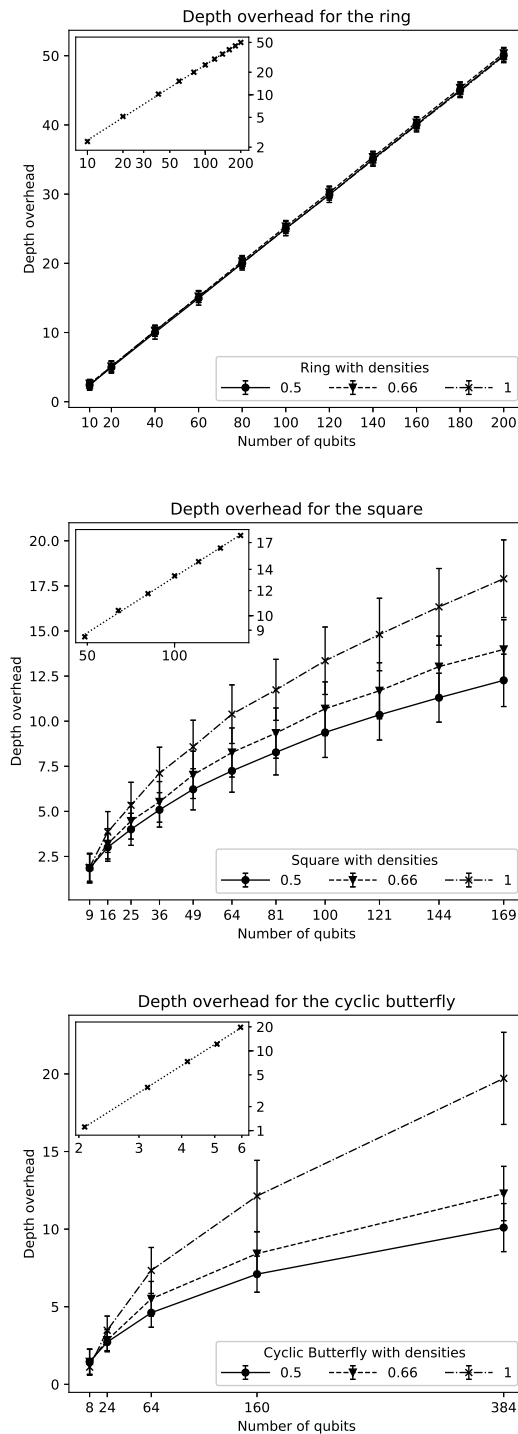
5.2 Realistic Benchmarks

Random circuits have an essentially uniform structure, which circuits arising from quantum algorithms typically lack. In certain cases this can make random circuits easier to route – although in the preceding section we have largely avoided this by using circuits of high density. To give $t|\text{ket}\rangle$ a more realistic test we have also evaluated its performance on a standard set of 156 circuits which perform various algorithms. These range in size from 6 to 16 qubits, and 7 to more than half a million gates.

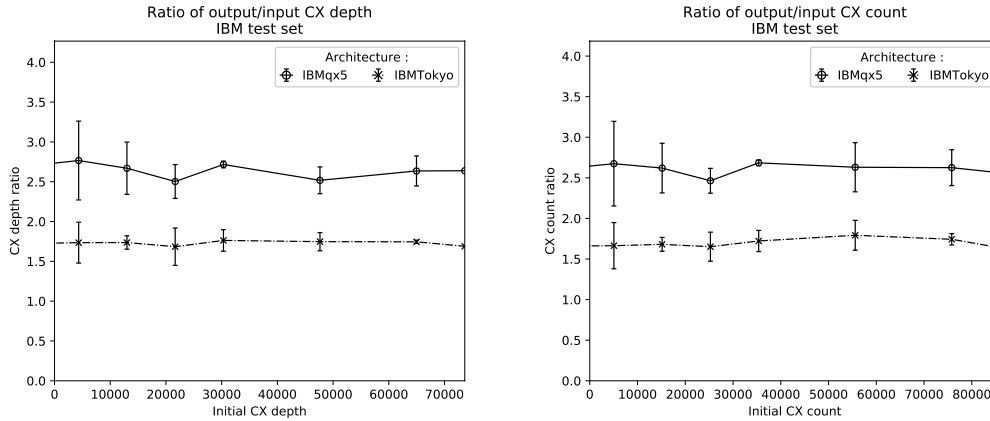
We ran $t|\text{ket}\rangle$ on each circuit of the benchmark set, with the 16-qubit *ibmqx5 Rueschlikon*, which is a 2×8 rectangular grid, as the target architecture. We then repeated the same test set using the 20-qubit IBM Tokyo as the target architecture. Since both these architectures have CNOT as their only two-qubit operation, and since it has lower fidelity than the single-qubit operations, we selected figures of merit based on minimising the CNOT count and depth of the output circuit. In this test we do perform SWAP synthesis, to get a more realistic evaluation of the output for these devices. Let $C_{CX}(c)$ be the total number of CNOT gates in circuit c , and let $D_{CX}(c)$ be the depth of the circuit counting only the CNOT gates. The two measures of interest are

$$R_D = \frac{D_{CX}(\text{out})}{D_{CX}(\text{in})} \quad R_C = \frac{C_{CX}(\text{out})}{C_{CX}(\text{in})}$$

where in and out are the input and output circuits respectively. The results are shown in Fig. 13. We can see that $t|\text{ket}\rangle$ achieves approximately linear overhead across the entire test



■ **Figure 12** Variation of depth overhead with architecture size for single timestep random circuits. Plots from left to right: the ring, square and cyclic butterfly architectures. The mean and standard deviation of the depth overhead versus number of nodes (or qubits) is represented. The inset plots represent the log-log linear fit for the ring and the square (resp. log-loglog fit for the butterfly) for the data set of density $d = 1$.



■ **Figure 13** Performance of $t|ket\rangle$ on realistic test examples. (left) Mean ratio of output to input CX depth as a function of circuit depth (averaged in bins) (right) Mean ratio of output to input CX count (averaged in bins).

set. The mean R_D of 2.64 and R_C of 2.61 for `ibmqx5`, and a mean R_D of 1.73 and R_C of 1.69 for IBM Tokyo.

We also compared the performance of $t|ket\rangle$ to a selection of other freely available quantum compiler systems: IBM’s QISKit [9], Project Q [16], and Rigetti Computing’s Quilc [15]⁷. None of the other compilers was able to complete the test set in the time allotted, despite being given at least an hour of compute time per example on a powerful computer⁸. For comparison, $t|ket\rangle$ completed the entire benchmark set in 15 mins on the same hardware. In addition, Project Q does not support routing for the IBM Tokyo architecture due to its unusual graph structure; therefore it was only tested on the `ibmqx5` architecture. Therefore comparison of all four compilers is only available for circuits of fewer than 2000 total gates. The comparative results are shown in Fig. 14. We can see that $t|ket\rangle$, Qiskit and Quilc exhibit approximately linear overhead, while Project Q appears somewhat worse than linear. A line of best fit calculated using the least squares method is shown for each compiler in Fig. 14. Quilc and $t|ket\rangle$ exhibit very similar performance; the others show significantly higher overhead.

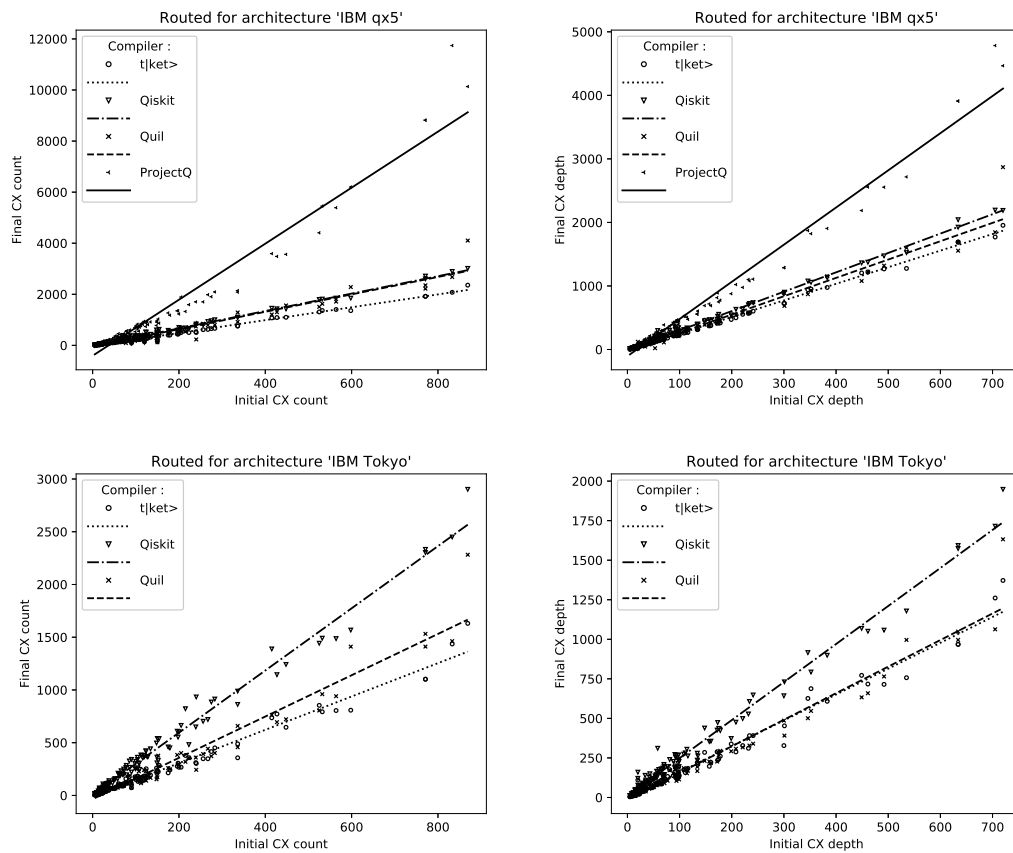
Finally, we compared the results to the published data of Zulehner et al. [20] who use the same benchmark set, but use total gate count and depth as the metric. Since Quilc does not generate the same gate set as the others, it was excluded from this comparison. The algorithm of Zulehner et al. [20] achieves comparable performance to $t|ket\rangle$. The results are presented in Appendix B.

The test set we used for this work was published by IBM as part of the QISKit Developer Challenge⁹, a public competition to design a better routing algorithm. The competition was won by Zulehner et al. [20]. The test circuits are available from http://iic.jku.at/eda/research/ibm_qx_mapping/.

⁷ Since Quilc emits CZ as its preferred two-qubit gate we computed its figures using D_{CZ} and C_{CZ} instead.

⁸ See Appendix B for more details.

⁹ <https://qx-awards.mybluemix.net/#qiskitDeveloperChallengeAward>



■ **Figure 14** Comparison of performance between different compilers. Top row: routing on the `ibmqx5` architecture. Bottom row: routing on the `IBM Tokyo` architecture. Left column: input CX count against output CX count. Right column: input CX depth against output CX depth. The benchmark is done against the test set available on http://iic.jku.at/eda/research/ibmqx_mapping/ and the results are averaged in bins when the initial count or depth is equal.

6 Conclusion

As better NISQ machines with the potential to effectively run quantum algorithms become available, the need for software solutions that allow users to easily run quantum circuits on them becomes more apparent. The `t|ket>` routing module is one such solution and provides hardware compatibility with minimal extra gate overhead. It is flexible, general and scalable. In this work we have outlined how the routing procedure works and the figures of merit we use to assess routing performance for different graphs.

Finally, we consider possible extensions of this work. Firstly, we note that reinforcement learning offers an alternative approach to the qubit routing problem [6]. Eventually we foresee implementing several approaches to routing in `t|ket>` to best adapt to differing algorithms and architectures.

Secondly, when considering the routing problem, we made the implicit assumption that all gates were equal. In real devices, notably superconducting devices, each gate has its own fidelity and run time and this has to be taken into account. Splitting a quantum circuit into timesteps becomes more complex as we introduce the different run times and we also have

to ensure that the overhead in the error rate encountered by qubits is as small as possible. Additionally, in real life experiments, it has been observed in [17] and [11] that even the properties of the qubits can fluctuate intra-days. This calls for a general protocol that could accommodate this constraint. Addressing these different constraints transforms the problem from a *routing* one to a *scheduling* one, which we plan to address with $t|ket\rangle$. Implementing these constraints and measuring $t|ket\rangle$ performance on this matter will be the object of future work.

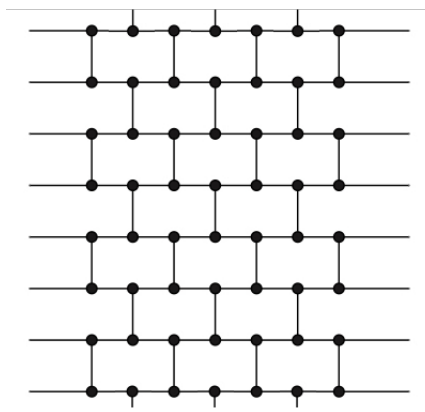
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A Dynamical Routing Versus Sorting Networks

The routing problem described in this work can be solved using classical sorting algorithms. One of these is the cyclic odd-even sort for the ring of Fig. 2b). Starting from an architecture with n nodes, one compares sequentially all even and odd labeled edges. After exactly $n - 1$ timesteps, the input will be sorted regardless of input.



■ **Figure 15** An example of sorting network on 8 inputs : odd-even sort over a ring.

For the ring, square and cyclic butterfly graphs presented in Section 4, we summarize in Table 3 some details on the degree and diameter these graphs and the depth overhead of classical sorting algorithms (precisely the quantity N introduced in Section 5).

The downside of classical sorting algorithms is that they are unadaptive: they compute the same sequence of comparisons regardless of input. As circuits are usually sparse, see Section 3.1, this leaves many unnecessary comparisons, and would treat quantum circuits as sequences of hard timesteps. Indeed, routing solutions derived from classical sorting algorithms tend to pack a quantum circuit into multiple timesteps and then insert SWAP gates in between timesteps. Solving the routing problem sequentially timestep by timestep produces a concatenation of locally optimal solutions which can be very far from the globally optimal one. A good solution should be dynamic, consider a SWAP gate's influence on multiple timesteps, and optimize the global problem rather than the local one. See Ref. [21] for an additional discussion on this matter. Additional details on sorting networks in quantum computing are available in Ref. [2, 4].

■ **Table 3** Comparison of different networks with n nodes.

Graph	Degree	Diameter	N
Ring	2	$\frac{n-1}{2}$	$n - 1$
Square grid	4	$2\sqrt{n} - 1$	$3\sqrt{n}$
Cyclic butterfly ($n = r \times 2^r$)	4	$\frac{3 \log_2(n)}{2}$	$6 \log_2(n)$

B Detailed Benchmark Results

The table rows are the names of the benchmark QASM circuits, which are available from www.github.com/iic-jku/ibm_qx_mapping. Benchmark data for Zulehner et al. is collected from results presented in their paper [20] – note they do not present data for the complete set of examples. An example Jupyter workbook which demonstrates the benchmarking procedure is found at https://github.com/CQCL/pytket/blob/master/examples/tket_benchmarking.ipynb.

All computations were run on a Google Cloud virtual machine with the following specification: machine type n1-standard-2 (2 vCPUs, 7.5GB Memory), Intel Broadwell, 16GB RAM and Standard Persistent Disk. Each example was run until completion, the computation aborted, or until 60 minutes of real time had passed, whichever came first. Note that Quilc aborts in much less than 60 minutes.

In the tables, g indicates the gate count of the circuit; in Table 4 this means all gates; in Table 5 and 6 this means CX count only. The circuit depth is labelled d ; in Table 4 this means total depth; in Table 5 and 6 this means CX depth only. The bold values are the best performance on the each row. The “ $t|ket\rangle$ comparison” column shows the ratio between $t|ket\rangle$ ’s performance and the best other compiler; values less than 1 indicate that $t|ket\rangle$ performs better.

NOTE

The example circuit “ground_state_estimation” gives anomalously low values after routing. This is due to an error in the circuit, which allows the post-routing clean-up pass of $t|ket\rangle$ to eliminate almost the entire circuit.

B.1 All Gates Comparison on ibmqx5

■ **Table 4** All gates comparison on ibmqx5.

Name	g_{in}	d_{in}	Qiskit 0.7.0		Zulehner et al.		CQC’s $t ket\rangle$		$t ket\rangle$ comparison	
			g_{out}	d_{out}	g_{out}	d_{out}	g_{out}	d_{out}	r_{gate}	r_{depth}
xor5_254	7	5	45	24	*	*	25	14	0.56	0.58
graycode6_47	5	5	13	7	*	*	15	9	1.15	1.29
ex1_226	7	5	56	32	*	*	25	14	0.45	0.44
4gt11_84	18	11	59	34	*	*	48	32	0.81	0.94
4mod5-v0_20	20	12	64	35	*	*	50	31	0.78	0.89
ex-1_166	19	12	53	36	*	*	53	34	1.00	0.94
4mod5-v1_22	21	12	75	46	*	*	64	40	0.85	0.87
mod5d1_63	22	13	94	53	*	*	65	39	0.69	0.74
ham3_102	20	13	62	39	*	*	47	32	0.76	0.82
4gt11_83	23	16	100	57	*	*	75	46	0.75	0.81
4gt11_82	27	20	109	61	*	*	86	55	0.79	0.90
rd32-v0_66	34	20	116	73	*	*	70	46	0.60	0.63
alu-v0_27	36	21	163	86	*	*	96	61	0.59	0.71
4mod5-v1_24	36	21	142	80	*	*	97	62	0.68	0.78
4mod5-v0_19	35	21	143	88	*	*	103	66	0.72	0.75
mod5mils_65	35	21	137	84	*	*	93	59	0.68	0.70

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Name	g_{in}	d_{in}	Qiskit 0.7.0		Zulehner et al.		CQC's $t \text{ket}\rangle$		$t \text{ket}\rangle$ comparison	
			g_{out}	d_{out}	g_{out}	d_{out}	g_{out}	d_{out}	r_{gate}	r_{depth}
rd32-v1_68	36	21	130	76	*	*	70	46	0.54	0.61
alu-v1_28	37	22	142	84	*	*	99	66	0.70	0.79
alu-v2_33	37	22	138	80	*	*	91	57	0.66	0.71
alu-v4_37	37	22	130	75	*	*	103	64	0.79	0.85
alu-v3_35	37	22	143	79	*	*	103	64	0.72	0.81
3_17_13	36	22	127	88	*	*	89	62	0.70	0.70
alu-v1_29	37	22	135	78	*	*	101	66	0.75	0.85
millier_11	50	29	158	107	*	*	139	92	0.88	0.86
alu-v3_34	52	30	212	126	*	*	146	99	0.69	0.79
decod24-v2_43	52	30	206	123	*	*	136	89	0.66	0.72
decod24-v0_38	51	30	173	108	*	*	127	84	0.73	0.78
mod5d2_64	53	32	185	110	*	*	158	105	0.85	0.95
4gt13_92	66	38	263	158	*	*	187	119	0.71	0.75
4gt13-v1_93	68	39	281	164	*	*	168	105	0.60	0.64
4mod5-v0_18	69	40	272	160	*	*	181	122	0.67	0.76
decod24-bdd_294	73	40	262	147	*	*	205	129	0.78	0.88
one-two-three- v2_100	69	40	256	151	*	*	194	129	0.76	0.85
one-two-three- v3_101	70	40	268	165	*	*	199	129	0.74	0.78
4mod5-v1_23	69	41	283	154	*	*	196	136	0.69	0.88
4mod5-bdd_287	70	41	283	152	*	*	212	133	0.75	0.88
rd32_270	84	47	289	167	*	*	220	148	0.76	0.89
4gt5_75	83	47	315	175	*	*	227	143	0.72	0.82
alu-bdd_288	84	48	319	170	*	*	253	160	0.79	0.94
alu-v0_26	84	49	331	188	*	*	230	145	0.69	0.77
decod24-v1_41	85	50	355	198	*	*	221	139	0.62	0.70
rd53_138	132	56	642	269	*	*	416	217	0.65	0.81
4gt5_76	91	56	360	195	*	*	266	168	0.74	0.86
4gt13_91	103	61	410	229	*	*	269	181	0.66	0.79
cnt3-5_179	175	61	684	275	*	*	569	221	0.83	0.80
qft_10	200	63	692	214	447	170	345	154	0.77	0.91
4gt13_90	107	65	427	250	*	*	284	190	0.67	0.76
alu-v4_36	115	66	410	232	*	*	286	184	0.70	0.79
mini_alu_305	173	69	829	317	474	225	524	243	1.11	1.08
ising_model_10	480	70	235	41	251	47	255	41	1.09	1.00
ising_model_16	786	71	391	41	426	48	426	41	1.09	1.00
ising_model_13	633	71	313	41	329	47	398	110	1.27	2.68
4gt5_77	131	74	451	266	*	*	356	226	0.79	0.85
sys6-v0_111	215	75	975	365	613	250	675	264	1.10	1.06
one-two-three- v1_99	132	76	501	299	*	*	354	233	0.71	0.78
one-two-three- v0_98	146	82	578	343	*	*	376	250	0.65	0.73
decod24-v3_45	150	84	551	318	*	*	383	247	0.70	0.78
4gt10-v1_81	148	84	555	310	*	*	377	248	0.68	0.80

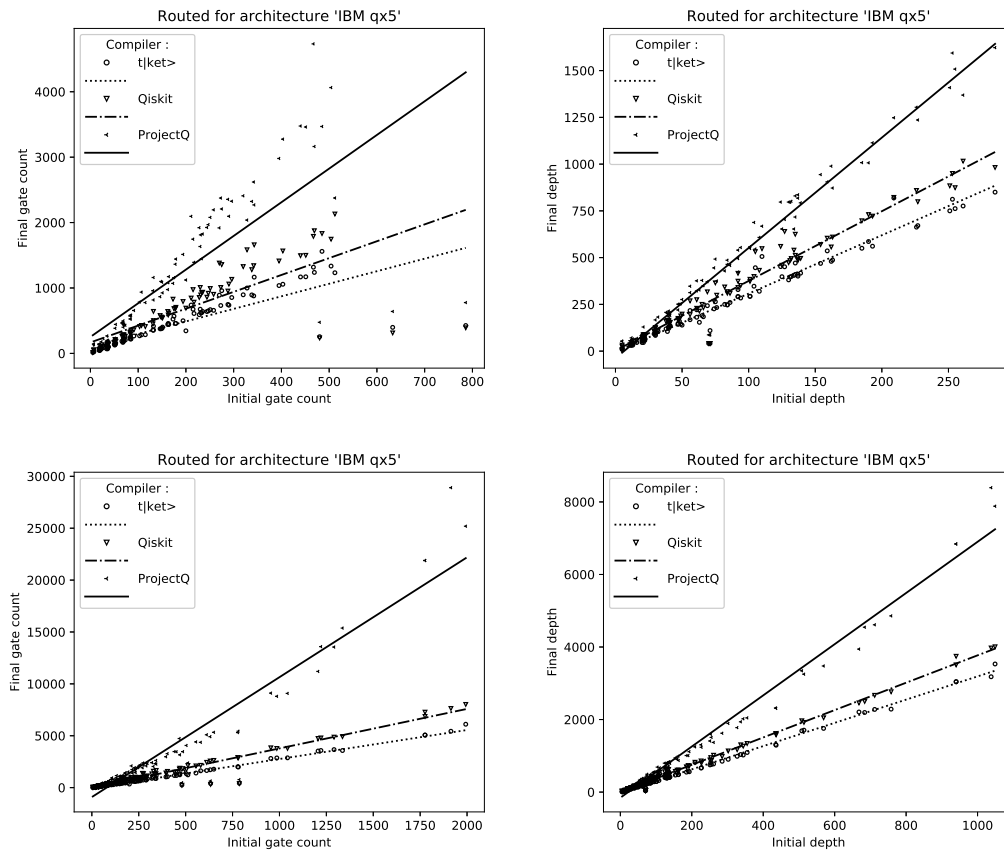
Name	g_{in}	d_{in}	Qiskit 0.7.0		Zulehner et al.		CQC's $t ket\rangle$		$t ket\rangle$ comparison	
			g_{out}	d_{out}	g_{out}	d_{out}	g_{out}	d_{out}	r_{gate}	r_{depth}
aj-e11_165	151	86	541	309	*	*	402	260	0.74	0.84
4mod7-v0_94	162	92	641	374	*	*	442	291	0.69	0.78
alu-v2_32	163	92	587	340	*	*	458	292	0.78	0.86
rd73_140	230	92	1008	416	656	301	675	329	1.03	1.09
4mod7-v1_96	164	94	617	351	*	*	443	284	0.72	0.81
4gt4-v0_80	179	101	704	373	*	*	458	293	0.65	0.79
mod10_176	178	101	685	384	*	*	459	293	0.67	0.76
0410184_169	211	104	846	399	758	336	739	347	0.97	1.03
qft_16	512	105	2131	532	1341	404	1233	446	0.92	1.10
4gt12-v0_88	194	108	793	432	*	*	499	320	0.63	0.74
rd84_142	343	110	1660	548	971	353	1166	506	1.20	1.43
rd53_311	275	124	1358	560	942	469	959	452	1.02	0.96
4_49_16	217	125	783	459	*	*	610	398	0.78	0.87
sym9_146	328	127	1584	640	955	425	999	451	1.05	1.06
4gt12-v1_89	228	130	855	473	*	*	592	381	0.69	0.81
4gt12-v0_87	247	131	919	484	*	*	650	396	0.71	0.82
4gt4-v0_79	231	132	893	495	*	*	622	399	0.70	0.81
hwb4_49	233	134	929	540	*	*	621	405	0.67	0.75
sym6_316	270	135	1381	625	852	456	890	471	1.04	1.03
4gt12-v0_86	251	135	992	512	*	*	668	410	0.67	0.80
4gt4-v0_72	258	137	903	485	*	*	658	401	0.73	0.83
4gt4-v0_78	235	137	935	492	*	*	641	411	0.69	0.84
mod10_171	244	139	859	496	*	*	640	417	0.75	0.84
4gt4-v1_74	273	154	1008	570	*	*	732	469	0.73	0.82
rd53_135	296	159	1132	604	*	*	854	536	0.75	0.89
mini-alu_167	288	162	953	557	*	*	748	480	0.78	0.86
one-two-three- v0_97	290	163	1060	610	*	*	737	487	0.70	0.80
ham7_104	320	185	1327	697	*	*	896	550	0.68	0.79
decod24- enable_126	338	190	1280	730	*	*	894	586	0.70	0.80
mod8-10_178	342	193	1341	722	*	*	879	561	0.66	0.78
cnt3-5_180	485	209	1833	822	1376	669	1560	819	1.13	1.22
ex3_229	403	226	1566	859	*	*	1057	663	0.67	0.77
4gt4-v0_73	395	227	1413	799	*	*	1037	671	0.73	0.84
mod8-10_177	440	251	1494	884	*	*	1169	750	0.78	0.85
C17_204	467	253	1789	950	*	*	1318	812	0.74	0.85
alu-v2_31	451	255	1499	874	*	*	1171	762	0.78	0.87
rd53_131	469	261	1875	1016	*	*	1238	776	0.66	0.76
alu-v2_30	504	285	1746	982	*	*	1335	850	0.76	0.87
mod5adder_127	555	302	2094	1135	*	*	1407	903	0.67	0.80
rd53_133	580	327	2149	1172	*	*	1623	986	0.76	0.84
cm82a_208	650	337	2624	1303	*	*	1777	1036	0.68	0.80
majority_239	612	344	2437	1267	*	*	1648	1022	0.68	0.81
ex2_227	631	355	2568	1340	*	*	1722	1092	0.67	0.81
sf_276	778	435	2895	1615	*	*	2012	1312	0.69	0.81

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Name	g_{in}	d_{in}	Qiskit 0.7.0		Zulehner et al.		CQC's $t \text{ket}\rangle$		$t \text{ket}\rangle$ comparison	
			g_{out}	d_{out}	g_{out}	d_{out}	g_{out}	d_{out}	r_{gate}	r_{depth}
sf_274	781	436	2875	1577	*	*	1989	1293	0.69	0.82
con1_216	954	508	3836	1966	*	*	2815	1689	0.73	0.86
wim_266	986	514	3777	1921	2985	1711	2861	1707	0.96	1.00
rd53_130	1043	569	3783	2049	*	*	2872	1756	0.76	0.86
f2_232	1206	668	4737	2459	*	*	3529	2208	0.74	0.90
cm152a_212	1221	684	4791	2499	3738	2155	3580	2195	0.96	1.02
rd53_251	1291	712	4868	2668	*	*	3665	2279	0.75	0.85
hwb5_53	1336	758	4917	2766	*	*	3577	2287	0.73	0.83
cm42a_207	1776	940	6862	3507	5431	3013	5066	3043	0.93	1.01
pm1_249	1776	940	7274	3744	5431	3013	5066	3043	0.93	1.01
dc1_220	1914	1038	7632	3973	5946	3378	5433	3180	0.91	0.94
squar5_261	1993	1049	8019	4006	6267	3448	6110	3532	0.97	1.02
z4_268	3073	1644	12567	6352	9717	5335	9379	5532	0.97	1.04
sqrt8_260	3009	1659	12852	6615	9744	5501	8869	5355	0.91	0.97
radd_250	3213	1781	13098	6880	10441	5872	9831	5892	0.94	1.00
adr4_197	3439	1839	13966	7050	11301	6205	10074	5910	0.89	0.95
sym6_145	3888	2187	14078	7794	*	*	10961	6858	0.78	0.88
misex1_241	4813	2676	-	-	15185	8729	14411	8834	0.95	1.01
rd73_252	5321	2867	-	-	*	*	15666	9288		
cycle10_2_110	6050	3386	-	-	19857	11141	18361	11314	0.92	1.02
hwb6_56	6723	3736	-	-	*	*	18688	11650		
square_root_7	7630	3847	-	-	25212	13205	23258	13305	0.92	1.01
ham15_107	8763	4819	-	-	28310	15891	26551	15951	0.94	1.00
dc2_222	9462	5242	-	-	30680	17269	29784	18303	0.97	1.06
sqn_258	10223	5458	-	-	32095	17801	29740	17456	0.93	0.98
inc_237	10619	5863	-	-	34375	19176	32096	19523	0.93	1.02
cm85a_209	11414	6374	-	-	37746	21189	34467	21014	0.91	0.99
rd84_253	13658	7261	-	-	45497	24473	41770	24147	0.92	0.99
co14_215	17936	8570	-	-	63826	30366	57906	30807	0.91	1.01
root_255	17159	8835	-	-	57874	30068	52900	30448	0.91	1.01
mlp4_245	18852	10328	-	-	*	*	59020	35251		
urf2_277	20112	11390	-	-	*	*	64763	37903		
sym9_148	21504	12087	-	-	66637	38849	61342	37448	0.92	0.96
life_238	22445	12511	-	-	74632	41767	67852	40987	0.91	0.98
hwb7_59	24379	13437	-	-	*	*	68463	41787		
max46_240	27126	14257	-	-	84914	46270	80329	46590	0.95	1.01
clip_206	33827	17879	-	-	114336	60882	104857	61053	0.92	1.00
9symml_195	34881	19235	-	-	116508	64279	106669	63651	0.92	0.99
sym9_193	34881	19235	-	-	116508	64279	106669	63651	0.92	0.99
sao2_257	38577	19563	-	-	131002	66975	120587	68114	0.92	1.02
dist_223	38046	19694	-	-	125867	66318	117367	67731	0.93	1.02
urf5_280	49829	27822	-	-	*	*	155513	92045		
urf1_278	54766	30955	-	-	*	*	178380	104583		
sym10_262	64283	35572	-	-	215569	118753	197690	118233	0.92	1.00
hwb8_113	69380	38717	-	-	*	*	201013	122660		
urf2_152	80480	44100	-	-	*	*	221274	139339		

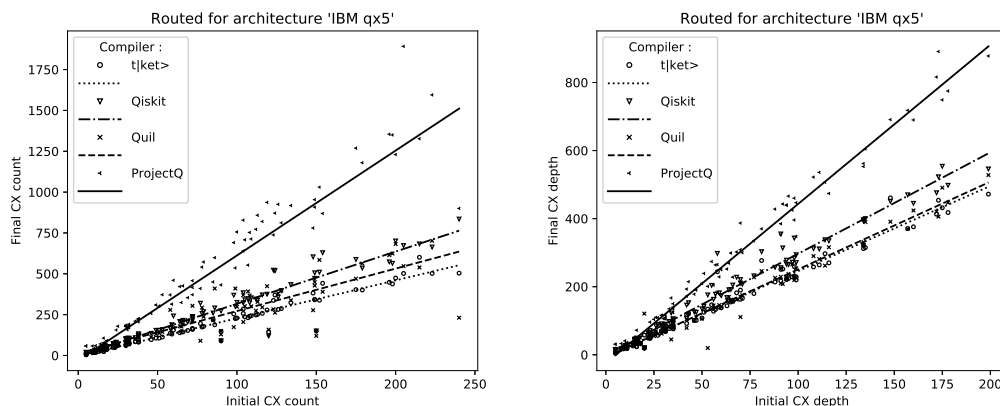
Name	g_{in}	d_{in}	Qiskit 0.7.0		Zulehner et al.		CQC's t ket>		t ket> comparison	
			g_{out}	d_{out}	g_{out}	d_{out}	g_{out}	d_{out}	r_{gate}	r_{depth}
urf3_279	125362	70702	—	—	440509	239702	406738	237181	0.92	0.99
plus63mod4096_163128744	72246	163128744	—	—	439981	243861	402395	243814	0.91	1.00
urf5_158	164416	89145	—	—	*	*	465129	284825		
urf6_160	171840	93645	—	—	580295	313011	541013	313653	0.93	1.00
urf1_149	184864	99585	—	—	*	*	525310	321185		
plus63mod8192_164187112	105142	164187112	—	—	640204	354076	585116	355168	0.91	1.00
hwb9_119	207775	116199	—	—	655220	375105	608175	369246	0.93	0.98
urf3_155	423488	229365	—	—	*	*	1211536	735676		
ground_state_esti-390180	245614	390180	—	—	520010	376695	12243	6804	0.02	0.02
mation_10										
urf4_187	512064	264330	—	—	1650845	878249	1487289	867091	0.90	0.99

g : the number of quantum gates (elementary operations), d : depth of the quantum circuits, — are time-outs and * are data not provided by the Zulehner et al.



■ **Figure 16** Routing comparison on ibmqx5, gate count and depth of the routed circuits when counting all gates. The upper charts are a zoomed in version of the initial segment of the lower charts. The results are averaged in bins when the initial count or depth is equal.

B.2 CX Only Comparison on ibmqx5



■ **Figure 17** Routing comparison on ibmqx5, CX count and CX depth when counting only CX gates. The charts are a zoomed in version of the initial segment of upper charts of Fig. 14.

■ **Table 5** CX gates only comparison on ibmqx5.

Name	g_{in}	d_{in}	Qiskit 0.7.0		Project Q 0.4.1		Quilc 1.1.1 Pyquil 2.1.1		CQC's t ket>		t ket> comparison	
			g_{out}	d_{out}	g_{out}	d_{out}	g_{out}	d_{out}	g_{out}	d_{out}	r_{gate}	r_{depth}
xor5_254	5	5	17	14	58	31	17	12	8	8	0.47	0.67
graycode6_47	5	5	5	5	5	5	5	5	5	5	1.00	1.00
ex1_226	5	5	20	16	58	31	17	12	8	8	0.47	0.67
4gt11_84	9	8	22	18	58	33	25	18	18	17	0.82	0.94
4mod5-v0_20	10	9	22	19	43	28	20	17	19	18	0.95	1.06
ex-1_166	9	9	19	19	18	18	27	21	18	18	1.00	1.00
4mod5-v1_22	11	10	29	27	60	41	29	21	23	22	0.79	1.05
mod5d1_63	13	11	37	29	48	36	40	28	25	22	0.68	0.79
ham3_102	11	11	24	22	20	20	24	20	18	18	0.90	0.90
4gt11_83	14	14	36	30	71	38	34	28	29	26	0.85	0.93
4gt11_82	18	18	42	33	91	50	43	34	36	33	0.86	1.00
rd32-v0_66	16	16	43	40	36	31	39	32	24	24	0.67	0.77
alu-v0_27	17	15	60	46	71	50	52	39	38	36	0.73	0.92
4mod5-v1_24	16	15	53	44	78	51	46	38	34	33	0.74	0.87
4mod5-v0_19	16	16	53	49	106	72	44	37	37	36	0.84	0.97
mod5mils_65	16	16	52	47	43	41	46	36	34	33	0.79	0.92
rd32-v1_68	16	16	47	40	36	31	36	29	24	24	0.67	0.83
alu-v1_28	18	16	52	44	42	36	50	40	39	37	0.93	1.03
alu-v2_33	17	15	53	45	72	51	52	39	35	33	0.67	0.85
alu-v4_37	18	16	51	43	49	43	53	40	39	37	0.80	0.93
alu-v3_35	18	16	55	45	49	43	54	40	39	37	0.80	0.93
3_17_13	17	17	47	47	41	41	50	39	35	35	0.85	0.90
alu-v1_29	17	15	51	42	71	50	51	38	38	36	0.75	0.95
milller_11	23	23	57	57	52	52	77	59	50	50	0.96	0.96
alu-v3_34	24	23	81	71	156	96	73	62	57	56	0.78	0.90

Name	g_{in}	d_{in}	Qiskit 0.7.0		Project Q 0.4.1		Quilc 1.1.1 Pyquil 2.1.1		CQC's $t ket\rangle$		$t ket\rangle$ comparison	
			g_{out}	d_{out}	g_{out}	d_{out}	g_{out}	d_{out}	g_{out}	d_{out}	r_{gate}	r_{depth}
decod24-v2_43	22	22	73	65	81	67	63	53	49	49	0.78	0.92
decod24-v0_38	23	23	62	56	88	65	66	52	48	48	0.77	0.92
mod5d2_64	25	25	70	61	179	104	63	55	61	60	0.97	1.09
4gt13_92	30	26	98	85	177	110	86	69	66	64	0.77	0.93
4gt13-v1_93	30	27	104	89	185	109	79	61	60	57	0.76	0.93
4mod5-v0_18	31	31	103	90	158	109	91	70	70	68	0.77	0.97
decod24-bdd_294	32	31	97	79	170	105	98	77	77	71	0.79	0.92
one-two-three- v2_100	32	29	96	83	191	116	69	62	71	71	1.03	1.15
one-two-three- v3_101	32	29	102	91	182	116	78	68	72	69	0.92	1.01
4mod5-v1_23	32	30	106	86	178	106	102	79	74	73	0.73	0.92
4mod5-bdd_287	31	31	106	83	170	115	100	76	82	75	0.82	0.99
rd32_270	36	35	109	92	210	124	101	82	84	82	0.83	1.00
4gt5_75	38	33	121	98	223	135	116	83	83	77	0.72	0.93
alu-bdd_288	38	35	122	96	206	140	124	90	95	88	0.78	0.98
alu-v0_26	38	35	125	103	224	135	115	80	83	78	0.72	0.97
decod24-v1_41	38	35	133	106	225	150	118	93	83	76	0.70	0.82
rd53_138	60	42	242	146	460	193	170	104	156	118	0.92	1.13
4gt5_76	46	42	135	107	257	172	112	79	97	92	0.87	1.16
4gt13_91	49	46	154	126	309	178	131	100	106	101	0.81	1.01
cnt3-5_179	85	43	260	153	450	215	216	121	219	121	1.01	1.00
qft_10	90	34	273	123	432	167	129	45	147	85	1.14	1.89
4gt13_90	53	50	158	135	372	210	144	106	113	108	0.78	1.02
alu-v4_36	51	47	154	125	303	190	136	110	106	101	0.78	0.92
mini_alu_305	77	53	320	176	410	201	–	–	196	134	0.61	0.76
ising_model_10	90	20	90	20	90	20	90	20	90	20	1.00	1.00
ising_model_16	150	20	150	20	150	20	150	20	150	20	1.00	1.00
ising_model_13	120	20	120	20	120	20	120	20	144	58	1.20	2.90
4gt5_77	58	51	165	143	371	239	158	121	136	125	0.86	1.03
sys6-v0_111	98	55	369	204	691	274	279	137	254	147	0.91	1.07
one-two-three- v1_99	59	56	187	163	314	205	174	135	131	128	0.75	0.95
one-two-three- v0_98	65	59	207	182	324	229	192	145	146	140	0.76	0.97
decod24-v3_45	64	57	208	178	422	264	177	146	139	133	0.79	0.91
4gt10-v1_81	66	60	215	174	426	250	179	138	144	138	0.80	1.00
aj-e11_165	69	63	205	168	354	252	190	141	153	144	0.81	1.02
4mod7-v0_94	72	66	239	205	372	228	217	160	162	157	0.75	0.98
alu-v2_32	72	64	225	191	416	269	211	157	165	157	0.78	1.00
rd73_140	104	68	384	228	640	302	304	170	257	182	0.85	1.07
4mod7-v1_96	72	65	234	192	458	299	205	162	160	155	0.78	0.96
4gt4-v0_80	79	71	268	207	572	300	218	162	178	166	0.82	1.02
mod10_176	78	70	257	211	541	309	238	175	174	163	0.73	0.93
0410184_169	104	70	323	221	828	387	293	171	284	190	0.97	1.11
qft_16	240	58	835	298	900	265	369	111	504	244	1.37	2.20

5:26 On the Qubit Routing Problem

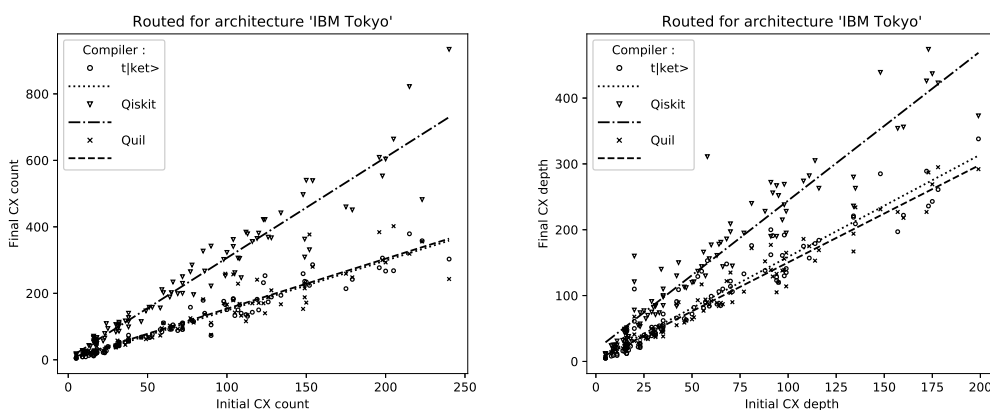
Name	g_{in}	d_{in}	Qiskit 0.7.0		Project Q 0.4.1		Quilc 1.1.1 Pyquil 2.1.1		CQC's $t ket\rangle$		$t ket\rangle$ comparison	
			g_{out}	d_{out}	g_{out}	d_{out}	g_{out}	d_{out}	g_{out}	d_{out}	r_{gate}	r_{depth}
4gt12-v0_88	86	77	291	232	599	335	231	182	188	180	0.81	0.99
rd84_142	154	81	629	303	869	370	410	228	442	277	1.08	1.21
rd53_311	124	92	519	314	871	443	390	246	370	252	0.95	1.02
4_49_16	99	91	300	256	536	353	262	208	226	217	0.86	1.04
sym9_146	148	91	604	355	780	385	410	229	382	251	0.93	1.10
4gt12-v1_89	100	88	325	257	756	428	277	210	229	214	0.83	1.02
4gt12-v0_87	112	94	345	266	772	440	298	226	248	221	0.83	0.98
4gt4-v0_79	105	94	341	278	708	439	274	223	236	222	0.86	1.00
hwb4_49	107	99	348	294	553	348	302	229	231	220	0.76	0.96
sym6_316	123	98	522	343	738	396	392	254	337	259	0.86	1.02
4gt12-v0_86	116	98	371	284	820	460	283	227	258	231	0.91	1.02
4gt4-v0_72	113	95	340	265	858	466	295	220	251	224	0.85	1.02
4gt4-v0_78	109	99	353	271	713	447	328	237	243	229	0.74	0.97
mod10_171	108	97	323	272	753	425	301	226	240	229	0.80	1.01
4gt4-v1_74	119	108	375	312	937	522	367	266	278	258	0.76	0.97
rd53_135	134	114	434	338	918	507	424	290	323	297	0.76	1.02
mini-alu_167	126	111	357	311	925	536	338	262	282	264	0.83	1.01
one-two-three- v0_97	128	116	397	335	812	474	380	281	287	270	0.76	0.96
ham7_104	149	134	506	393	954	562	397	316	343	312	0.86	0.99
decod24- enable_126	149	134	472	397	908	553	428	323	341	322	0.80	1.00
mod8-10_178	152	135	510	400	1030	605	449	331	338	315	0.75	0.95
cnt3-5_180	215	148	683	451	1327	691	585	390	601	461	1.03	1.18
ex3_229	175	157	588	470	1269	718	539	391	403	371	0.75	0.95
4gt4-v0_73	179	160	535	445	1180	690	470	370	401	376	0.85	1.02
mod8-10_177	196	178	573	498	1354	775	563	424	448	418	0.80	0.99
C17_204	205	173	673	523	1892	891	614	447	502	454	0.82	1.02
alu-v2_31	198	172	564	476	1350	816	547	406	438	413	0.80	1.02
rd53_131	200	175	701	554	1230	749	624	421	474	432	0.76	1.03
alu-v2_30	223	199	664	546	1595	878	682	491	502	472	0.76	0.96
mod5adder_127	239	208	793	633	1705	1022	702	528	533	499	0.76	0.95
rd53_133	256	221	805	640	1703	977	739	543	615	554	0.83	1.02
cm82a_208	283	234	1003	724	2092	1081	848	581	665	576	0.78	0.99
majority_239	267	232	932	704	1985	1102	805	581	624	568	0.78	0.98
ex2_227	275	241	965	737	1907	1107	789	584	656	603	0.83	1.03
sf_276	336	301	1104	902	2083	1290	935	743	762	727	0.81	0.98
sf_274	336	300	1095	878	2145	1287	922	686	757	725	0.82	1.06
con1_216	415	346	1454	1078	3593	1872	1288	891	1075	940	0.83	1.05
wim_266	427	352	1432	1058	3482	1823	1209	870	1089	951	0.90	1.09
rd53_130	448	383	1430	1132	3563	1905	1300	930	1099	976	0.85	1.05
f2_232	525	449	1796	1364	4409	2187	1563	1154	1309	1205	0.84	1.04
cm152a_212	532	461	1813	1374	5455	2557	1510	1078	1364	1221	0.90	1.13
rd53_251	564	492	1851	1474	5391	2555	1629	1221	1405	1268	0.86	1.04
hwb5_53	598	535	1850	1525	6201	2717	1713	1320	1360	1276	0.79	0.97
cm42a_207	771	634	2607	1926	8818	3910	2284	1600	1920	1691	0.84	1.06

Name	g_{in}	d_{in}	Qiskit 0.7.0		Project Q 0.4.1		Quilc 1.1.1 Pyquil 2.1.1		CQC's $t ket\rangle$		$t ket\rangle$ comparison	
			g_{out}	d_{out}	g_{out}	d_{out}	g_{out}	d_{out}	g_{out}	d_{out}	r_{gate}	r_{depth}
pm1_249	771	634	2713	2043	8818	3910	2220	1555	1920	1691	0.86	1.09
dc1_220	833	705	2895	2194	11741	4784	2351	1690	2077	1770	0.88	1.05
squar5_261	869	720	3015	2189	10135	4466	2676	1845	2358	1954	0.88	1.06
z4_268	1343	1112	4744	3473	22664	8032	4104	2870	3583	3059	0.87	1.07
sqrt8_260	1314	1121	4853	3633	22130	8209	4107	2937	3416	2985	0.83	1.02
radd_250	1405	1210	4952	3782	23920	8909	4290	3027	3768	3281	0.88	1.08
adr4_197	1498	1249	5284	3883	22303	8649	4538	3142	3871	3279	0.85	1.04
sym6_145	1701	1499	5356	4324	40194	11879	4910	3675	4170	3820	0.85	1.04
misex1_241	2100	1797	–	–	20756	10450	5798	4367	5578	4941	0.96	1.13
rd73_252	2319	1963	–	–	45433	15172	–	–	6007	5173	0.13	0.34
cycle10_2_110	2648	2276	–	–	50777	17976	–	–	7084	6316	0.14	0.35
hwb6_56	2952	2559	–	–	72955	21358	–	–	7125	6496	0.10	0.30
square_root_7	3089	2520	–	–	37275	16316	–	–	8928	7401	0.24	0.45
ham15_107	3858	3273	–	–	46860	21421	–	–	10206	8884	0.22	0.41
dc2_222	4131	3518	–	–	45200	21119	–	–	11545	10210	0.26	0.48
sqn_258	4459	3719	–	–	93394	29983	–	–	11425	9743	0.12	0.32
inc_237	4636	3928	–	–	39432	21180	–	–	12381	10872	0.31	0.51
cm85a_209	4986	4256	–	–	71744	29352	–	–	13297	11722	0.19	0.40
rd84_253	5960	4917	–	–	118473	40259	–	–	16027	13432	0.14	0.33
co14_215	7840	5759	–	–	84431	36897	–	–	22357	17144	0.26	0.46
root_255	7493	5965	–	–	128324	47123	–	–	20332	16951	0.16	0.36
mlp4_245	8232	6930	–	–	50107	31076	–	–	22759	19640	0.45	0.63
urf2_277	10066	8312	–	–	243218	71917	–	–	25127	21186	0.10	0.29
sym9_148	9408	8062	–	–	241725	73636	–	–	23489	20883	0.10	0.28
life_238	9800	8356	–	–	221220	72011	–	–	26064	22788	0.12	0.32
hwb7_59	10681	9112	–	–	264057	78857	–	–	26033	23163	0.10	0.29
max46_240	11844	9657	–	–	269243	84007	–	–	30709	25891	0.11	0.31
clip_206	14772	12028	–	–	213901	85381	–	–	40504	34045	0.19	0.40
9symml_195	15232	12849	–	–	–	–	–	–	40897	35349	–	–
sym9_193	15232	12849	–	–	–	–	–	–	40897	35349	–	–
sao2_257	16864	13209	–	–	–	–	–	–	46536	37963	–	–
dist_223	16624	13274	–	–	–	–	–	–	45230	37762	–	–
urf5_280	23764	19888	–	–	–	–	–	–	60233	51479	–	–
urf1_278	26692	22307	–	–	–	–	–	–	69370	58597	–	–
sym10_262	28084	23736	–	–	–	–	–	–	76180	65905	–	–
hwb8_113	30372	26041	–	–	–	–	–	–	77247	68560	–	–
urf2_152	35210	32247	–	–	–	–	–	–	84345	77320	–	–
urf3_279	60380	50568	–	–	–	–	–	–	158115	132770	–	–
plus63mod4096_16356329	48265	–	–	–	–	–	–	–	155209	135715	–	–
urf5_158	71932	64750	–	–	–	–	–	–	177757	158774	–	–
urf6_160	75180	67637	–	–	–	–	–	–	209231	174548	–	–
urf1_149	80878	72933	–	–	–	–	–	–	200949	179071	–	–
plus63mod8192_16481865	70222	–	–	–	–	–	–	–	226354	198162	–	–
hwb9_119	90955	77968	–	–	–	–	–	–	233049	205682	–	–
urf3_155	185276	167215	–	–	–	–	–	–	463538	409727	–	–

Name	g_{in}	d_{in}	Qiskit 0.7.0		Project Q 0.4.1		Quilc 1.1.1 Pyquil 2.1.1		CQC's t ket>		t ket> comparison	
			g_{out}	d_{out}	g_{out}	d_{out}	g_{out}	d_{out}	g_{out}	d_{out}	r_{gate}	r_{depth}
ground_state_es-154209151095 timation_10			–	–	–	–	–	–	5039	3897		
urf4_187	224028	185975	–	–	–	–	–	–	568938	481368		

g : the number of quantum gates (elementary operations),
 d : depth of the quantum circuits and – are time-outs

B.3 CX Only Comparison on IBM Tokyo



■ **Figure 18** Routing comparison on IBM Tokyo, CX count and CX depth when counting only CX gates. The charts are a zoomed in version of the initial segment of lower charts of Fig. 14.

■ **Table 6** CX gates only comparison on IBM Tokyo.

Name	g_{in}	d_{in}	Qiskit 0.7.0		Quilc 1.1.1 Pyquil 2.1.1		CQC's t ket>		t ket> comparison	
			g_{out}	d_{out}	g_{out}	d_{out}	g_{out}	d_{out}	r_{gate}	r_{depth}
xor5_254	5	5	14	11	7	7	5	5	0.71	0.71
graycode6_47	5	5	17	11	5	5	5	5	1.00	1.00
ex1_226	5	5	18	12	7	7	5	5	0.71	0.71
4gt11_84	9	8	27	24	15	14	9	8	0.60	0.57
4mod5-v0_20	10	9	25	19	16	15	19	18	1.19	1.20
ex-1_166	9	9	28	25	18	15	9	9	0.50	0.60
4mod5-v1_22	11	10	26	25	20	18	23	22	1.15	1.22
mod5d1_63	13	11	43	31	28	23	13	11	0.46	0.48
ham3_102	11	11	25	25	18	15	9	9	0.50	0.60
4gt11_83	14	14	41	32	20	20	17	16	0.85	0.80
4gt11_82	18	18	49	34	30	27	24	23	0.80	0.85
rd32-v0_66	16	16	57	43	21	20	12	12	0.57	0.60
alu-v0_27	17	15	63	48	53	34	20	19	0.38	0.56
4mod5-v1_24	16	15	66	49	28	27	16	15	0.57	0.56
4mod5-v0_19	16	16	67	51	25	25	25	25	1.00	1.00

Name	g_{in}	d_{in}	Qiskit 0.7.0		Quilc 1.1.1 Pyquil 2.1.1		CQC's $t ket\rangle$		$t ket\rangle$ comparison	
			g_{out}	d_{out}	g_{out}	d_{out}	g_{out}	d_{out}	r_{gate}	r_{depth}
mod5mils_65	16	16	71	48	28	28	25	25	0.89	0.89
rd32-v1_68	16	16	53	45	24	17	12	12	0.50	0.71
alu-v1_28	18	16	60	35	40	26	21	20	0.53	0.77
alu-v2_33	17	15	59	44	29	28	20	19	0.69	0.68
alu-v4_37	18	16	67	45	52	33	21	20	0.40	0.61
alu-v3_35	18	16	57	43	52	33	21	20	0.40	0.61
3_17_13	17	17	46	38	26	25	17	17	0.65	0.68
alu-v1_29	17	15	57	43	53	34	20	19	0.38	0.56
millier_11	23	23	65	53	32	29	23	23	0.72	0.79
alu-v3_34	24	23	109	74	37	36	27	27	0.73	0.75
decod24-v2_43	22	22	57	55	28	28	22	22	0.79	0.79
decod24-v0_38	23	23	79	57	27	25	21	21	0.78	0.84
mod5d2_64	25	25	94	77	38	38	40	40	1.05	1.05
4gt13_92	30	26	84	65	39	35	42	38	1.08	1.09
4gt13-v1_93	30	27	106	70	37	34	39	36	1.05	1.06
4mod5-v0_18	31	31	91	71	58	46	43	40	0.74	0.87
decod24-bdd_294	32	31	102	85	44	37	53	52	1.20	1.41
one-two-three- v2_100	32	29	86	75	46	41	53	52	1.15	1.27
one-two-three- v3_101	32	29	108	91	53	50	42	39	0.79	0.78
4mod5-v1_23	32	30	113	82	50	49	47	42	0.94	0.86
4mod5-bdd_287	31	31	103	84	46	39	43	43	0.93	1.10
rd32_270	36	35	117	98	45	38	54	53	1.20	1.39
4gt5_75	38	33	99	74	56	53	56	54	1.00	1.02
alu-bdd_288	38	35	140	110	65	45	74	72	1.14	1.60
alu-v0_26	38	35	115	85	56	48	57	56	1.02	1.17
decod24-v1_41	38	35	127	100	56	50	62	62	1.11	1.24
rd53_138	60	42	202	130	111	87	111	91	1.00	1.05
4gt5_76	46	42	115	84	67	55	68	66	1.01	1.20
4gt13_91	49	46	147	113	62	59	70	65	1.13	1.10
cnt3-5_179	85	43	327	150	182	90	179	109	0.98	1.21
qft_10	90	34	342	140	75	45	73	50	0.97	1.11
4gt13_90	53	50	158	120	67	64	77	72	1.15	1.12
alu-v4_36	51	47	158	112	67	62	67	63	1.00	1.02
mini_alu_305	77	53	265	137	125	93	158	129	1.26	1.39
ising_model_10	90	20	222	78	111	41	105	50	0.95	1.22
ising_model_16	150	20	540	160	172	31	234	110	1.36	3.55
ising_model_13	120	20	381	121	171	68	150	61	0.88	0.90
4gt5_77	58	51	156	121	73	67	91	82	1.25	1.22
sys6-v0_111	98	55	302	144	170	117	176	137	1.04	1.17
one-two-three-v1_99	59	56	211	166	95	77	84	81	0.88	1.05
one-two-three-v0_98	65	59	202	156	94	86	92	84	0.98	0.98
decod24-v3_45	64	57	189	130	103	94	92	90	0.89	0.96
4gt10-v1_81	66	60	234	177	100	92	105	99	1.05	1.08
aj-e11_165	69	63	199	161	93	89	88	87	0.95	0.98

5:30 On the Qubit Routing Problem

Name	g_{in}	d_{in}	Qiskit 0.7.0		Quilc 1.1.1 Pyquil 2.1.1		CQC's $t \text{ket}\rangle$		$t \text{ket}\rangle$ comparison	
			g_{out}	d_{out}	g_{out}	d_{out}	g_{out}	d_{out}	r_{gate}	r_{depth}
4mod7-v0_94	72	66	200	144	97	87	111	110	1.14	1.26
alu-v2_32	72	64	250	178	92	84	109	106	1.18	1.26
rd73_140	104	68	341	186	179	122	182	148	1.02	1.21
4mod7-v1_96	72	65	230	181	100	89	91	85	0.91	0.96
4gt4-v0_80	79	71	196	145	112	90	115	106	1.03	1.18
mod10_176	78	70	285	197	120	104	118	114	0.98	1.10
0410184_169	104	70	362	209	257	135	184	122	0.72	0.90
qft_16	240	58	934	311	243	90	303	153	1.25	1.70
4gt12-v0_88	86	77	267	195	137	106	140	133	1.02	1.25
rd84_142	154	81	539	240	280	172	286	176	1.02	1.02
rd53_311	124	92	422	256	–	–	253	191	0.60	0.75
4_49_16	99	91	253	190	140	129	166	162	1.19	1.26
sym9_146	148	91	497	272	259	177	259	200	1.00	1.13
4gt12-v1_89	100	88	323	228	153	139	151	138	0.99	0.99
4gt12-v0_87	112	94	384	267	166	152	136	123	0.82	0.81
4gt4-v0_79	105	94	262	190	116	105	133	128	1.15	1.22
hwb4_49	107	99	306	228	142	133	150	141	1.06	1.06
sym6_316	123	98	422	269	229	165	232	192	1.01	1.16
4gt12-v0_86	116	98	356	238	170	156	143	130	0.84	0.83
4gt4-v0_72	113	95	379	252	170	139	131	120	0.77	0.86
4gt4-v0_78	109	99	247	195	135	120	140	135	1.04	1.12
mod10_171	108	97	305	215	133	114	165	161	1.24	1.41
4gt4-v1_74	119	108	365	274	168	138	182	175	1.08	1.27
rd53_135	134	114	442	305	241	186	194	179	0.80	0.96
mini-alu_167	126	111	369	282	167	153	174	157	1.04	1.03
one-two-three-v0_97	128	116	367	263	188	175	189	184	1.01	1.05
ham7_104	149	134	309	236	209	169	236	221	1.13	1.31
decod24-enable_126	149	134	363	280	215	194	227	219	1.06	1.13
mod8-10_178	152	135	331	263	188	167	224	209	1.19	1.25
cnt3-5_180	215	148	822	439	377	234	379	285	1.01	1.22
ex3_229	175	157	460	354	319	231	214	197	0.67	0.85
4gt4-v0_73	179	160	451	356	259	227	242	222	0.93	0.98
mod8-10_177	196	178	609	423	248	218	277	261	1.12	1.20
C17_204	205	173	664	474	384	295	268	236	0.70	0.80
alu-v2_31	198	172	553	426	402	287	306	289	0.76	1.01
rd53_131	200	175	604	437	300	227	267	243	0.89	1.07
alu-v2_30	223	199	482	373	293	269	358	338	1.22	1.26
mod5adder_127	239	208	650	476	356	292	311	288	0.87	0.99
rd53_133	256	221	703	499	359	308	348	328	0.97	1.06
cm82a_208	283	234	914	607	393	317	451	391	1.15	1.23
majority_239	267	232	720	528	402	328	348	311	0.87	0.95
ex2_227	275	241	886	648	443	371	416	391	0.94	1.05
sf_276	336	301	989	731	372	340	489	453	1.31	1.33
sf_274	336	300	863	643	457	391	357	328	0.78	0.84
con1_216	415	346	1389	916	659	486	736	626	1.12	1.29
wim_266	427	352	1145	793	763	501	772	688	1.01	1.37

Name	g_{in}	d_{in}	Qiskit 0.7.0		Quilc 1.1.1 Pyquil 2.1.1		CQC's $t ket\rangle$		$t ket\rangle$ comparison	
			g_{out}	d_{out}	g_{out}	d_{out}	g_{out}	d_{out}	r_{gate}	r_{depth}
rd53_130	448	383	1242	899	695	547	646	608	0.93	1.11
f2_232	525	449	1443	1069	722	621	854	772	1.18	1.24
cm152a_212	532	461	1491	1051	805	633	793	717	0.99	1.13
rd53_251	564	492	1487	1058	960	659	805	715	0.84	1.08
hwb5_53	598	535	1568	1179	941	765	808	757	0.86	0.99
cm42a_207	771	634	2333	1593	1411	996	1102	968	0.78	0.97
pm1_249	771	634	2303	1574	1411	996	1102	968	0.78	0.97
dc1_220	833	705	2450	1715	1532	1049	1436	1261	0.94	1.20
squar5_261	869	720	2902	1948	1463	1063	1631	1372	1.11	1.29
z4_268	1343	1112	4185	2828	2282	1632	2235	1914	0.98	1.17
sqrt8_260	1314	1121	4079	2846	2406	1665	2235	1964	0.93	1.18
radd_250	1405	1210	4346	3050	–	–	2697	2361	0.62	0.77
adr4_197	1498	1249	4584	3110	2333	1720	2737	2368	1.17	1.38
sym6_145	1701	1499	4872	3517	2554	2042	2301	2145	0.90	1.05
misex1_241	2100	1797	–	–	3249	2435	4291	3760	1.32	1.54
rd73_252	2319	1963	–	–	3854	2798	3748	3276	0.97	1.17
cycle10_2_110	2648	2276	–	–	4511	3463	4342	3802	0.96	1.10
hwb6_56	2952	2559	–	–	4405	3575	4205	3904	0.95	1.09
square_root_7	3089	2520	–	–	4967	3427	5790	4833	1.17	1.41
ham15_107	3858	3273	–	–	6649	4828	6485	5605	0.98	1.16
dc2_222	4131	3518	–	–	–	–	7694	6708		
sqn_258	4459	3719	–	–	–	–	6863	5984		
inc_237	4636	3928	–	–	–	–	8274	7176		
cm85a_209	4986	4256	–	–	–	–	8166	7093		
rd84_253	5960	4917	–	–	–	–	9506	8154		
co14_215	7840	5759	–	–	–	–	14415	11195		
root_255	7493	5965	–	–	–	–	11971	9940		
mlp4_245	8232	6930	–	–	–	–	15156	13061		
urf2_277	10066	8312	–	–	–	–	17367	15384		
sym9_148	9408	8062	–	–	–	–	13893	12321		
life_238	9800	8356	–	–	–	–	15944	13926		
hwb7_59	10681	9112	–	–	–	–	17655	15828		
max46_240	11844	9657	–	–	–	–	19519	16979		
clip_206	14772	12028	–	–	–	–	25499	21345		
9symml_195	15232	12849	–	–	–	–	24532	21295		
sym9_193	15232	12849	–	–	–	–	24532	21295		
sao2_257	16864	13209	–	–	–	–	28799	23847		
dist_223	16624	13274	–	–	–	–	27953	23342		
urf5_280	23764	19888	–	–	–	–	41610	36329		
urf1_278	26692	22307	–	–	–	–	46023	40020		
sym10_262	28084	23736	–	–	–	–	44383	38132		
hwb8_113	30372	26041	–	–	–	–	50008	44245		
urf2_152	35210	32247	–	–	–	–	58307	53905		
urf3_279	60380	50568	–	–	–	–	105870	91838		
plus63mod4096_163	56329	48265	–	–	–	–	95107	82375		
urf5_158	71932	64750	–	–	–	–	122288	110318		

5:32 On the Qubit Routing Problem

Name	g_{in}	d_{in}	Qiskit 0.7.0		Quilc 1.1.1 Pyquil 2.1.1		CQC's $t ket\rangle$		$t ket\rangle$ comparison	
			g_{out}	d_{out}	g_{out}	d_{out}	g_{out}	d_{out}	r_{gate}	r_{depth}
urf6_160	75180	67637	–	–	–	–	141416	120999		
urf1_149	80878	72933	–	–	–	–	137791	123873		
plus63mod8192_164	81865	70222	–	–	–	–	145872	125957		
hwb9_119	90955	77968	–	–	–	–	149106	131678		
urf3_155	185276	167215	–	–	–	–	317732	285000		
ground_state _esti- mation_10	154209	151095	–	–	–	–	1015	776		
urf4_187	224028	185975	–	–	–	–	385355	330368		

g : the number of quantum gates (elementary operations),

d : depth of the quantum circuits and – are time-outs.