Investigation of the Impact of Interoperability of Voltage Source Converters on HVDC Grid Fault Behaviour

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Abstract

Future HVDC grids are expected to incorporate different power converters from multiple vendors in the same system. Even if a complete converter station is developed by a single manufacturer, it might be challenging to integrate this terminal into a DC grid that comprises of several converter stations built by other vendors. Moreover, the different fault response exhibited by each converter technology complicates the design of HVDC protection systems. Therefore, this study investigates the fault response of a multivendor HVDC grid. An illustrative 4-terminal meshed HVDC grid, which is modelled in PSCAD environment, is used to perform studies of interoperability of different converter topologies on a common HVDC network. The investigation of the fault behaviour of such a multivendor HVDC network highlights the main impediments that need to be tackled and a set of actions that needs to be done at a converter level in order to mitigate the impact of DC faults on the HVDC system. Moreover, the key parameters that need to be taken into account when designing a protection scheme for a multivendor HVDC grid are identified.

1 Introduction

High Voltage Direct Transmission (HVDC) systems have proven to be an attractive option for bulk power transfer over long distances, facilitating the integration of large offshore wind farms dispersed over wide geographical areas and the interconnection with the onshore AC grids. To date, most HVDC systems are using Line Commutated Converter (LCC) technology; however, in recent years, Voltage Source Converter (VSC) technology has become the preferred option due to the fact that it offers a plethora of advantages such as better reliability, flexibility and controllability at relatively lower cost and losses, and the capability to interconnect asynchronous AC networks [1]. HVDC grids could be considered as the natural evolution of existing point-to-point links and is expected to be mostly modular. HVDC grids are perceived to offer better reliability, security, redundancy and economic and technologic advantages to the conventional AC grids.

The major challenge towards the realisation of HVDC grids to date is the absence of cost-effective DC protection systems and switchgears [2]. Owing to the very high rate of rise of the fault currents and the under-voltages during DC faults, DC protection and control systems are characterised by more stringent requirements in terms of speed, selectivity, sensitivity and reliability [3]. Without adequate control and protection solutions, converter stations can block their operation, resulting in interruption of large power transfer between the HVDC grid and the surrounding AC networks. DC grids can be more complex when different converter topologies are incorporated. This is because such different converters employ different control strategies, exhibit different transient response, and have different means of surviving and riding through DC faults.

To date, most HVDC systems are built by a single manufacturer. However, as HVDC grids gain more attention, their scale is expected to become increasingly larger and hence their implementation will necessitate the involvement of multiple vendors as in the case of large-scale AC power systems. The use of different converter topologies should not compromise the overall functionality of the grid, which must remain statically and dynamically stable regardless of which control concept is applied to each station [4]. Hence, the main challenge at this point, is to achieve interoperability of the various converter technologies with the ultimate aim to operate the grid reliably and securely under all network conditions, including DC faults. This is a major challenge that needs to be addressed in order to enhance the applicability, the maturity, the modularity, and flexibility of HVDC grids.

The significance of a multivendor solution for future HVDC grids has been highlighted in [5]. The technical feasibility of incorporating different converter technologies into a single HVDC grid has been proven in [6]. However, the fault behaviour of a multivendor HVDC grid has not been comprehensively studied yet. Therefore, this paper aims to investigate the impact of interoperability of VSC converters on HVDC grid fault behaviour in order to highlight the protection requirements of such a multivendor grid. The paper is structured as follows. In Section 2, the fault behaviour of different VSC converters is explained. Section 3 presents the HVDC test network that is used for the simulation studies performed in Section 4. The main findings are discussed in Section 5 and conclusions are drawn in Section 6.

2 Fault Behaviour of VSC Converters

This section discusses different VSC topologies which are likely to be employed in future HVDC grids and their respective fault behaviours during a pole-to-pole DC fault. Pole-to-

pole DC faults occur as a result of insulation breakdown or direct contact between the negative and positive conductors of a DC line. Although a pole-to-pole DC fault presents a low probability of occurrence, it is one of the most severe faults that can happen in an HVDC system and therefore the fault response of each converter during this fault should be investigated.

2.1 Two-level Converter

The two-level converter is widely used in the first generation of point-to-point VSC-based HVDC transmission links. A two-level converter composes of six arms, that employ Insulated Gate Bipolar Transistors (IGBTs), with each pair of arms constituting a phase leg. To enable operation at high voltage, a large number of IGBTs must be connected in series to ensure even voltage sharing between individual IGBTs during turn-on and turn-off. Pulse width modulation (PWM) is usually adopted to control the gate signals of the IGBTs for reduced filtering requirements and better dynamic performance. Large physical volume and relatively high conversion losses are the main limitations of this converter. Moreover, the DC link capacitor that maintains a constant DC voltage gives rise to a significant discharge current during DC faults. Two-level converters are defenceless against DC faults because when the IGBTs are turned off to protect the from overcurrent, it operates as an uncontrolled rectifier. The fault response of the two-level converter is characterised by three stages [7].

Stage A: DC capacitor discharge. This stage represents the natural response of the two-level converter to a pole-to-pole DC short circuit fault. The discharge of the DC-link capacitor is associated with a large transient discharge current that increases rapidly and can reach very high peaks.

Stage B: Diode freewheeling. Following the DC voltage collapse, the cable impedance forces the fault current to commutate to the anti-parallel diodes. During this stage, each converter leg carries one third of the total DC fault current. This is the most hazardous phase for the diodes.

Stage C: Grid current feeding. In this stage, the blocked converter behaves as an uncontrolled rectifier, injecting a steady-state fault current. The line inductor starts to contribute, and an R-L-C circuit is formed that presents a forced response in the form of an AC current source.

2.2 Half-bridge MMC Converter

Some of he limitations of two-level converters were overcome with the advent of Modular Multi-level Converters (MMC). The fundamental component of MMCs is the sub-module (SM), which consists of semiconductor switches that can be arranged in various topologies, such as half-bridge, full-bridge etc. The Half-bridge (HB) MMC converter has evolved into the preferred technology for new HVDC systems. A central DC link capacitor is no longer needed since the total capacitance is distributed among the sub-modules. During a fault, the distributed SM capacitors could be quickly bypassed and therefore the capacitor discharge from the converter is avoided. Because of the limited discharge of the capacitors during a fault, the grid restoration time could be greatly reduced. Similarly, three stages can be distinguished for the half-bridge MMC. Unlike the two-level converter, half-bridge MMC does not have a DC-link capacitor and therefore the first stage differs.

Stage A: SM capacitors discharge. This stage takes place after the fault is seen by the converter until the time the converter blocks, causing the turn-off of the IGBTs. During this transient phase, which is in the order of tens of microseconds, the inserted sub-module capacitors discharge into the fault. Given that a sorting algorithm for the SMs is integrated in the control system of the converter, all SM capacitances are exposed to some extent.

Stage B: Diode freewheeling. This stage initiates once the converter is blocked. At this time, the SM capacitors are bypassed and the current flows into the fault through the antiparallel diodes, leaving all three AC phases exposed to reduced load impedance and consequently, the AC current rises. The arm and cable inductance play a significant role in this stage [8].

Stage C: Grid current feeding. This stage starts when the current flowing through three of the converter arms has decayed to zero. At this stage, the total DC fault current is contributed by the interconnected AC grid. The fault current reaches a steady-state value determined by the strength of the AC grid, the converter transformer impedance, the arm reactors, the inductive cable termination and the distance to the fault.

2.3 Fault-blocking Converters

Towards the aim of preventing the uncontrolled grid infeed to DC faults, converter topologies that can block or control the DC fault current have been proposed, such as the full-bridge (FB) MMC converter [9]. FB MMC converter can produce both positive and negative voltage and remain operational during a pole-to-pole DC fault. The voltage of the submodules can be modulated to oppose the fault current flow. This feature of DC fault blocking capability can be exploited to improve the HVDC grid fault behaviour. Other topologies that demonstrate the same feature have also been proposed [10, 11]. However, most fault-blocking converters use additional switching devices per SM, thus increasing conversion losses and total cost of the converter.

3 HVDC Test Network

This paper uses the four-terminal HVDC grid shown in Figure 1, to investigate the impact of the interoperability of different VSC converters on the DC grid fault behaviour. This test grid was designed based on a hypothetical, yet realistic scenario that the HVDC grid is formed by gradual extension of existing HVDC systems. Converters 1 and 2 (C1 and C2) are two-level converters that represent a point-to-point link that was originally built for the power transfer from the offshore wind farm, with converter C2 connected to the onshore AC grid. Similarly, converters C3 and C4 are two HB-MMC converters that represent a point-to-point link that was designed at a later stage. Finally, the multivendor HVDC grid is formed through the interconnection of the two point-to-point links. The drivers behind the development of such HVDC grid could be the increased reliability and flexibility and the ability of asynchronous AC

grids to access power from wind farms regardless of their locations. The AC networks are designed to have a short-circuit ratio (SCR) equal to 10. The DC grid can be either considered as embedded within the same AC grid or as a means of interconnection between two separate AC networks.

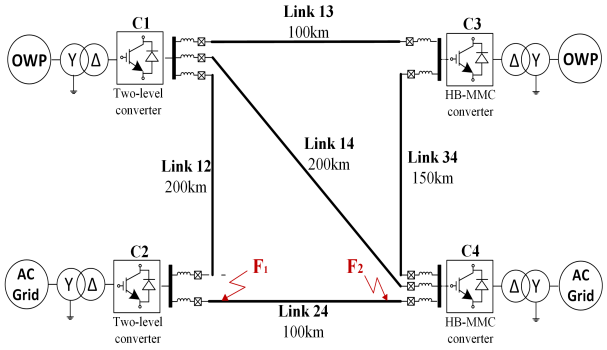

Figure 1: Multivendor HVDC test grid model.

The test system is modelled with the EMTDC/PSCAD simulation tool. The network architecture and the cable parameters are adapted from [12]. The network is operating at ±320kV DC in a symmetric monopolar configuration. All the DC lines are modelled as frequency-dependent cables, using the available cable model in PSCAD library. The modelling approach for the MMC converters is based on average value modelling, with the appropriate modifications to accurately represent the converter behaviour during the blocking state [13]. The converters are programmed to trip when the current flow through the IGBT devices exceeds two times the rated current. DC circuit breakers (DCCBs) are included at the end of each DC line. The current breaking time of the CBs can be adjusted according to the breaker technology that is used. The main parameters of the converters are summarised in table 1.

Table 1: VSC converter parameters.

Parameters	Two-level converters	HB-MMC converters
Nominal DC voltage [kV]	± 320	± 320
Rated apparent power [MVA]	1000	1200
Rated AC output voltage [kV]	360	360
DC-link capacitor [μF]	50	-
Arm inductance [mH]	-	4
SM capacitance [μF]	-	31.28
DC bus filter [mH]	5	5

Converters C1 and C3 are configured to control the active power of the offshore wind farms, while converters C2 and C4 employ voltage droop control in order to regulate the DC system voltage. The same droop constant is used, resulting in equal power sharing amongst the two converters. In the pre-fault stage, converter C1 and C3 are configured to regulate the active power at 700MW respectively, converter C2 is set to export 800MW to the neighbouring AC grid and converter C4 is set to export 600MW.

4 Multivendor HVDC Grid Fault Analysis

4.1 HVDC Grid Fault Response

This study is performed in the absence of any protection systems in order to investigate the natural response of the system during a permanent pole-to-pole fault. Pole-to-pole faults have been selected for the simulation studies due to their severity. To assess the biggest impact a fault can have on the surrounding AC networks, the investigated fault locations (shown in Figure 1) are chosen to be on the line connecting the two AC grid connected terminals that are responsible for voltage regulation. In particular, faults F1 and F2 occur at 5km and 95km of line 24 respectively. When a fault occurs, travelling waves start to travel along the cable to both directions from the fault location. As a travelling wave travels along the cable, it induces the discharge of the distributed capacitance of the associated cable. When it reaches a discontinuity, such as a converter terminal, part of the wave is reflected back to the fault location and part of it is transmitted to other cables connected at the same terminal. The same procedure happens when the transmitted waves reach the other terminals. Once a travelling wave reaches a two-level converter, the DC-link capacitor starts to discharge, while a travelling wave that reaches a HB-MMC results in the discharge of the sub-module capacitors until the converter is blocked.

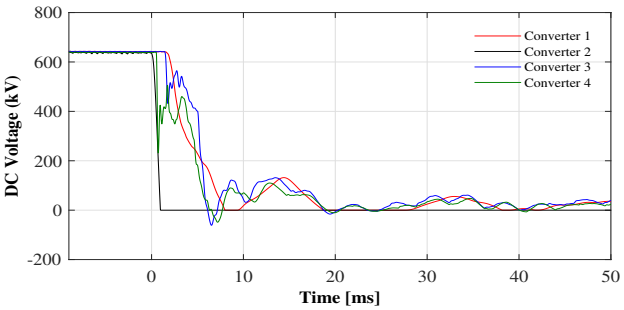

Figure 2: Converter voltages during fault F1.

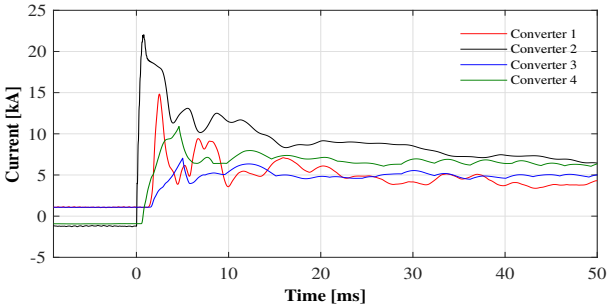

Figure 3: Converter fault current contributions to fault F1.

DC bus voltages at converter terminals are illustrated in Figure 2 following a fault that occurs at 0s at location F1. The system voltage collapses in 5-6ms after fault inception. The voltages at the converters terminals closer to the fault (C2 and C4) drop first within 4ms and converter 1 & 3 voltages collapse a few ms later after the arrival of the travelling waves at the terminals. While the voltage at two-level converters drops very quickly, the voltage at the MMC-based terminals collapses following converter blocking. The corresponding converter fault current

contributions are shown in Figure 3. From the converters voltage and current responses, the three stages that were described in section 2 can be distinguished. At first, all converters present a steep current increase during the first stage. Then the second stage initiates once the converters are blocked (the voltage at each terminal drops rapidly following converter blocking) and the current flows through the freewheeling diodes and lastly, the fault currents reach a steady-state value at stage three. Converter C2 demonstrates the highest peak current and the highest rate of rise of current, since it is the converter closer to the fault. The currents start to increase at different times due to the time it takes for the travelling waves to reach each terminal.

It is worth noting that converter C1 demonstrates a higher initial rate of rise of current compared to converter C4, despite being further from the fault. This is attributed to the fact, that when converter C4 blocks, further discharge from the distributed sub-modules' capacitors is inhibited. On the contrary, the two-level converter C1 is defenceless against the DC fault, since the DC-link capacitor discharge cannot be contained, thus leading to high rate of rise of current and high peak current even for distant faults. Moreover, the series connection of SM capacitors decreases the total capacitance limiting the initial current surge. As a result of these phenomena, converter C1 blocks on overcurrent before the HB-MMC converters. It can be concluded that the integration of two-level converters in a multi-vendor HVDC grid poses additional limitations to the protection systems in terms of the timescales within which they are required to operate.

4.2 Impact of DC Reactor

Converter blocking is needed to primarily to protect the power electronic devices. In the case of HB-MMC converters, converter blocking also avoids further discharge of the SM capacitors that can affect the proper function of the control system and deteriorate post-fault restoration time. The natural system fault response analysis demonstrated that MMC converters do not experience a sudden voltage drop until the moment they are blocked. Therefore, it is crucial to delay the converter blocking for as long as possible. Towards this aim, it has been widely proposed in the literature to use current limiting DC reactors at each cable ends to limit the magnitude and the initial rate of rise of the fault current, thus prolonging the time before the converter blocks.

The impact of inductance on converters C2 and C4 fault currents for different values of the DC reactor for fault F1 is illustrated in Figure 4 and 5 respectively, when DC reactors are placed at each cable end. It is observed that the higher the size of the series DC reactor, the larger the reduction in the fault current magnitude and the slower the rate of rise of current for both converters. It is remarkable that even a small DC reactor can produce a great impact on the fault current of the two-level converter. However, as the value of the inductance increases, the impact is lessened. Likewise, in Figure 6, the DC bus voltage at C4 terminal is displayed for different DC reactor values. The reactor affects both the initial voltage drop due to the arrival of the first incident travelling wave and the time the converter blocks its operation. In particular, an increase in the inductance causes a lower initial voltage drop and an increase in the converter blocking time. The latter feature is of vital importance for the protection systems, because it provides additional valuable time for fault detection and discrimination.

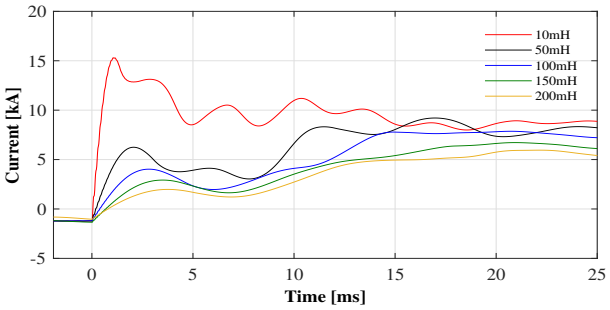

Figure 4: C2 fault currents for different DC reactor sizes.

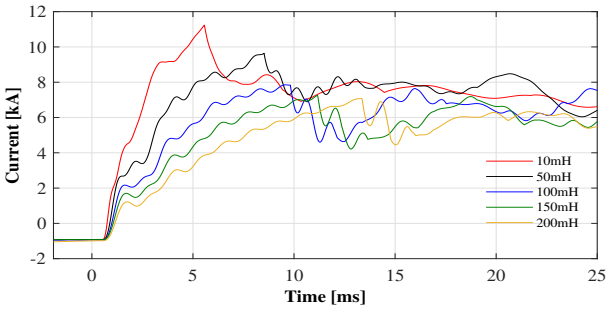

Figure 5: C4 fault currents for different DC reactor sizes.

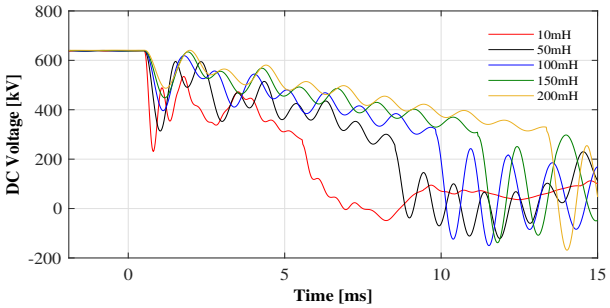

Figure 6: C4 voltage for different DC reactor sizes.

4.3 Impact of Breaking Speed

From the fault analysis, it has been demonstrated that all converters trip in less than 5ms after fault inception. Therefore, in order to minimize the impact of the fault and the disturbance to the neighbouring AC networks, a fast protection strategy is required. Moreover, the protection systems should be selective and trigger only for the faults that lie within their protection zone, while remain idle for faults outside their zone. Selectivity can be achieved by placing HVDC breakers at each end of each DC line to facilitate the isolation of a fault. The required fault clearance time depends on how stringent the requirements are for the adjacent AC grids. In this section, the impact of different breaker opening times is assessed for faults F1 and F2. A fast fault detection time is assumed ($\sim$0.5ms) and 50mH current limiting inductors are used in each cable end.

Table 2: Converter outages for different breaking times.

Fault	Breaking Time	C1	C2	C3	C4
F1	2 ms	No block	No block	No block	No block
	4 ms	Block	Block	No block	No block
	6 ms	Block	Block	Block	Block
F2	2 ms	No block	No block	No block	No block
	4 ms	No block	No block	No block	Block
	6 ms	Block	Block	Block	Block

Table 2. describes which converters block their operation by turning off their IGBTs and which remain operational in each fault case. A 2ms breaker operating time is fast enough to prevent all converters from blocking for both fault locations, while 6ms is very slow leading to all converters switching off the IGBTs. For 4ms operating time, fault F1 leads to the outage of the closest converters C2 and C4, as well as the outage of 2-level converter C2. While for a fault closer to the MMC converter C4, only the converters connected to the faulted line are blocked. The results highlight that the use of fast HVDC breakers is required in order to ensure that all converters retain their operation during faults. It is worth noting that hybrid HVDC breakers have been reported to achieve fault current interruption in the range of 2-5ms [14]. Moreover, the placement of faster HVDC breakers is advisable at the cable ends, which are connected at two-level converter terminals.

4.4 HVDC System Restoration

The power transfer between the DC grid and the AC networks should be restored as quickly as possible in order to minimize the effects of the disturbance to the AC network in terms of system frequency, rotor angle stability etc. Figure 7 illustrates the voltage recovery process after the application of fault F1, when the system relies on a selective strategy based on HVDC breakers with 2ms opening time following fault detection and series DC reactors (50mH) at each line end. The voltage recovers within ± 5 of the steady-state value within 100ms. Two-level converters demonstrate larger post-fault voltage oscillations.

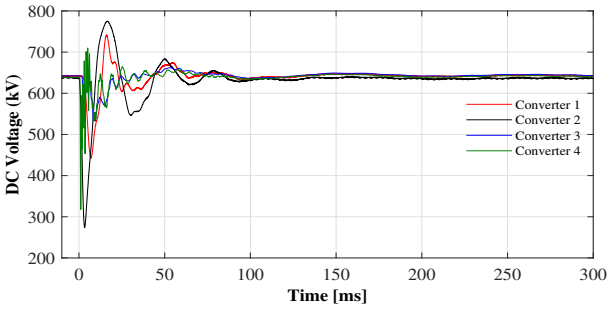

Figure 7: Converter voltages during fault.

The transferred active and reactive power of each converter are demonstrated in Figure 8. The negative sign in power indicates that power is exported from the DC system to the AC networks. Power-controlled converters experience minimal disturbance during the fault, while converters regulating the DC voltage (which are closer to the fault) experience a prolonged power disruption. The active power exchange with the AC grids is completely restored after 120ms.The restart sequence of the converters can play a significant role. In this analysis, no particular sequence has been applied and each converter retrieves normal operation once the fault current has been extinguished. In a larger grid, an appropriate restart sequence might be necessary in order to ensure the quickest restoration possible.

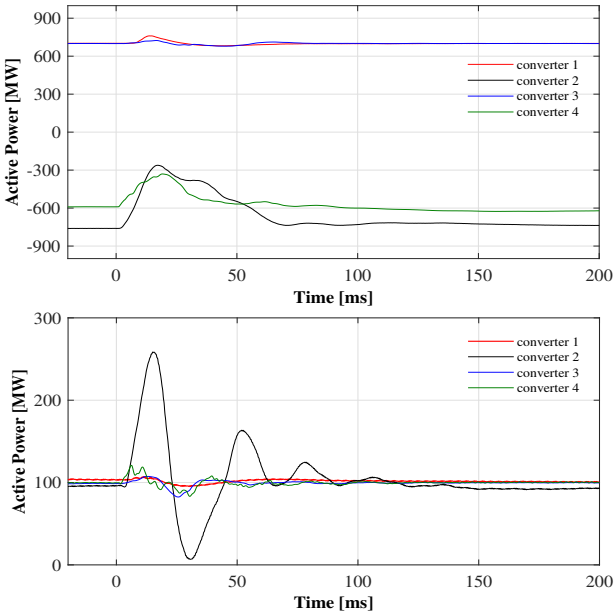

Figure 8: Active and Reactive power during the fault.

5 Discussion

The analysis demonstrated that a DC fault in a multivendor HVDC grid propagates along the whole system within a few ms after fault inception. Two level converters, owing to their high fault current contributions, introduce stringent requirements regarding fault clearing times. Hence, HVDC protection systems should be fast and selective to avoid disconnection of healthy parts. Given the large cable lengths that will most likely be involved in future HVDC grids, DC fault detection algorithms that are dependent only on local measurements will be preferred over communication-based algorithms unless the communication scheme is sufficiently fast.

In a multivendor grid that contains 2-level converters, the converter blocking times could be significantly shorter due to high discharge currents from large DC link capacitors. The length of converter blocking times under the most severe DC fault conditions should determine the current breaking time of the HVDC breakers. However, incorporation of sizeable DC reactors can extend converter blocking times. Moreover, the selection of an appropriate DC reactor allows for the breaker to act within their operation time before the maximum current breaking capability is exceeded. Thus, the size of DC reactors should be selected in conjunction with the appropriate HVDC breaker technology and their associated operation time. In the presence of a fast-selective protection strategy and sufficiently large DC reactors, the conditions under which a converter blocks can be readjusted accordingly in order to allow for the timely operation of the

protection systems while also ensuring security of supply. In addition, different protection switchgear, such as DCCBs with shorter current breaking times can be used at terminals with VSC converters that are more vulnerable to DC faults, such as two-level converters.

The impact of the duration of the recovery period after a fault depends on the size of the HVDC grid and the number of embedded AC networks. The AC network might be able to accommodate the complete permanent loss of a small HVDC grid, which can be considered as N-1 event for which the network is designed to withstand. However, a fault in a large HVDC grid can result in a large temporary loss of power for which the surrounding grids may not be in a position to tolerate. The amount of maximum allowed power loss strongly depends on the duration of the recovery period and the strength and inertia of the affected AC grids. Hence, it is important that a set of requirements is formed by network operators in terms of the maximum duration and the amount of loss of power infeed that can be tolerated due to temporary stop of the HVDC grid. In this way, the fault clearing strategy and the overall aims of the protection systems can be determined.

As of yet, the HVDC grid concept is in its infancy and there is no standardisation regarding requirements about the voltage level, the control and protection principles etc. The determination of such functional requirements will pave the way for the development of the specifications on the equipment that HVDC grids will contain. Recently, several international standardisation bodies and independent groups have highlighted the necessity for the standardisation of the HVDC systems. CIGRE working groups [2], the European HVDC study group [4] and CENELEC [15] have worked on standards and technical guidelines for HVDC and although these are very important steps towards standardisation, there is still a long way to go.

6 Conclusions

This paper investigated the impact of interoperability of different VSC converters on HVDC grid fault behaviour. A realistic scenario was presented on how a multivendor HVDC grid can be formed from the expansion of existing point-to-point links, which are based on different converter technologies. The higher overcurrents demonstrated by two-level converters shorten significantly the available time window for successful fault clearance by the circuit breakers. It was shown that even when fast acting breakers are used, the power restoration period may be relatively long for the AC grids to tolerate.

The analysis performed in this paper forms a basis towards the design of the HVDC protection systems that should be realised by considering and harmonising the requirements for the DCCB current breaking time, the size of DC reactors and the converter blocking criteria. Moreover, it was recommended that the selection of the appropriate protection equipment at each terminal should differ depending on the converter technology used. In particular, the vulnerability of two-level converters to DC faults indicates the need for faster protection systems compared to the ones used for MMC converters integrated within the same HVDC grid. Finally, emphasis was called on the importance of aligning the requirements that the grid operators might form, in an effort to facilitate the development of multivendor HVDC grids, with the objectives of the fault clearing strategy.

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