

Hybrid Converter Topologies for dc Transmission Systems

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Abstract: this paper presents two hybrid converters with reduced power circuit complexity compared to the mixed cell modular multilevel converter (MC-MMC). The proposed converters (refer to as types 1 and 2), with the type 1 converter is formed by replacing the director switch in each arm of the conventional alternate arm converter by high-voltage half-bridge cell, rated at half of the dc link voltage. Also, the type 1 converter resembles special case of MC-MMC, where the entire half-bridge cells of each arm are replaced by a single high-voltage half-bridge cell, with both capacitors of the half and full bridge cells are exposed to fundamental current as in the conventional MMC. The upper and lower arms of the type 2 converter resemble a front-to-front connection of two three-phase hybrid cascaded two-level converters, where the cell capacitors of the three-phase two-level converters that act as director switches in the upper and lower arms do not experience fundamental currents. Thus, the type 2 converter is expected to offer substantial reduction in footprint compared to type 1 converter and the MC-MMC. The technical viability of the proposed hybrid converters are assessed using simulations, with both converters are modelled in MATLAB-SIMULINK using electromagnetic transient simulation approach, considering normal and transient conditions. Experimental results obtained from single-phase type 1 converter confirm the practical viability of the proposed converters.

1 Introduction

Since successful construction and operation of the Trans-Bay high-voltage direct current (HVDC) link, the half-bridge modular multilevel converter (HB-MMC) has received wide acceptance from utility and transmission systems operators. The HB-MMC offers attractive features such as[1-4]: potential scalability to ultra-high voltage overhead dc systems; and its ability to operate normally with a limited number of failed sub-modules, and resilient to ac faults. However, its main limitation is massive footprint due to the large number of its submodule capacitors. The full-bridge modular multilevel converter (FB-MMC) offers additional advantages such as[1, 5-7]: bipolar dc link voltage operation (thus, dc power reversal is achievable by reversing the dc link current or voltage); cell capacitor voltages can be regulated independently of the dc link voltage (hence, allowing operation with a variable dc link, including zero dc link voltage and over-modulation); and Ability to block, control and extinguish dc faults.

But the FB-MMC suffers from high semiconductor losses. Amongst other converter topologies proposed, the alternate arm converter (AAC) and hybrid cascaded two-level converter (HC2LC) offer relatively small footprint compared to FB-MMC, and retain some of the attributes of the FB-MMC such as dc fault blocking capability, variable dc voltage operation (including zero dc voltage), and a modest reduction of semiconductor losses[8]. However, the conventional AAC has problems of arm current commutation when it operate with power factor angle. All methods proposed to minimize the problem of arm current commutation in the conventional AAC deliberately alter its operation for a small portion of fundamental period, widely referred to as an overlap period, where both upper and lower arms of the same phase leg of the AAC conduct simultaneously as in the MMC case[9, 10]. Operation of the conventional AAC with fixed and actively controlled overlap period have been studied extensively. A fixed and short overlap period is effective when the conventional AAC operates at its sweet spot (maximum modulation index, $4/\pi \approx 1.27$, and near the unity power factor). The fixed overlap method is less attractive in HVDC applications as converter station is expected to operate over the

full P-Q envelope, including provision of reactive power during ac network faults. Active control of the overlap period over a wide range is able to reduce or even eliminate the problem of arm current commutation in the conventional AAC, but it has two implications:

- It increases the number of full-bridge cells needed per AAC arm to $N_{FBO}(1 + \sin^2 \mu)$ to enable upper and lower arms of the same phase-leg to operate as MMC during over overlap period (where, N_{FBO} and μ are the nominal number of FB cells per arm corresponding to half of the dc link voltage and μ is the overlap angle). This increases the AAC semiconductor losses.
- When the number of FB cells per arm is maintained at N_{FBO} , active control of the overlap angle over wide range reduces the maximum attainable modulation index.

Injection of 3rd harmonic into the modulating signal of each phase leg has been exploited to extend the region around zero voltage level and the overlap period accordingly, so as the AAC can operate as an MMC without the need for the active control of the overlap[11]. But the main downside of this method is that it increases the blocking voltage of the director switches, which sacrifices some of the AAC efficiency. Recently, extended over-lap AAC has been proposed to address the aforementioned shortcomings of the conventional AAC, particularly, the dependency of seamless arm current commutation on the power factor and over-voltage problem across the director switches, and elimination of the dc link capacitors[9]. In the extended overlap AAC (or simply EO-AAC), a triangular zero sequence injection is adopted (instead of previous sinusoidal zero sequence) to achieve extended overlap period up to 60°. It has been shown that with incorporation of extra FB cells in each arm of the EO-AAC, operation over full power factor range (0~1) is achievable without the above drawbacks. Also, the authors claim that the new triangular zero sequence guarantees simultaneous conduction of four arms of the EO-AAC at each instant, with two arms from the same phase leg provide path for dc current, and remaining two arms belong to different phase legs conduct to provide paths for ac phase currents. In this way, the EO-AAC eliminates the circulating currents between the phase legs and the arm inductors. However, it requires large dc inductor

at positive and negative dc rails to limit the charging current of the cell capacitors in the phase-leg that provides a path for dc current and to prevent the injection of ac current into dc link.

The mixed cell modular multilevel converter (MC-MMC) has similar footprint as that of the HB-MMC and FB-MMC, but it remains extremely attractive as it offers lower semiconductor loss than the AAC and retains most of the attributes of the FB-MMC such as modularity, dc fault blocking, and reduced dc link voltage operation[3, 12].

In recent years, several topologies of multilevel converters have been derived from the two fundamental topologies of the modular multilevel converter (the HB-MMC and FB-MMC) by employing different types of unipolar, asymmetric bipolar and symmetric bipolar cells[13]. Derivation of these topologies are motivated by a single aim of optimizing the circuit topology of the MMC type converters in terms of footprint and volume, semiconductor losses, control flexibilities and resiliency to dc faults. It has been recognized that the MMCs that employ asymmetric bipolar cells (cells that generate unequal number of positive and negative voltage levels) such as the double clamped offer good engineering compromise between semiconductor losses, dc fault blocking and control flexibilities[5, 13]. This is because these asymmetric cells allow MMCs to use the negative voltage levels of the asymmetric cells to recreate any dc voltage level from rated positive dc voltage to zero, while retaining full control over the power exchange between ac and dc sides. Therefore, the MMCs with asymmetric cells have wider control range and better dc fault ride-through performance compared to those with unipolar cells. In contrast, the MMCs that employ symmetric bipolar cells (cells generate equal number of positive and negative voltage levels) such as the FB cell and five-level cross-connected cell offer the maximum control flexibility and resiliency to dc fault and bipolar dc voltage operation at the expense of increased semiconductor losses compared to those with asymmetric cells[13, 14]. Apart from the FB-MMC, all other MMCs with symmetric cells are less attractive practically due to increased complexity of the cells structures and internal fault management.

Recently, an active forced commutated bridge converter is proposed for HVDC transmission systems with rated powers and voltages similar to that of the line commutated converters, i.e., 2000MW~3000MW and 800kV per converter[15]. Although the proposed active forced commutated bridge (AFC-B) converter requires large ac and dc side filtering, it offers many of the attributes of the FB-MMC at level of semiconductor losses similar or even lower than that of the HB-MMC as it uses thyristors in the main conduction paths. The AFC-B converter uses the FB cells in each of its limbs to actively commutate the current between the upper and lower arms of the same phase-leg; thus, no risk of commutation failure. The use of symmetrical thyristor allows the AFC-B converter to offer dc fault blocking, bipolar dc voltage operation, active or dc power reversal with change of polarity of dc link current or voltage, reactive power control in under and over-excitation regions and resiliency to both ac and dc short circuit faults.

In [16], a revised two-stage series bridge converter (SBC) is proposed, in which the high-voltage director switches are arranged as FB cells to facilitate connection to ac side. The high-voltage (HV) director switches operate at fundamental frequency and switch under zero voltage; thus, no switching losses incur in the HV-FB cells (director switches). The dc

terminals of each HV-FB cell are tapped into a portion of the HB chain-link which is connected across the dc rail. Each portion of the HB chain link is rated for $\frac{1}{2}V_{dc}$ (where $\frac{1}{2}V_{dc}$ is the rail-to-rail dc link voltage), and it is controlled to synthesize a rectified dc voltage with maximum peak of $\frac{1}{2}V_{dc}$ to be imposed at the dc input of each HV-FB cell. The main limitation of the original SBC has been addressed in [17, 18] by incorporating additional FB chain-link in series with the HV-FB cell of each phase in order to decouple reactive power and ac voltage control from the dc link voltage. The revised SBC adds losses and increases footprint compared to the original version [17, 18]; however, its footprint is expected to be smaller than the MMC type converters.

This paper presents type '1' and '2' hybrid converters as further optimization of the AAC such that the main attributes of the MC-MMC are retained, but with a reduced total capacitor volume as well as the power circuit and control complexity. Detailed operating principle, modulation and capacitor voltage balancing of the proposed converters are described. The open loop simulation results of both converters are used to demonstrate the main attributes such as seamless current commutation between the arms, low-frequency operation of the switching devices of the high-voltage half-bridge (HV-HB) cells and scalability to high-voltage applications. Whilst the suitability of the proposed converters for HVDC applications is demonstrated when both converters are modelled as one converter terminal of HVDC link. It has been shown that both converters can operate in all four quadrants; facilitate continued operation during a permanent pole-to-ground dc fault, with reduced dc voltage; and can block dc faults. The experimental results obtained from a single-phase scaled down proto-type of type '1' converter confirm the validity of the theoretical discussions and of the simulation results.

2 The proposed converter topologies

Fig.1(a) and (b) display the two hybrid converters being proposed for HVDC applications as alternatives to the conventional MC-MMC and AAC. Each arm of the type '1' converter in Fig.1(a) comprises of ' N_{FB} ' full-bridge cells, one high-voltage half-bridge cell and an arm inductor. During normal operation, the switching devices and cell capacitors of each full-bridge cell are designed to withstand voltage stress of $\frac{1}{2}V_{dc}/N_{FB}$, where V_{dc} represents the rated converter rail-to-rail dc link voltage. The switching devices and cell capacitors of each half-bridge cell withstand a voltage stresses of $\frac{1}{2}V_{dc}$ thus, strict series device connection is required to form high-voltage composite switching devices for the half-bridge cells. It is worth emphasizing that the technical feasibility of series connected IGBTs up to 400kV DC and operate at switching frequency above 1kHz has been demonstrated in East-West HVDC interconnector between UK and Republic of Ireland[19].

Considering phase 'a' as an example, the voltages across the upper and lower arms are:

$$v_{a1} \approx \frac{1}{2}V_{cref}(1 - m\sin(\omega t + \delta)) \quad (1)$$

$$v_{a2} \approx \frac{1}{2}V_{cref}(1 + m\sin(\omega t + \delta)) \quad (2)$$

where, the total voltage across the FB and HB cell capacitors of each arm is regulated at desirable dc voltage level (preferably at the nominal pole-to-pole dc link voltage), independent of the actual dc link; and ' ω ' and ' δ ' are the fundamental frequency in rad/s and arbitrary converter load angle.

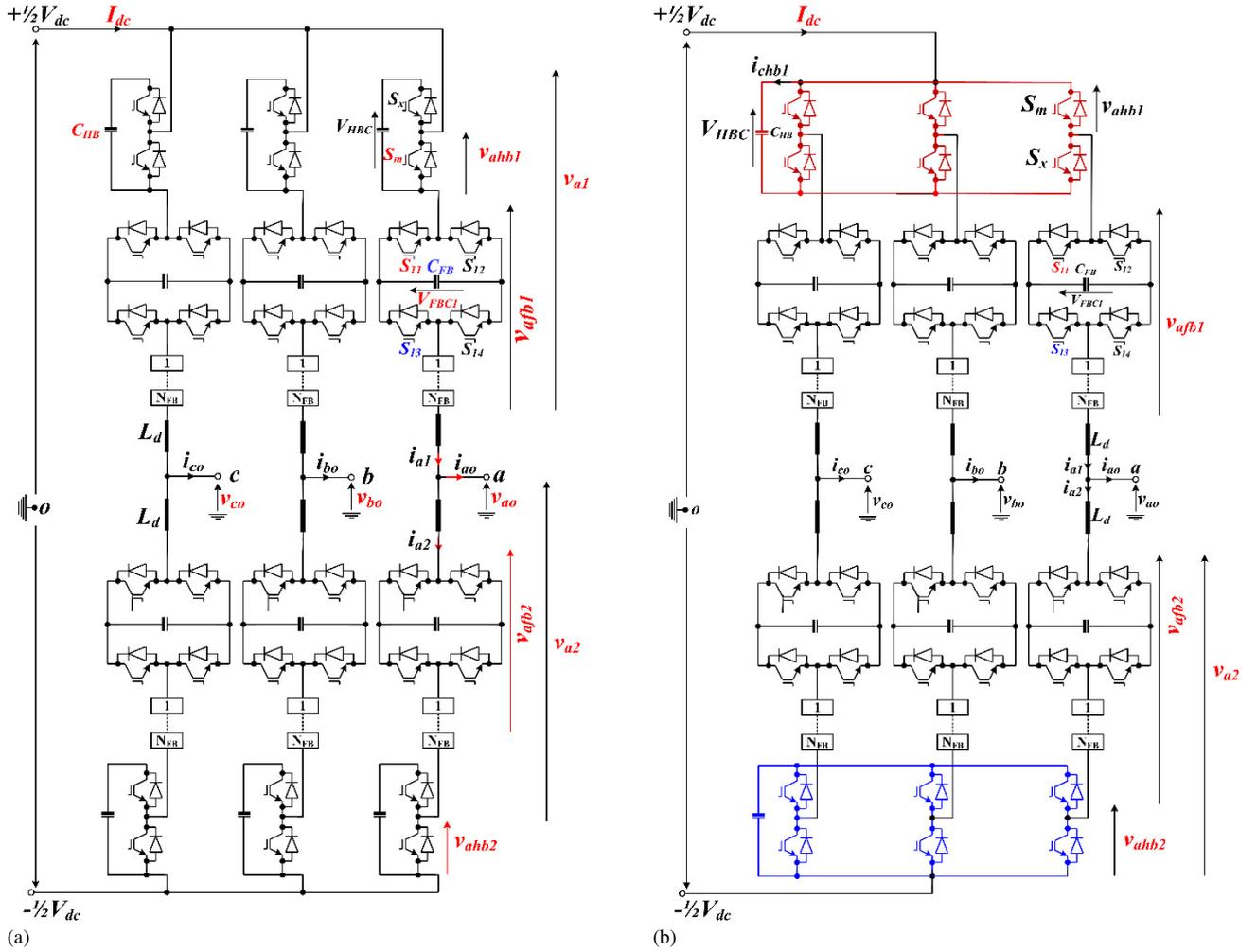


Fig.1: The proposed hybrid converters: (a) type '1' topology and (b) type '2' topology

Arm voltage synthesis in the type #1 hybrid converter in Fig.1(a) is summarized as follows:

- 1) When the voltage level to be synthesized in the arm j is within the range $\frac{1}{2}V_{dc} \leq v_{aj} \leq V_{dc}$, the output voltage of the half-bridge cell (v_{ahbj}) is added to the total output voltage (v_{afbj}) of the full-bridge cells being synthesized by inserting the appropriate number of the full-bridge cells into the power path with positive polarity

$$(v_{aj} \approx v_{hb} + v_{fb} \approx \frac{1}{2}V_{dc} + \sum_{k=1}^{n_{afbj}} V_{FBCj,k}), \text{ see Fig. 2. Selection of the}$$

full-bridge cells for insertion take into account the arm current polarity and magnitude of the capacitor voltages; where the subscript $j=1$ and 2 stand for the upper and lower arms and $n_{afbj} = mN_{FB}|\sin(\omega t + \delta)|$ represents the number of the full-bridge cells to be inserted into the power path. The ' $N_{FB} - n_{afbj}$ ' remaining FB cells which are not selected can be divided equally into two groups based on their voltage magnitudes, so that they can be inserted into the power path with opposite output voltage polarities to minimize the deviations of the FB cells capacitor voltages from the desired settling point $\frac{1}{2}V_{dc}/N_{FB}$.

- 2) When the voltage level to be synthesized is within the range $0 \leq v_{aj} < \frac{1}{2}V_{dc}$, the arm voltage can be synthesized by one of two possibilities (see Fig. 2):
 - a) Insertion of the full-bridge cells with positive output voltage polarity, and this case the number of full-bridge cells to be inserted to synthesize the desired

voltage level calculated as: $n_{afbj} = N_{FB} - mN_{FB}|\sin(\omega t + \delta)|$; therefore, the arm voltage to be synthesized can be approximated by:

$$v_{aj} \approx v_{fb} \approx \sum_{k=1}^{n_{afbj}} V_{FBCj,k}. \text{ The same strategy used in 1) to}$$

realize forced insertion of the cell capacitors in order to minimize capacitor voltage drift, applies.

- b) Subtraction of the total voltage being generated by the full-bridge cells (v_{afbj}) from that being generated by the half-bridge cell (v_{ahbj}). In this case, the number of full-bridge cells to be inserted with negative output voltage polarity in order to generate the desired voltage level is $n_{afbj} = mN_{FB}|\sin(\omega t + \delta)|$; thus, the arm voltage can be described by:

$$v_{aj} \approx v_{hb} - v_{fb} \approx \frac{1}{2}V_{dc} - \sum_{k=1}^{n_{afbj}} V_{FBCj,k}.$$

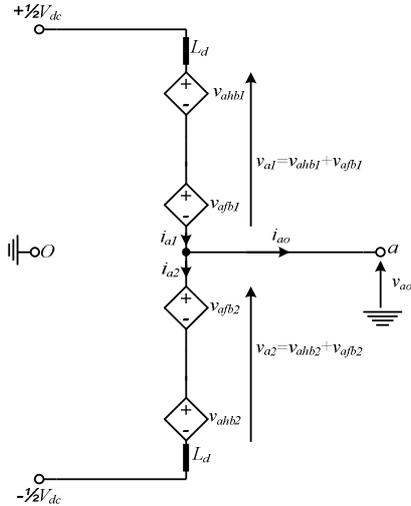
These two possibilities for generation of the arm voltage in this range could be exploited to ensure the voltage balancing of the half and full bridge cells of each arm. It worth emphasizing that the voltage ' $\frac{1}{2}V_{dc}$ ' can be synthesized by half-bridge cell only, with all full-bridge cells are bypassed; or by bypassing the half-bridge cells and inserting all full-bridge cells with positive polarity. Similarly, the '0' voltage can be synthesized by two different ways. However, the switching of the half-bridge cells when synthesizing the voltage levels 0 and $\frac{1}{2}V_{dc}$ should be minimized to reduce the switching losses. Therefore, exploitation of the '0' and ' $\frac{1}{2}V_{dc}$ ' voltage levels in order to reduce the energy requirements of the unipolar half-bridge

cells must be kept to minimum (trade-off between capacitor size and switching losses).

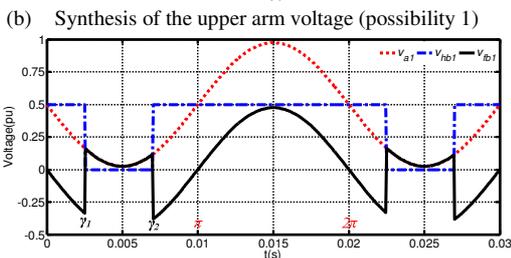
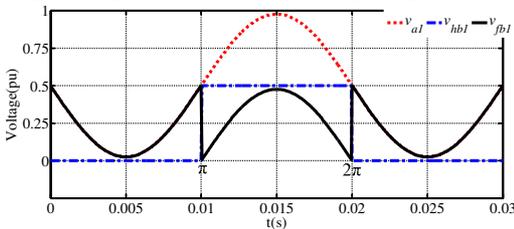
3) When the voltage level to be generated is $-1/2V_{dc} \leq v_{aj} < 0$ as expected during reduced dc link operation and a dc fault, only full-bridge cells are available to synthesize the negative voltage levels of the arms; thus, the number of full-bridge cells to be inserted with negative polarities is $n_{afbj} = mN_{FB} |\sin(\omega t + \delta)|$.

Switching device voltage and current stresses and the operating principle of the type 2 hybrid converter in Fig.1(b) are identical to that of the type 1 hybrid converter in Fig.1(a); except the capacitances of the three-phase HB cell of the type 2 hybrid converter in Fig.1(b) are smaller. This is because the capacitors of the three-phase HB cells of type 2 only experience the high-frequency current harmonics associated with the converter switching and not the fundamental current.

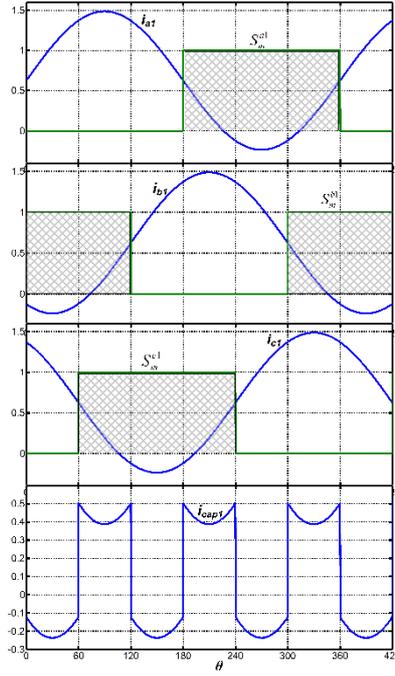
In comparison to the conventional MC-MMC that uses N cells per arm with equally split between the HB and FB cells, the type 1 converter in Fig.1(a) may have smaller footprint, weight and volume because its single high-voltage capacitor per arm would require less space, and mechanical support to ensure necessary insulation level from ground level compared to that of the ' $1/2N$ ' half-bridge cells in the MC-MMC. Also, the control complexity of the type 1 converter in Fig.1(a) and number of cell capacitor voltages to be measured for feedback are halved compared to the conventional MC-MMC. Both hybrid converters in Fig.1 (a) and (b) insert the same number of devices in a conduction path as in the MC-MMC, and, also offer reduced dc link operation and dc fault blocking.



(a) Simplified representation of one phase-leg of type #1 hybrid converter



(c) Synthesis of the upper arm voltage (possibility 2)



(d) Synthesis of the capacitor current of the type '2'

Fig. 2: Illustration of the arm voltage using simplified per arm represented of the proposed hybrid converters

3 Analysis of the proposed converter topologies

This section uses simplified representation of the proposed converters in Fig. 2 to derive their mathematical models. From Fig. 2(a), dynamics of phase 'a' upper and lower arms of types '1' and '2' can be described as:

$$\begin{aligned} L_d di_{a1}/dt + R_d i_{a1} + v_{a1} - \frac{1}{2}V_{dc} + v_{ao} &= 0 \\ L_d di_{a2}/dt + R_d i_{a2} + v_{a2} - \frac{1}{2}V_{dc} - v_{ao} &= 0 \end{aligned} \quad (3)$$

With perfect suppression of the circulating currents, phase 'a' upper and lower arm currents are:

$$\begin{aligned} i_{a1} &\approx I_d + \frac{1}{2}i_{a0} \\ i_{a2} &\approx I_d - \frac{1}{2}i_{a0} \end{aligned} \quad (4)$$

Where ' I_d ' represents the dc component of the common-mode current.

After algebraic manipulation of (3), subtraction and addition, the following equations are obtained:

$$\begin{aligned} L_d d(i_{a1} - i_{a2})/dt + R_d (i_{a1} - i_{a2}) + (v_{a1} - v_{a2}) + 2v_{ao} &= 0 \\ L_d d(i_{a1} + i_{a2})/dt + R_d (i_{a1} + i_{a2}) + (v_{a1} + v_{a2}) - V_{dc} &= 0 \end{aligned} \quad (5)$$

When the upper and lower arm voltages across are expressed as: $v_{a1} = \frac{1}{2}\bar{V}_c [\alpha_d - m \sin(\omega t + \delta)]$ and $v_{a2} = \frac{1}{2}\bar{V}_c [\alpha_d + m \sin(\omega t + \delta)]$, equation (5) can be decomposed as:

$$\frac{1}{2}L_d di_{a0}/dt + \frac{1}{2}R_d i_{a0} = \frac{1}{2}m\bar{V}_c \sin(\omega t + \delta) - v_{ao} \quad (6)$$

$$L_d dI_d/dt + R_d I_d = \frac{1}{2}[V_{dc} - \alpha_d \bar{V}_c] \quad (7)$$

Equations (6) and (7) show that the differences between fundamental voltage behind the arm inductors and fundamental output voltage ' v_{ao} ', and the dc voltage ' V_{dc} ' and common-mode voltage ' $v_{a1} + v_{a2} = \alpha_d \bar{V}_c$ ', determine the fundamental output phase current ' i_{a0} ', and the dc component of common-mode or arm currents ' I_d ', respectively as in the conventional MMC.

The upper and lower arm voltages of the proposed converter can be expressed in terms of the full and half-bridge cells switching functions as:

$$v_{aj} \approx v_{fbj,a} + v_{hbja} \approx S_{hbja}^a(t)V_{CHBj}^a + \sum_k^{N_{FB}} [S_{fbj,k}^a(t)V_{CFBj,k}^a] \quad (8)$$

The switching function of the k^{th} FB cell in j^{th} arm ' $s_{fbj,k}(t)$ ' takes the values of 1, 0 and -1, with the states '1' and '-1' stand for the cell insertion with positive and negative voltage polarities, and '0' for the cell bypass. Whilst the switching function of the high-voltage HB cell of the j^{th} arm ' $s_{hbj}(t)$ ' takes the values of 1 and 0, with the state '1' stands for cell insertion with positive polarity and '0' for bypass. When each arm of the proposed converter contains sufficient number of FB cells, equation (8) for phase 'a' can be approximated as:

$$\begin{aligned} v_{a1} &= v_{hb1,a} + v_{fb1,a} = s_{hb1}^a(t)V_{CHB1} + \sum_k^{N_{FB}} [s_{fb1,k}^a(t)V_{CFB1,k}^a] \approx \frac{1}{2}\bar{V}_c[\alpha_d - m\sin(\omega t + \delta)] \\ v_{a2} &= v_{hb2,a} + v_{fb2,a} = s_{hb2}^a(t)V_{CHB2} + \sum_k^{N_{FB}} [s_{fb2,k}^a(t)V_{CFB2,k}^a] \approx \frac{1}{2}\bar{V}_c[\alpha_d + m\sin(\omega t + \delta)] \end{aligned} \quad (9)$$

Where $\bar{V}_c \approx \frac{1}{2}(\sum_{j=1}^2 \sum_{k=1}^{N_{FB}} V_{CFBj,k}^a + \sum_{j=1}^2 V_{CHBj}^a)$ and $\alpha_d \approx V_{dc}/\bar{V}_c$. From (9), the differential arm voltage represents the output phase voltage ' v_{ao} ' when the voltage drops across the arm inductors are neglected:

$$v_{ao}(t) \approx v_{a2}(t) - v_{a1}(t) \approx \frac{1}{2}m\bar{V}_c \sin(\omega t + \delta) \quad (10)$$

To simplify the capacitor voltage balancing analysis, the dc voltage across each arm ' \bar{V}_c ', is assumed to be regulated at V_{dc} ; thus, $\alpha_d \approx 1$. Considering the switching possibility in Fig. 2(b) as an example, the phase 'a' modulation functions of the FB cells for types '1' and '2' converters and half-bridge cell of the type '1' converter (upper arm) can be approximated by:

$$m_{fb1}(t) = \begin{cases} 0 \leq \omega t \leq \pi: & d_1 = \frac{1}{2}[1 - m\sin(\omega t + \delta)] \\ \pi \leq \omega t \leq 2\pi: & d_2 = -\frac{1}{2}m\sin(\omega t + \delta) \end{cases} \quad (11)$$

$$m_{hb1}(t) = \begin{cases} 0 \leq \omega t \leq \pi: & \rho_1 = 0 \\ \pi \leq \omega t \leq 2\pi: & \rho_2 = \frac{1}{2} \end{cases} \quad (12)$$

Since the average capacitor current is a good indicator of the capacitor voltage balance, the average capacitor currents of the FB and HB cells (I_{cap1}^{fb} and I_{cap1}^{hb}) are:

$$I_{cap1}^{fb} \approx \frac{1}{2\pi} \left(\int_0^\pi d_1 i_{a1} d\omega t + \int_\pi^{2\pi} d_2 i_{a1} d\omega t \right) \approx \frac{1}{4\pi} I_m \cos \varphi - \frac{1}{16} m I_m \cos \varphi \approx \left[\frac{1}{m\pi} - \frac{1}{4} \right] I_d \quad (13)$$

$$I_{cap1}^{hb} \approx \frac{1}{2\pi} \int_0^\pi \rho_2 i_{a1} d\omega t \approx -\left[\frac{1}{m\pi} - \frac{1}{4} \right] I_d \quad (14)$$

The above analysis of the state-of-charge of the FB cell capacitors is applicable to both type '1' and '2' converters, while that of the HB cell capacitors which is developed on per phase basis is only applicable to type '1' converter. This analysis indicates that the average currents the FB and HB cell capacitors draw are nonzero, which indicates the necessity for a dedicated capacitor voltage balancing to ensure that the total arm dc voltage is correctly distributed between the HB and FB cells, and even distribution of the voltage across the low-voltage rated FB cells. The average power being exchanged between the HB and FB cells of the phase 'a' upper arm and ac side over one fundamental period is:

$$P_{a1} \approx \int_0^{2\pi} v_{a1}(t) i_{a1}(t) d\omega t \approx 0 \quad (15)$$

Equation (15) indicates indicate shows that the arms of the proposed converters exchange zero active powers with the ac side over each fundamental period, which confirms the energy balance at arm level. This is mathematically supported as the average currents of the full and half bridge cell capacitors in (13) and (14) have the same magnitudes and opposite polarities, which indicate the sufficiency of the exploitation of

the redundant switch states within each arm to force the average currents of the HB and FB cell capacitors to be zero. Additionally, the above discussions indicate that during one fundamental period the charging of the HB cell capacitors happen when the FB cell capacitors discharge, and the opposite is true. To quantitatively substantiate the sufficiency of the exploitation of the manipulation of the redundant switch states for ensuring the voltage balance of the half and full-bridge cells that constitute each, the average currents of the half and full-bridge cell capacitors are redefined, considering the switching possibility in Fig. 2(c) as follows:

$$I_{cap1}^{hb} \approx \frac{1}{2\pi} \left(\int_0^{\gamma_1} \frac{1}{2} i_{a1} d\omega t + \int_{\gamma_2}^{2\pi} \frac{1}{2} i_{a1} d\omega t \right) \approx \frac{1}{2} I_d \left[1 - \frac{1}{2\pi} (\gamma_2 - \gamma_1) \right] \quad (16)$$

$$I_{cap1}^{fb} \approx -\frac{1}{2} I_d \left[1 - \frac{1}{2\pi} (\gamma_2 - \gamma_1) \right]_d \quad (17)$$

Equations (16) and (17) show that the switching instances of the high-voltage HB cells (which are exemplified by γ_1 and γ_2) can be manipulated to force the average currents drawn by the HB and FB cell capacitors to zeros. With Equations (16) and (17) indicate that the HB and FB capacitor average currents become zeros when $\gamma_1 - \gamma_2 = 2\pi$, which clearly show it is not possible to force the average currents of the HB and FB cell capacitors to zero over one fundamental period when the HB cells strictly operate at 50Hz. From the above discussions, it is concluded that the HB cells need to operate at more than 50Hz in order to nullify the HB and FB cell capacitor average currents over one fundamental period. But this conclusion does not preclude capacitor voltage balancing over several fundamental periods when the HB cells operate at 50Hz.

For analysis of the state-of-charge of the cell capacitors of the three-phase cells of the type '2' converter, the switching functions S_m^{a1} , S_m^{c1} and S_m^{c1} that describe the states of the switches that insert the high-voltage cell capacitor into the power paths are defined as depicted in Fig. 2(d). Using these switching functions, the capacitor current of three-phase cell of the upper arms can be defined in terms of arm currents ' i_{a1} , i_{b1} and i_{c1} ' as:

$$i_{cap1}^{fb}(t) = S_m^{a1} i_{a1} + S_m^{b1} i_{b1} + S_m^{c1} i_{c1} \quad (18)$$

The theoretical plot of the capacitor current in (18), assuming the case of unity power factor is shown at the bottom of the Fig. 2(d). This theoretical plot shows that the fundamental currents do not flow in the capacitors of the three-phase cells of type '2' converter as that of the type '1'; instead, with ideal switching possibility in Fig. 2 (b) and (d), these capacitors are expose to 3rd harmonic currents. In fact, these capacitors will be exposed to higher frequencies characteristic harmonics than the 3rd harmonic as the capacitor voltage balancing described earlier will force the three-phase cells of the type '2' converter to switch several times per fundamental period. Provided the capacitor voltage ripple is inversely proportional to frequency of the current that flows through it, the three-phase half-bridge cells of type '2' converter are expected to have lower capacitance requirement compared to type '1' converter.

Benefiting from the cyclic behaviour of the capacitor current in Fig. 2(d), the average capacitor current in the three-phase cell can be calculated over 120°. Considering the period $0 \leq \theta \leq 120^\circ$, the HB average capacitor current can be expressed as:

$$I_{cap}^{hb1} = \frac{3}{2\pi} \left(\int_0^{\frac{1}{3}\pi} i_{b1} d\omega t + \int_{\frac{1}{3}\pi}^{\frac{2}{3}\pi} (i_{b1} + i_{c1}) d\omega t \right) = -3I_d \left[\frac{1}{\pi m} - \frac{1}{4} \right] \quad (19)$$

Notice the average capacitor current of the three-phase half-bridge cell in (19) of the type '2' converter is three times that of the half-bridge of the type '1' converter presented in (14). Equation (19) indicates the necessity of additional switching actions at the three-phase cells of the type '2' converter in order to nullify the average currents. Notice that the average capacitor currents of the FB and HB cells of the types '1' and '2' converter become zeros under zero power factor operation (as $\varphi = \pi/2$, $I_d = \frac{1}{4}mI_m \cos\varphi = 0$, in reactive power applications such as STATCOM), which indicates the natural balancing of the capacitor voltages of the HB and FB cells without the need for extra-switching at the single-phase and three-phase HB cells.

For approximate sizing of the HB and FB cell capacitances of the type '1' converter, an ideal switching possibility in Fig. 2(b) is assumed. Therefore, equivalent continuous capacitor currents of the FB and HB cells can be expressed in piecewise manner over two time intervals as illustrated earlier. On this basis, the full and half bridge capacitor voltages of the phase 'a' upper arm could be expressed as:

$$0 \leq \omega t \leq \pi: \begin{cases} dV_{FBC1}(t)/dt \approx N_{FB} di_{a1}/C_{FB} \\ dV_{HBC1}(t)/dt \approx 0 \end{cases} \quad (20)$$

After trigonometry and algebraic manipulations, (20) can be reduced to:

$$0 \leq \omega t \leq \pi: \begin{cases} \Delta V_{FBC1}(t) \approx \frac{N_{FB}}{2\omega C_{FB}} \left[-K \cos(\omega t + \delta + \varphi + \gamma) + \frac{1}{8} m I_m \sin(2\omega t + 2\delta + \varphi) \right] \\ V_{HBC1}(t) \approx V_{HBC1}(0) \Rightarrow \Delta V_{HBC1}(t) = 0 \end{cases} \quad (21)$$

Where, $\gamma = \tan^{-1} \left[\frac{\frac{1}{2} I_m \sin \varphi}{\frac{1}{2} I_m \cos \varphi - m I_d} \right]$ and $K = \sqrt{\frac{1}{4} I_m^2 - (4 - m^2) I_d^2}$

$$\pi < \omega t \leq 2\pi: \begin{cases} dV_{FBC1}(t)/dt \approx N_{FB} di_{a1}/C_{FB} \\ dV_{HBC1}(t)/dt \approx i_{a1}/C_{HB} \end{cases} \quad (22)$$

Similarly, (22) can be reduced to:

$$\pi < \omega t \leq 2\pi: \begin{cases} \frac{dV_{FBC1}(t)}{dt} \approx \frac{N_{FB} \left[I_d - \frac{1}{2} m I_d \sin(\omega t + \delta + \varphi) + \frac{1}{4} m I_m \cos(2\omega t + 2\delta + \varphi) \right]}{C_{FB}} \\ \frac{dV_{HBC1}(t)}{dt} \approx \frac{\frac{1}{2} \left[I_d + \frac{1}{2} I_m \sin(\omega t + \delta + \varphi) \right]}{C_{HB}} \end{cases} \quad (23)$$

Since the dc components of the capacitor currents will in (23) will be nullified by the capacitor voltage balancing and have no influence on the capacitor voltage ripples, these dc components will be ignored in the calculations of the capacitor voltage ripples will be undertaken below. Thus, (23) becomes:

$$\pi < \omega t \leq 2\pi: \begin{cases} \frac{dV_{FBC1}(t)}{dt} \approx \frac{\frac{1}{2} N_{FB} \left[-m I_d \sin(\omega t + \delta + \varphi) + \frac{1}{2} m I_m \cos(2\omega t + 2\delta + \varphi) \right]}{C_{FB}} \\ \frac{dV_{HBC1}(t)}{dt} \approx \frac{\frac{1}{4} I_m \sin(\omega t + \delta + \varphi)}{C_{HB}} \end{cases} \quad (24)$$

After integration of the (24), yields:

$$\pi < \omega t \leq 2\pi: \begin{cases} \Delta V_{FBC1}(\omega t) \approx \frac{\frac{1}{2} N_{FB} \left[m I_d \cos(\omega t + \delta + \varphi) + \frac{1}{4} m I_m \sin(2\omega t + 2\delta + \varphi) \right]}{\omega C_{FB}} \\ \Delta V_{HBC1}(\omega t) \approx -\frac{1}{4} \frac{I_m \cos(\omega t + \delta + \varphi)}{\omega C_{HB}} \end{cases} \quad (25)$$

Time-domain simulations and validations of equations (21) and (25) show that the theoretical capacitances of the FB and HB cells which are calculated based on equation (25), considering only the fundamental capacitor voltage ripples ($C_{FB} = N_{FB} m I_d / 2\omega \Delta \hat{V}_{FBC}$ and $C_{HB} = I_m / 4\omega \Delta \hat{V}_{HBC}$) overestimate and underestimate the final fine tuned values of the cell

capacitances by less than 10%. It is worth emphasizing that the above analyses ignore the contribution of the capacitor voltage balancing. Therefore, time-domain simulations is needed to further fine-tune the theoretical estimates of the HB and FB cell capacitances in order to ensure satisfactory performance during ac and dc faults.

4 Illustrative Simulations

To assess the performances of the proposed converters, both type '1' and '2' converters are modelled using electromagnetic transient simulation program (EMTP) approach, which was originally proposed by H. Dommel in 1969 in [20], and later applied to MMC in [21]. In this approach, the converter switching devices are described by two-state switched resistors, and each cell capacitor is replaced by its electromagnetic transient equivalent (the Thevenin equivalent voltage that represents the history terms behind the factitious resistance of the capacitor). This modelling approach is used due to its efficiency in full-scale simulations of modular type converters with hundreds of cells per arm [21]. Since the proposed converters operate as MMCs, the common-mode capacitor voltages of the phase legs drive the circulating currents as part of the arm currents. Therefore, a resonant based circulating current suppression controller tuned at 2nd and 4th order harmonics are incorporated. To regulate the half and full bridge cell capacitor voltages of the proposed converters, independent of the dc link voltage, additional controllers that regulate the common-mode capacitor voltage sums of the phase legs are implemented. The capacitor voltage balancing described in section 2 are employed to ensure that total voltage across the arm is equally split between the FB cells and HV-HB cells, and total voltage across the full-bridge cells are evenly distributed between individual FB cells..

For ease of illustration, the proposed type '1' and '2' converter topologies are fed from a 640kV dc link when they operate with 0.95 modulation index, and their ac sides were connected to a passive load of 100Ω and 238mH (which is equivalent to 889MW and 665MVar inductive). To substantiate the theoretical discussions presented in section 2, Fig. 3 and Fig.4, and Fig. 5 and Fig.6 present selected simulation waveforms that illustrate the basic operation and scalability of the type 1 and 2 converters in Fig.1(a) and (b) respectively. The simulation parameters and operating conditions are summarized in their respective captions.

4.1 Illustrative simulations of type 1 hybrid converter:

Fig. 3 (a) and (b) show the phase output voltage 'v_{ao}' of type 1 converter measured relative to ground (dc link mid-point, o), and voltage across the upper arm of phase 'a', v_{a1} superimposed on the output voltages of the HV-HB and FB cells of phase 'a' upper arm, v_{ahb1} and v_{afb1}. Observe that synthesis of the desired output and arm voltages require proper coordination between the switching actions of the HV-HB and FB cells of the same arm, and of the upper and lower arms of the same phase leg such that v_{ahb1} + v_{afb1} = v_{a1} ≈ 1/2 V_{dc} (1 - m sin ωt) and v_{ao} = 1/2 (v_{a2} - v_{a1}) ≈ 1/2 m V_{dc} sin ωt. This necessitates full exploitations of the positive and negative output voltage levels of the FB cells of each arm with that of the HV-HB cell as described in section 2, and depicted in Fig. 3 (a) and (b). Additionally, sample waveform for the output voltage of the HV-HB cell 'v_{ahb1}' of the upper arm in Fig. 3 (b) indicates that the switching devices of the HV-HB cells which are rated for 1/2 V_{dc} operate at extremely low switching frequency, ranging

from 50Hz ~200Hz (this entails low switching loss at high-voltage half-bridge cells). This result supports the theoretical discussions that claim the necessity for extra switching actions at the HV-HB cells to enable utilization of the redundant switch states when arm voltages between 0 and $\frac{1}{2}V_{dc}$ for balancing of the HB and FB capacitor voltages. The waveforms in Fig. 3 (a) and (b) and above discussions show that the use of HV-HB cells with series connected devices do not have any noticeable negative implications on the converter output voltage in terms of dv/dt nor insulation requirements of the converter transformer. However, in practical implementation of full-scale HVDC converter, additional engineering measures will be needed to match the switching speeds of the HV-HB cells devices and that of the FB cells in order to minimize the magnitude and duration of voltage spikes that may arise in the common-mode voltage. The short duration mismatch between the common-mode voltage of the affected phase-leg and unaffected phase legs and input dc link voltage will result in short duration inrush currents that will be suppressed instantly by the arm inductors. The plots of the three-phase output currents (i_{ao} , i_{bo} and i_{co}) and phase 'a' upper and lower arm currents (i_{a1} and i_{a2}) in Fig. 3 (c) and (d) indicate that the type 1 converter generates high quality output currents, and the upper and lower arms of the same phase-leg conduct simultaneously and exhibit continuous arm currents as in conventional MMC. The upper and lower arm currents of type '1' converter comprise of half of the output phase ac current plus dc current and other parasitic current components as in conventional MMC ($i_{a1}=i_d+\frac{1}{2}i_{ao}+i_{ah}$, where $i_d\approx\frac{1}{3}I_{dc}$ and i_{ah} represent the dc and harmonic current components of phase 'a' common-mode current). Fig.4 (a) and (b) show that the capacitor voltages of the HV-HB and FB cells of the type 1 converter in Fig.1(a) are well maintained at the desired set-points ($V_{HBC}\approx\frac{1}{2}\times 640\text{kV}\approx 320\text{kV}$ and $V_{FBC}\approx\frac{1}{2}\times 640\text{kV}/20\approx 16\text{kV}$ when $N_{FB}=20$), and these are achieved by exploiting only the available redundant switch states described in section 2. Notice that the output voltage and capacitor voltages of the HB cells of type 1 converter in Fig. 3 (b) and Fig.4 (a) remain constant for considerable parts of the fundamental period, which indicates reduced switching losses of the HV-HB cells. However, exposure of the HV-HB cell capacitors to fundamental currents plus remnant of circulating currents have resulted in low-frequency capacitor voltage ripples cells as in the conventional MMC case, see Fig.4 (a).

In summary, the aforementioned discussions show that the type '1' converter resembles a new version of MC-MMC, where large number of cascaded low-rated voltage cells of conventional MC-MMC are replaced by one equivalent high-voltage half-bridge cell. In this way, insulation and isolation requirements and cost of the supporting mechanical structure needed for suspension of the high-voltage half-bridge cells might be reduced; hence, the footprint. Also, type '1' converter in Fig.1(a) could be seen as an improved alternate arm converter, where the director switches of the conventional AAC are replaced by the high-voltage half-bridge cell to facilitate typical MMC operation all the time, instead of over narrow window as discussed earlier as part of motivation of this paper.

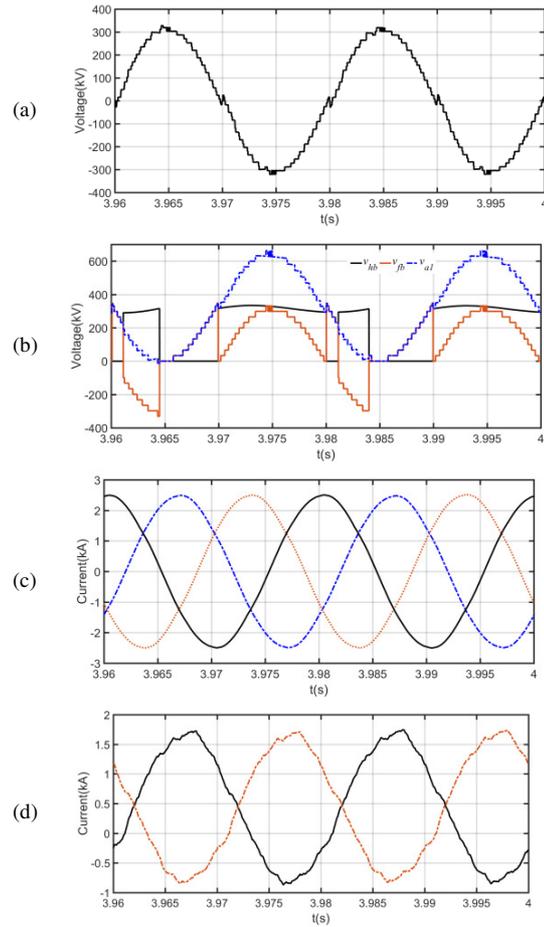


Fig. 3: Simulation waveforms that illustrate the basic operation of type '1' converter ($V_{dc}=640\text{kV}$, $L_d=35\text{mH}$, $C_{HB}=100\mu\text{F}$, $C_{FB}=250\mu\text{F}$, $N_{FB}=20$, and modulation index $m=0.95$)

- (a) Pre-filter phase voltage (v_{ao}) measured relative to ground.
- (b) Upper arm voltage in blue, and output voltages of the HV-HB and FB cells in black and red respectively
- (c) Three-phase output currents
- (d) Upper and lower arm currents of the same phase-leg

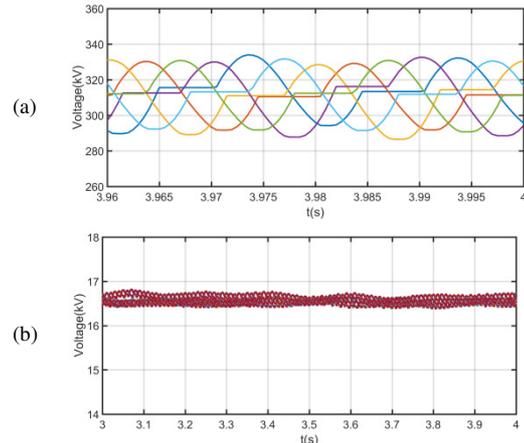


Fig.4: Simulation waveforms that illustrate the basic operation of type '1' converter ($V_{dc}=640\text{kV}$, $L_d=35\text{mH}$, $C_{HB}=100\mu\text{F}$, $C_{FB}=250\mu\text{F}$, $N_{FB}=20$, and modulation index $m=0.95$)

- (a) Capacitor voltages of the six HV-HB cells
- (b) Capacitor voltages of the FB cells.

4.2 Illustrative simulations of type 2 hybrid converter

Fig. 5 (a) and (b) present phase 'a' output voltage ' v_{ao} ', and voltage across phase 'a' upper arm ' v_{a1} ' superimposed on the output voltages of the three-phase HV-HB and FB cells of phase 'a' upper arm (v_{ahb1} and v_{afb1}) of the type 2 converter in Fig.1(b). Observe that both positive and negative voltage levels

of the FB cells in each arm are exploited in coordinating with the voltage levels of the three-phase HV-HB cell in order to ensure correct operation of the type ‘2’ converter, while each arm generates the desired voltage $v_{a1}=v_{ahb1}+v_{afb1}\approx\frac{1}{2}V_{dc}(I-m\sin\omega t)$ in order to synthesize the correct output voltage $v_{ao}\approx\frac{1}{2}mV_{dc}\sin\omega t$.

Fig. 5(b) shows that the output voltage of the three-phase high-voltage cell of the type ‘2’ converter in Fig.1(b) exhibits a modest increase in the switching frequency compared to that of the single-phase HV-HB cells of the type ‘1’ converter. However, the effective switching frequency of the three-phase cell remains low (about 150Hz, which indicates low switching losses as in type 1 converter). The results Fig. 5 (a) and (b) and above discussions suggest that the use of high-voltage three-phase cells with series connected devices do not increase dv/dt on the converter transformer. The three-phase output currents (i_{ao} , i_{bo} and i_{co}) and phase ‘a’ upper and lower arm currents (i_{a1} and i_{a2}) in Fig. 5 (c) and (d) indicate that the type ‘2’ converter generates high quality output currents, with its arm currents are similar to that of type ‘1’ converter. Fig.6 (a) and (b) show that the capacitor voltages of the HV three-phase cells and of the FB cells of the type ‘2’ converter in Fig.1(b) are tightly regulated using the redundant switch states described in section 2, with the FB cell capacitor voltages are tightly regulated at $V_{FBC}\approx\frac{1}{2}\times 640\text{kV}/151\approx 2.12\text{kV}$ as $N_{FB}=151$ for the simulated type ‘2’ converter. Fig.6 (a) shows that the capacitor voltages of the three-phase cells of the type 2 converter oscillate at six times the fundamental frequency, and this is an indication of low capacitance requirement of the type ‘2’ converter compared to that of type ‘1’ converter and conventional MMC. The case presented in Fig.6 demonstrates the scalability and suitability of type ‘2’ converter for high-voltage applications, including adherence to the same operating principle as that of the type ‘1’ converter.

In summary, the type ‘2’ converter in Fig.1(b) is expected to have smaller footprint, weight and volume than the type 1 in Fig.1(a), including the requirement for smaller capacitance. Loosely, the type 2 converter in Fig.1(b) resembles front-to-front connection of two three-phase two-level hybrid cascaded converter.

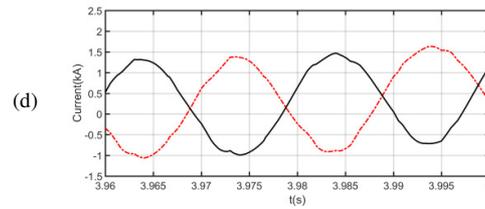
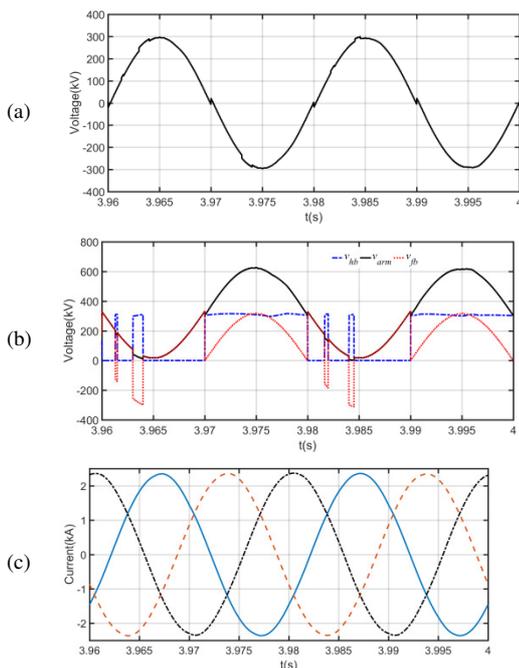


Fig. 5: Simulation waveforms that illustrate the basic operation of type ‘2’ converter and its scalability ($V_{dc}=640\text{kV}$, $L_d=35\text{mH}$, $C_{HB}=100\mu\text{F}$, $C_{FB}=1.25\text{mF}$, $N_{FB}=151$ and 95 modulation index).

- (a) pre-filter phase voltage (v_{ao}) measured relative to ground
(b) upper arm voltage in blue, and half and full-bridge cells output voltages in black and red respectively
(c) three-phase output currents
(d) upper and lower arm currents of the same phase-leg

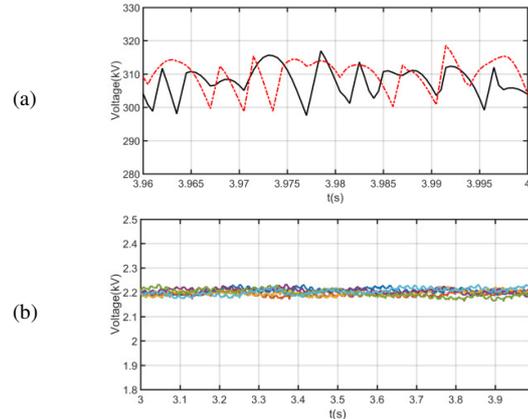


Fig.6: Simulation waveforms that illustrate the basic operation of type ‘2’ converter and its scalability ($V_{dc}=640\text{kV}$, $L_d=35\text{mH}$, $C_{HB}=100\mu\text{F}$, $C_{FB}=1.25\text{mF}$, $N_{FB}=151$ and 95 modulation index).

- (a) Capacitor voltages of the two three-phase HV-HB cells
(b) Capacitor voltages of the FB cells .

5 DC Side System Studies

Fig.7(a) and (b) present the test system and control system being used to assess the performance of the proposed converters in system settings. Details synthesis of the control system in Fig.8(b) can be found in[22]. Besides the test system parameters in Fig.7(a), additional parameters are listed in Table I.

Simulation scenarios to be considered in assessments of the proposed converters are:

- Normal operation with adjustable set-points.
- Pole-restraining during a pole-to-ground dc fault
- Pole-to-pole dc short circuit faults.
- Reduced dc voltage operation

The equivalent inertias of the type 1 and 2 converters are 34ms (34kJ/MVA) and 17ms (17kJ/MVA) respectively.

Table I: Parameters of the illustrative test system in Fig.7(a)

Converter rated apparent power	1200MVA
Converter rated active power	1140MW
Converter rated reactive power	$\pm 375\text{MVAr}$
Rated dc link voltage	640kV
Half-bridge cell capacitance	100 μF
Full-bridge cell capacitance	1.25mF
Arm inductance	35mF
Number of full-bridge cells per arm	151
dc line resistance	0.01 Ω/km
dc line inductance	1mH/km
dc line capacitance	0.2 $\mu\text{F}/\text{km}$

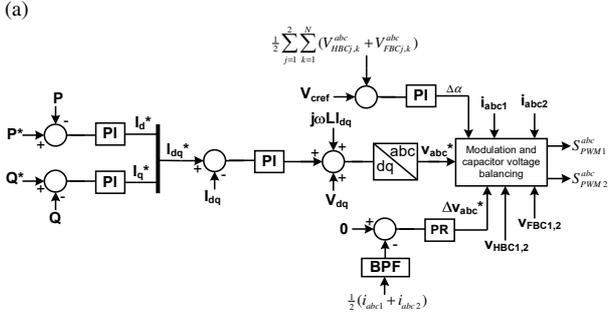
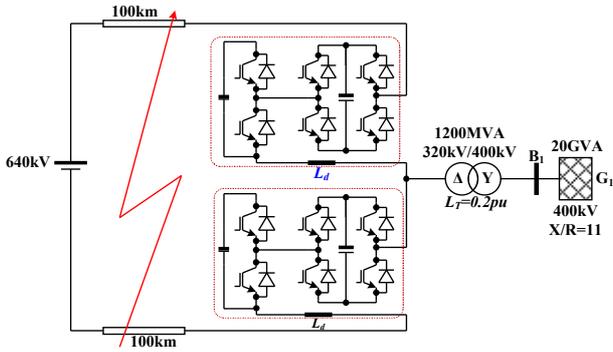


Fig. 7: (a) Illustrative test system and (b) functional block diagram of the control system employed with the test system in Fig.7(a).

5.1 Normal operation

Fig.8 presents simulation waveforms for normal operation of type 1 converter when it is operating as power controlling terminal of HVDC link, see Fig.7. Initially, it maintains its output active power at zero, and at $t=0.5s$, it ramps its output active power from 0 to 1140MW (rated power), and followed by ramp down of its reactive power output from 0 to -375MVar (rated) at $t=1s$. At $t=2s$, the power flow direction is reversed from 1140MW to -1140MW.

Fig.8 (a) and (b) show converter output active and reactive powers, and three-phase currents at the converter terminal, measured at 320kV side of the interfacing transformer. The plots for the phase 'a' upper and lower arm currents in Fig.8(c), captured when the converter operates with unity power factor confirm satisfactory operation of type '1' with power flow in both directions, while generating reactive power. The plots in Fig.8(d) show that the HV-HB and FB cells of the same arm operate in a manner that ensures correct synthesis of the arm voltage, while the switching devices of the HV-HB operate at extremely low frequency. Fig.9 (a) and (b) show that the voltage stresses across the HV-HB and FB cell capacitors and switching devices are maintained around the desired settling points as the type '1' converter varies its active and reactive power set-points.

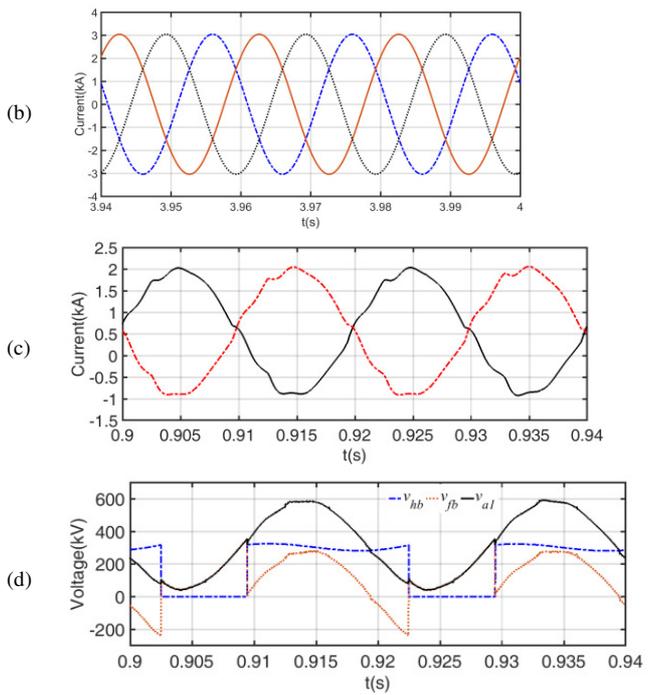
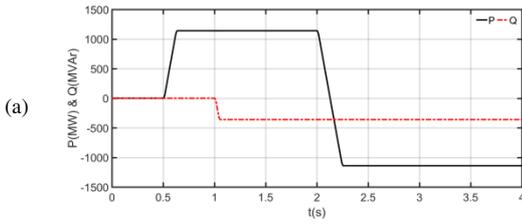


Fig.8: Waveforms illustrate normal operation of type '1' converter
(a) Active and reactive powers.
(b) Output phase currents
(c) Phase 'a' upper and lower arm currents
(d) Phase 'a' upper arm voltage superimposed on the output voltages of the HV-HB cells and total voltage across the FB cells.

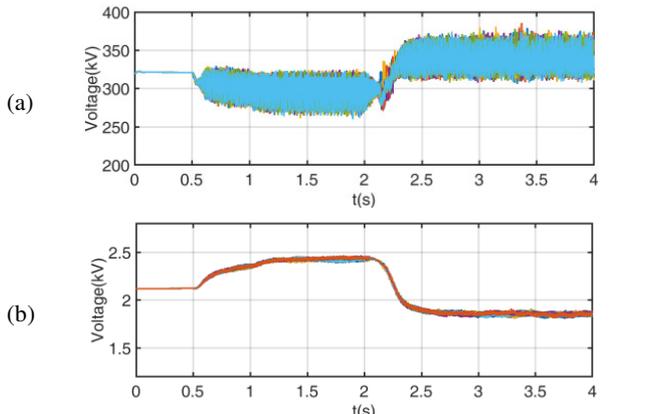


Fig.9: Waveforms illustrate normal operation of the type '1' converter
(a) Pole Half-bridge capacitor voltages
(b) Full-bridge capacitor voltages

5.2 Pole restraining during pole-to-ground dc fault

Fig.10 shows simulation waveforms when the positive dc cable in the test system in Fig.7 is subjected to a permanent pole-to-ground dc fault (at the middle of the dc cable) at $t=1.25s$, and immediately the type '1' converter reduces its output active power from 1140MW to 570MW in preparation for pole restraining (Halving of the pole-to-pole dc voltage). After 150ms from fault inception, the converter dc link voltage is halved to facilitate continued operation, whilst preventing insulation failure at the healthy pole due to excessive voltage stress. Fig.10 (a) shows the positive and negative pole dc voltages, measured relative to ground. The dc voltage of the faulty pole drops to zero, while that of the healthy pole has doubled briefly, prior to the initiation of pole restraining. Fig.10 (b) shows phase 'a' upper and lower arm voltages (v_{a1} and v_{a2}), and output voltages being synthesized by the HV-HB and FB cells of phase 'a' upper and lower arms (v_{hb1} and v_{hb2} ,

and v_{fb1} and v_{fb2}) during pole restraining (when the dc voltage is halved). These plots confirm low frequency operation of the HV-HB cells as articulated earlier. The plots for half and full bridge capacitor voltages in Fig.10 (c) and (d) indicate that the type '1' converter are able to ride-through a permanent pole-to-ground dc fault, with the voltage stresses on the switching devices and cell capacitors remain under controlled. Fig.11 (a) shows the type 1 converter is able to synthesize the required ac voltage at the converter terminal when its dc link voltage is halved during pole-restraining, exploiting the ability of its arms to generate negative voltage levels. Moreover, during a permanent pole-to-ground dc fault, the phase voltage of the type 1 converter in Fig.11 (a) exhibits a lower dc component than the $\frac{1}{2}V_{dc}$ as it will be expected in conventional two-level converter and HB-MMC.

5.3 Pole-to-pole dc short circuit

Fig.12 displays simulation waveforms when the test system in Fig.7(a) is subjected to a permanent pole-to-pole dc short circuit fault at the midpoint of the dc line at $t=1.25s$, and the type '1' hybrid converter is blocked after $30\mu s$ from fault inception. Fig.12 (a) displays the pole-to-pole dc link voltage at dc line mid-point. The plots for the converter output and arm currents in Fig.12(b) and (c) confirm the dc fault blocking capability of the type '1' converter. The plots in Fig.13 (a) and (b) indicate that the HV-HB and FB cell capacitor voltages of the type '1' converter remain flat and fixed at pre-fault values as in other reverse blocking converters such the MC-MMC and FB-MMC.

5.4 Reduced dc voltage operation

Fig.14 shows simulation waveforms for the type '2' converter when its active power output is reduced from rated (1140MW) to 0 at $t=0.9s$, and followed by a permanent reduction of its dc link voltage from rated (640kV) to 64kV (10% of rated dc voltage). At $t=2.25s$, its reactive power output is increased from 0 to 375MVar (rated capacitive).

Fig.14 (a) and (b) indicate that the type '2' converter in Fig.1(b) is able to operate with rated and reduced dc link voltage, while its output and arm currents remain fully controlled. These plots show that the type '2' converter is able to source the rated capacitive reactive power when it operates with 10% of the rated dc link voltage. The traces for the phase 'a' upper arm voltage and the output voltages of its corresponding half and full bridge cells in Fig.14 (c) indicate that when the dc link voltage is reduced below $\frac{1}{2}V_{dc}$, the HV-HB cells are bypassed completely. Instead, the arm voltages needed to synthesize the ac voltages being imposed by the ac grid at converter ac terminals are being generated entirely using only the FB cells (zero switching frequency at HV-HB

cells). Thus, the HV-HB cells incur no switching losses, only on-state losses are incurred during such operation. Fig.15 (a) and (b) show that the capacitor voltages of the HV-HB and FB cells of the type '2' converter remain balanced and regulated around the desired set-points.

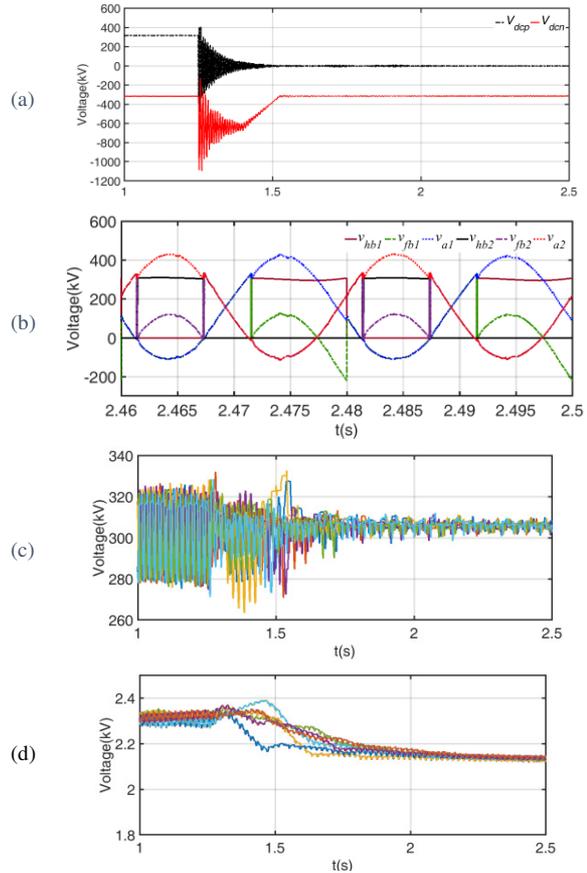


Fig.10: Waveforms demonstrate pole restraining that facilitates continued operation under permanent pole-to-ground dc fault.

- (a) Positive and negative dc pole voltages.
- (b) Phase 'a' upper arm voltage superimposed on the output of the HB cell and total voltage across the FB cells.
- (c) Voltages across the HB cells.
- (d) Voltage across the FB cells

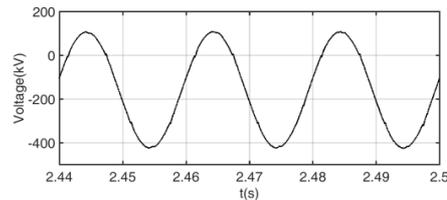


Fig.11: Waveforms demonstrate pole restraining that facilitates continued operation under permanent pole-to-ground dc fault.

- (a) Phase 'a' phase voltage, zoomed during a pole-to-ground dc fault following application of pole restraining.

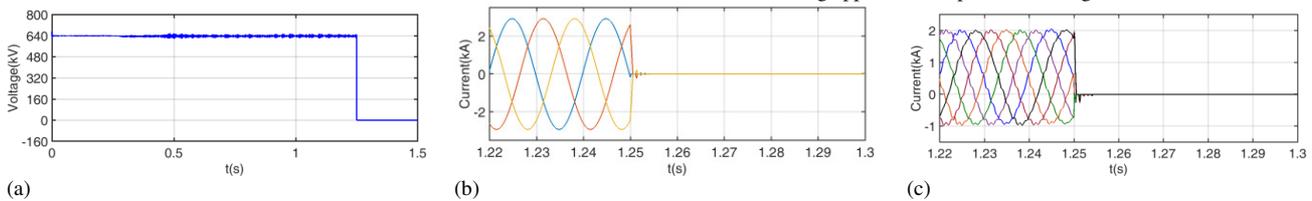


Fig.12: Simulation waveforms demonstrate dc fault blocking.

- (a) Pole-to-pole dc link voltage
- (b) Three-phase output currents measured at the low-voltage side of the interfacing transformer, zoomed around the fault instant
- (c) Snapshot of the arm currents, zoomed around the fault instant

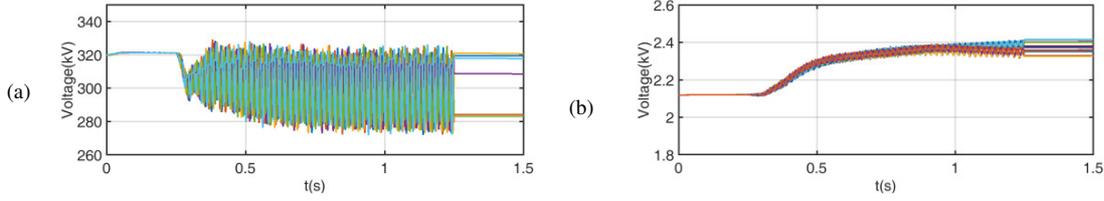


Fig.13: Simulation waveforms demonstrate dc fault blocking

- (a) HV-HB capacitor voltages.
- (b) FB capacitor voltages.

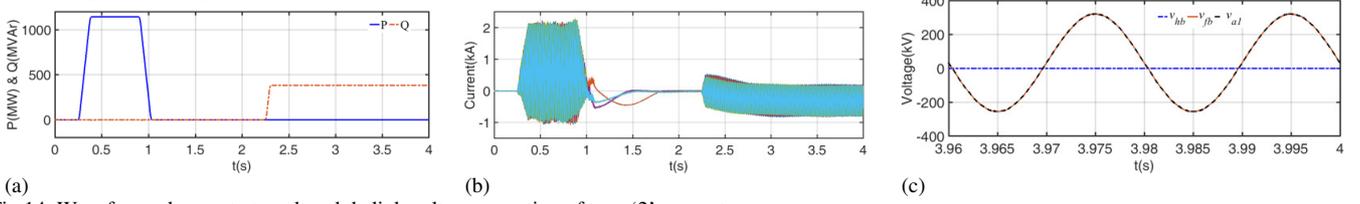


Fig.14: Waveforms demonstrate reduced dc link voltage operation of type '2' converter.

- (a) Active and reactive powers that the converter exchanges with the ac grid at bus B₁.
- (b) Upper and lower arm currents of the three phase legs.
- (c) Phase 'a' upper arm voltage superimposed on the voltages being synthesized by its corresponding half and full bridge cells.

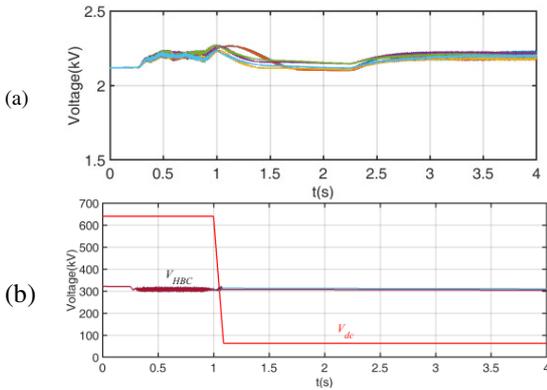


Fig.15: Waveforms demonstrate reduced dc link voltage operation of type '2' converter.

- (a) FB capacitor voltages of the six arms
- (b) DC link voltage superimposed on the HV-HB cell capacitor voltages of the six arms.

6 Experimental validation

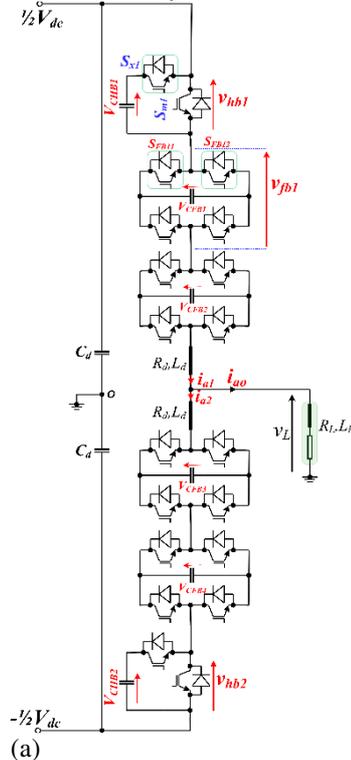
This section presents experimental validation of the proposed converters, particularly, the type '1' converter, which represents the basis for the type 2 converter. Fig. 16 (a) and (b) show the schematic diagram and photograph of the experimental test rig of a single-phase type 1 converter, with two FB cells and one HB cell in each per arm. Experimental test rig parameters are: $V_{dc}=220V$, $C_{HB}=1mF$, $C_{FB}=2.2mF$ and $L_d=2mH$, $R_d=0.5\Omega$ and 2kHz switching frequency, with the converter being tested is connected to a passive load of 10 Ω and 15.5mH, and operated at 0.95 and 0.4 modulation indices.

Fig. 17 presents experimental waveforms for 0.95 modulation index case. Fig. 17(a) displays the output phase voltage ' v_L ' superimposed on the output phase current ' i_{ao} ', while Fig. 17(b) presents output phase current ' i_{ao} ' overlaid on the upper and lower arm currents ' i_{a1} and i_{a2} '. These waveforms show that the type 1 converter with only two full-bridge cells and one half-bridge cell per arm generates the same number of voltage levels per phase as the conventional MMC with four half or full bridge cells per arm. Additionally, its upper and lower arm currents are similar to that of the conventional modular multilevel converter in the sense of:

- The upper and lower arm currents are continuous, with both arms are conducting simultaneously.

- The arm currents comprise of half of the fundamental current and common-current which has two components (the dc current and circulating current), with the circulating current has adverse effect on semiconductor losses and capacitor voltage ripples; thus, to be suppressed as in MMC case.

Fig. 17(c) and (d) present experimental waveforms for the FB and HB cell capacitor voltages of the upper and lower arms of the type 1 converter being examined. Observe that the FB and HB cell capacitor voltages remain balanced and settle approximately around 55V ($1/4V_{dc}$) and 110V ($1/2V_{dc}$) respectively, with small drifts from the ideal theoretical values due to dc voltage drops in the switching devices and arm inductors' internal resistances. The plots for additional case with 0.4 modulation in Fig. 18 indicate that the type '1' can operate satisfactory over full modulation index linear range.





(b)

Fig. 16: Schematic diagram and picture of one phase-leg of the type '1' converter

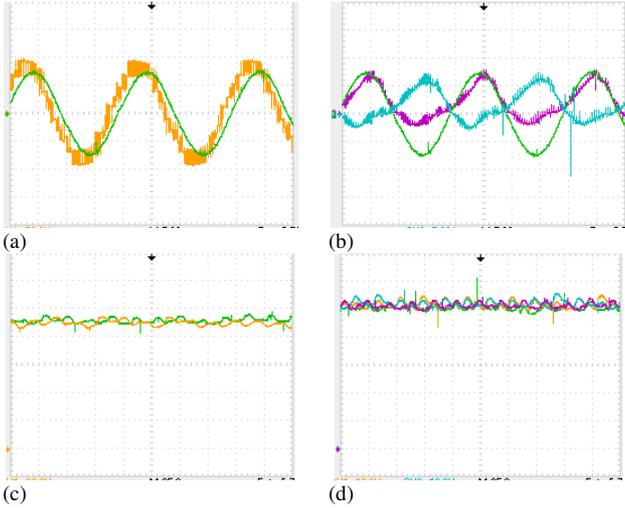


Fig. 17: Experimental waveforms for type '1' hybrid converter when it operates at 0.95 modulation index, 2kHz switching frequency, $V_{dc}=220V$, and connected to phase load of 10Ω and $15.5mH$.

- (a) Output phase voltage and current (v_L and i_{ao} , 5ms/div, 50V/div and 5A/div).
 (b) Upper and lower arm currents ' i_{a1} and i_{a2} ' superimposed on the output phase current ' i_{ao} ' (5ms/div, 5A/div).
 (c) Upper and lower arms FB cell capacitor voltages (25ms/div, 20V/div)
 (d) Upper and lower arms HB cell capacitor voltages (25ms/div, 10V/div)

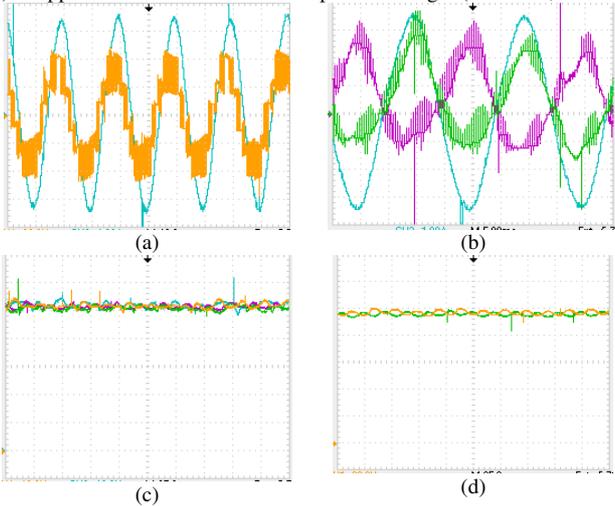


Table II shows the proposed converters have marginally higher semiconductor losses than MC-MMC in some cases due to the differences in the way they exploit their IGBTs and freewheeling diodes and potential impact of large voltage step of the high-voltage half-bridge cell. Whilst the AAC exhibits higher semiconductor losses compared to the proposed converter and MC-MMC even though its director switches incur zero switching losses (this is due to increased voltage

Fig. 18: Experimental waveforms for type #1 hybrid converter when it operates at 0.4 modulation index, lagging power factor, 2kHz switching frequency, $V_{dc}=220V$ and connected to a passive of 10Ω and $15.5mH$.

- (a) Output phase voltage and current ' v_L and i_{ao} ' (10ms/div, 20/div and 1A/div)
 (a) Upper and lower arm currents ' i_{a1} and i_{a2} ' superimposed on the output phase current ' i_{ao} ' (5ms/div, 1A/div)
 (b) Full-bridge cell capacitor voltages of the upper and lower arms
 (c) Half-bridge cell capacitor voltages of the upper and lower arms

7 Estimate of Semiconductor Losses

Table II presents a semiconductor loss comparison between the proposed converters, the MC-MMC and the AAC. This comparison assumes that all converters are rated at 1000MVA, 640kV dc link voltage, 353kV line-to-line ac voltage and 4.5kV, 1800A IGBTs (T1800GB45A), with steady state voltage stress per switch in 2.8kV in HB and FB cells and director switches. Each converter on-state losses are calculated from simulation on cell by cell basis using $P_{OnS_T} = V_{T0}\bar{I}_T + R_T I_{rms_T}^2$ and $P_{OnS_D} = V_{D0}\bar{I}_D + R_D I_{rms_D}^2$, where, V_{T0} and V_{D0} , and R_T and R_D are IGBT and freewheeling diode threshold voltage drops and on-state resistances, and \bar{I}_T and \bar{I}_D and $I_{rms_T}^2$ and $I_{rms_D}^2$ are IGBT and diode average and root mean square currents. Switching losses are calculated on the basis of IGBT turn-on and turn-off energy losses (E_{on} and E_{off}) which are approximated by the following polynomials:

$$E_{on} = -270.7 \times 10^{-12} i_{on}^4 + 1.812 \times 10^{-6} i_{on}^3 - 2.744 \times 10^{-3} i_{on}^2 + 4.953 i_{on}$$

$$E_{off} = -3.11 \times 10^{-9} i_{off}^4 + 11.57 \times 10^{-6} i_{off}^3 - 13.65 \times 10^{-3} i_{off}^2 + 8.921 i_{off}$$

where i_{on} and i_{off} are currents at the turn-on and turn-off instances. Switching loss per IGBT is approximated by: $P_{sw} = (f_{on}\bar{E}_{on} + f_{off}\bar{E}_{off})$, where \bar{E}_{on} and \bar{E}_{off} are average turn-on and turn-off energy losses over one fundamental cycle, and f_{on} and f_{off} are average switching frequencies. The number of FB cells in each arm of the proposed converters, AAC and MC-MMC is assumed to be $N_{FB}=320/2.8 \approx 115$, while the number of HB cells in each arm of MC-MMC is 115. Each high-voltage HB cell of the proposed converter is rated for 320kV, with each of its series connected IGBT comprises of 115 IGBT. Each director switch of the AAC arm is rated for $4/\pi \times 320 \approx 407kV$ and comprises 146 series connected IGBTs.

rating of director switches and frequent over-currents and over-voltages during current commutation between the arms).

Table III shows the case when the AAC switching device utilization is the same as the proposed converter and MC-MMC. Observe that the AAC semiconductor losses have reduced to practically the same level as the MC-MMC and the proposed converters. Since both of the selected operating conditions correspond to modulation indices lower than 1, the AAC with full bridge cells rated for $1/2 V_{dc}$ can still block a dc fault. Fixing the operating point of the AAC at the sweet spot

means that the converter loses the ability to manipulate its terminal voltage (larger and smaller) relative to the grid voltage in order to exchange capacitive and inductive reactive powers.

Table II: Summary of semiconductor losses assuming all converter being compared have the same dc link voltage and ac side voltage ($V_{dc}=640kV$ and line to line ac voltage $V_L=353kV_{rms}$)

	Proposed hybrid converter				MC-MMC		AAC	
	Type #1		Type #2		On-state	Switching	On-state	Switching
	On-state	Switching	On-state	Switching				
P=1000MVA at PF=1	5.25MW	2.36MW	5.48MW	2.35MW	5.35MW	2.34MW	7.50MW	1.35MW
Total losses	7.61MW (0.76%)		7.83MW (0.78%)		7.69MW (0.77%)		8.85MW (0.89%)	
P=800MVA at PF=0.8 lagging	5.08MW	2.12MW	5.10MW	2.17MW	5.34MW	2.31MW	7.52MW	1.43MW
Total losses	7.20MW (0.72%)		7.27MW (0.73%)		7.65MW (0.77%)		8.98MW (0.90%)	
P=800MW at PF=0.8 tor leading	5.53MW	2.60MW	5.65MW	2.31MW	5.34MW	2.39MW	7.21MW	1.37MW
Total losses	8.13MW (0.81%)		7.96MW (0.80%)		7.74MW (0.77%)		8.58MW (0.86%)	

Table III: AAC semiconductor losses when the dc link voltage utilization is assumed to be the same as the proposed converters and MC-MMC ($V_{dc}=640kV$ and line-to-line ac voltage $V_{L,AAC} \approx \bar{m}_{AAC}/\bar{m}_{MMC} \times V_{L,MMC} \approx 1.273/1.154 \times 353kV \approx 389.4kV$, where \bar{m}_{AAC} and \bar{m}_{MMC} are the AAC and MMC maximum attainable modulation indices)

P=1000MW at PF=1		P=800MW at PF=0.8 lagging		P=800MW at PF=0.8 leading	
On-state	Switching				
6.11MW	1.16MW	6.83MW	1.50MW	5.83	1.19MW
7.27MW (0.73%)		8.33MW		7.02MW (0.70%)	

8 Conclusions

This paper has investigated the suitability of the presented type 1 and 2 hybrid converters for dc transmission systems. Theoretical discussions, and open and closed loop simulations suggest that the type converter offers all the attributes of MC-MMC but with a reduced complexity in the power circuit and control system, including a modest reduction in footprint, energy storage requirement, and switching losses. In contrast, the type 2 hybrid converter offers the performance of the MC-MMC and type 1 hybrid converter, but with a substantial reduction in converter footprint and energy storage requirement. Thus, it can be concluded that the type 2 hybrid converter offers the best design trade-off in terms of cost, footprint, weight and volume and control range for HVDC converters compared to type 1 converter and conventional AAC and MMC. The presented experimental results confirm the validity of the theoretical discussions and open simulations presented earlier.

9 References

- [1] A. A. J. Far, M. Hajian, D. Jovicic, and Y. Audichya, "High-power modular multilevel converter optimal design for DC/DC converter applications," *IET Power Electronics*, vol. 9, pp. 247-255, 2016.
- [2] G. P. Adam, I. A. Gowaid, S. J. Finney, D. Holliday, and B. W. Williams, "Review of dc-dc converters for multi-terminal HVDC transmission networks," *IET Power Electronics*, vol. 9, pp. 281-296, 2016.
- [3] Z. Xu, S. Wang, and H. Xiao, "Hybrid high-voltage direct current topology with line commutated converter and modular multilevel converter in series connection suitable for bulk power overhead line transmission," *IET Power Electronics*, vol. 9, pp. 2307-2317, 2016.
- [4] A. F. Q. Gonçalves, C. R. Aguiar, R. F. Bastos, G. G. Pozzebon, and R. Q. Machado, "Voltage and power control used to stabilise the distributed generation system for stand-alone or grid-connected operation," *IET Power Electronics*, vol. 9, pp. 491-501, 2016.
- [5] C. Petino, M. Heidemann, D. Eichhoff, M. Stumpe, E. Spahic, and F. Schettler, "Application of multilevel full bridge converters in HVDC multiterminal systems," *IET Power Electronics*, vol. 9, pp. 297-304, 2016.
- [6] A. Elserougi, A. M. Massoud, A. S. Abdel-Khalik, and S. Ahmed, "Three-wire bipolar high-voltage direct current line using an existing single-circuit high-voltage alternating current line for integrating renewable energy sources in multiterminal DC networks," *IET Renewable Power Generation*, vol. 10, pp. 370-379, 2016.
- [7] N. Ahmed, L. Angquist, A. Antonopoulos, L. Harnefors, et al., "Performance of the modular multilevel converter with redundant submodules," in *Industrial Electronics Society, IECON 2015 - 41st Annual Conference of the IEEE*, 2015, pp. 003922-003927.
- [8] M. M. C. Merlin and T. C. Green, "Cell capacitor sizing in multilevel converters: cases of the modular multilevel converter and alternate arm converter," *IET Power Electronics*, vol. 8, pp. 350-360, 2015.
- [9] M. M. C. Merlin, D. S. Sanchez, P. D. Judge, G. Chaffey, P. Clemow, T. C. Green, et al., "The Extended Overlap Alternate Arm Converter: A Voltage Source Converter with DC Fault Ride-Through Capability and a Compact Design," *IEEE Transactions on Power Electronics*, vol. PP, pp. 1-1, 2017.
- [10] F. J. Moreno, M. M. C. Merlin, D. R. Trainer, T. C. Green, and K. J. Dyke, "Zero phase sequence voltage injection for the alternate arm converter," in *AC and DC Power Transmission, 11th IET International Conference on*, 2015, pp. 1-6.
- [11] F. J. Moreno, M. M. C. Merlin, D. R. Trainer, T. C. Green, and K. J. Dyke, "Zero phase sequence voltage injection for the alternate arm converter," in *11th IET International Conference on AC and DC Power Transmission*, 2015, pp. 1-6.
- [12] E. C. Mathew, M. B. Ghat, and A. Shukla, "A Generalized Cross-Connected Submodule Structure for Hybrid Multilevel Converters," *IEEE Transactions on Industry Applications*, vol. 52, pp. 3159-3170, 2016.
- [13] G. P. Adam, I. Abdelsalam, J. E. Fletcher, G. M. Burt, D. Holliday, and S. J. Finney, "New Efficient Submodule for a Modular Multilevel Converter in Multiterminal HVDC Networks," *IEEE Transactions on Power Electronics*, vol. 32, pp. 4258-4278, 2017.
- [14] J. J. Jung, S. Cui, J. H. Lee, and S. K. Sul, "A New Topology of Multilevel VSC Converter for a Hybrid HVDC Transmission System," *IEEE Transactions on Power Electronics*, vol. 32, pp. 4199-4209, 2017.
- [15] P. Li, S. J. Finney, and D. Holliday, "Active-Forced-Commutated Bridge Using Hybrid Devices for High Efficiency Voltage Source Converters," *IEEE Transactions on Power Electronics*, vol. 32, pp. 2485-2489, 2017.
- [16] E. Amankwah, A. Costabeber, A. Watson, D. Trainer, O. Jasim, J. Chivite-Zabalza, et al., "The Series Bridge Converter (SBC): A hybrid modular multilevel converter for HVDC applications," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, 2016, pp. 1-9.
- [17] R. Feldman, M. Tomasini, J. C. Clare, P. Wheeler, D. R. Trainer, and R. S. Whitehouse, "A hybrid voltage source converter arrangement for HVDC power transmission and reactive power compensation," in *5th IET International Conference on Power Electronics, Machines and Drives (PEMD 2010)*, 2010, pp. 1-6.

- [18] R. Feldman, M. Tomasini, J. C. Clare, P. Wheeler, D. R. Trainer, and R. S. Whitehouse, "A low loss modular multilevel voltage source converter for HVDC power transmission and reactive power compensation," in *9th IET International Conference on AC and DC Power Transmission, 2010. ACDC*, 2010, pp. 1-5.
- [19] J. Egan, P. O. Rourke, R. Sellick, P. Tomlinson, B. Johnson, and S. Svensson, "Overview of the 500MW EirGrid East-West Interconnector, considering System Design and execution-phase issues," in *Power Engineering Conference (UPEC), 2013 48th International Universities'*, 2013, pp. 1-6.
- [20] H. W. Dommel, "Digital Computer Solution of Electromagnetic Transients in Single-and Multiphase Networks," *Power Apparatus and Systems, IEEE Transactions on*, vol. PAS-88, pp. 388-399, 1969.
- [21] U. N. Gnanarathna, A. M. Gole, and R. P. Jayasinghe, "Efficient Modeling of Modular Multilevel HVDC Converters (MMC) on Electromagnetic Transient Simulation Programs," *Power Delivery, IEEE Transactions on*, vol. 26, pp. 316-324, 2011.
- [22] G. P. Adam and I. E. Davidson, "Robust and Generic Control of Full-Bridge Modular Multilevel Converter High-Voltage DC Transmission Systems," *IEEE Transactions on Power Delivery*, vol. 30, pp. 2468-2476, 2015.