Modular Two-level Voltage Source Converter for Direct Current Transmission Systems

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***Abstract*—This paper presents a modular two-level voltage source converter (M2L-VSC) suitable for short distance dc transmission systems with relatively low dc operating voltage. The proposed M2L-VSC consists of two sets of three-phase cells, with each cell has its own capacitor, and these capacitors do not discharge when converter is blocked during dc short circuit fault. The main attributes of the proposed M2L-VSC are absence of the 2nd order harmonic from the arm currents, and reduced energy storage requirement as the cell capacitor only experience high-order harmonic currents associated with the switching frequency as in conventional two-level converter (C2L). The technical feasibility of the M2L-VSC for dc transmission systems has been assessed using simulations and corroborated experimentally. It has been shown that the transient responses of M2L-VSC to ac and dc faults are similar to that of the modular multilevel converter (MMC).**

***Key words*— ac and dc fault ride-through capability, high-voltage dc transmission systems, modular multilevel converter, and two-level voltage source converter.**

I. INTRODUCTION

In recent years, the uses of voltage source converters in high-voltage dc (VSC-HVDC) transmission systems have increased substantially, predominantly, for reinforcement of weak ac networks, and connections of offshore wind farms and oil platforms. The C2L based VSC-HVDC transmission systems are known for their simple power circuits and straightforward control systems, and small footprint[1, 2].The main drawbacks of the C2L in HVDC transmission systems are [1-4]: suffer from high semiconductor losses, predominantly, switching losses, and require large ac filters; and increase dc fault level as the dc link capacitors contribute large discharge currents to dc fault.

Introduction of MMC to the HVDC transmission systems addresses many of the shortcomings of the C2L and offers a number of attractive features such as [1-4]: reduced semiconductor losses; no ac filters; substantial reduction in the magnitude of the dc fault current as the distributed cell capacitors do not discharge when converter is blocked during dc faults; extremely low *dv/dt* due to sequential switching of small voltage steps; and the use of power electronic building blocks (PEBB) facilitate scalability of single pole to much higher dc operating voltage such as 640kV and 800kV.

The main drawbacks of the MMC are[1-4]: large footprint; and complex and slow dynamic response due to its high energy content (nearly ten times that of the two-level converter). Moreover, the exponential increase in the number of measurable quantities and in the complexity of the power circuit and control systems, makes the MMC susceptible to malfunctions and less attractive for HVDC links with relatively low rated powers and dc voltages (less than 300MW and ±150kV per pole).

Besides the MMC, there are a number of hybrid multilevel converters have been discussed in the open literate that retain most of the features of the MMC, while reducing footprint and complexity of the power circuit. But most of these hybrid converters tend to achieve the above features at expense of increased semiconductor losses[2, 5].

This paper presents a M2L-VSC for dc transmission systems, with relatively low dc voltage and rated power, which aims to:

- Reduce the complexity of the control and power circuit and converter footprint compared to MMC.
- Reduce dc circuit breakers (DCCBs) current stresses during dc faults as the cell capacitors of the M2L-VSC do not contribute any current to dc fault when converter is blocked during dc short circuit faults [6, 7].
- Large reduction in the cell capacitance which is achieved by the adoption of the three-phase cells could results substantial saving in converter cost and improved dynamic response.

Moreover, this paper briefly discusses the operating principle of the M2L-VSC. The performances of the M2L-VSC in HVDC transmission systems have been examined, considering open loop with passive loads at 50Hz and 1Hz, closed loop using simulations and scaled-down experimentations. Results obtained from these examinations have shown that the transient responses of proposed M2L-VSC during ac and dc faults are similar to that of the conventional MMC[6, 7].

II. MODULAR TWO-LEVEL VOLTAGE SOURCED CONVERTER

Fig. 1 shows a three-phase M2L-VSC that employs only two three-phase high-voltage cells instead of large number of half-bridge cells rated for small fraction of total dc ink voltage. The use of a single three-phase cell arrangement per three arms, upper and lower arms has proven to be technical attractive in terms of size, weight and energy storage requirement as the cell capacitors of the M2L-VSC do not

experience fundamental currents. Exposure of the cell capacitors of the M2L-VSC to only high-frequency harmonics associated with the carrier frequency of the pulse width modulation has led to substantial reduction in the cell capacitance requirement. The arm inductors are needed for filtering of the high frequency harmonics associated with the switching of the upper and lower cells and to limit any potential inrush current that may arise due to the mismatch between the common-mode voltages and the input dc link voltage. Also, the arm inductors limit the ac grid contribution to dc short circuit fault and restrain the rate of change of arm current that will be seen by the freewheeling diodes when M2L-VSC is blocked during dc short circuit fault. Besides its inherent natural cell capacitor voltage balance, the common-mode currents of the M2L-VSC do not contain unwanted components such as 2nd order harmonic currents (also known as circulating current), and this is because its common-mode voltages do not contain a 2nd harmonic component to drive the circulating current as in the conventional MMC. Because the connection points of the upper and lower arm cells are opposite (positive rail and ac poles for upper cells and ac poles and negative rail for lower cells), both upper and lower arm cells receive the same gating signals to ensure complementary operation of the upper and lower arms and satisfy the Kirchhoff voltage law by the all three phases:

$$\mathbf{v}_{abc1}(t)+\mathbf{v}_{abc2}(t)\approx\boldsymbol{\psi}V_{dc} \tag{1}$$

The column vectors for the switched output voltages of the upper and lower cells, $v_{abc1}=[v_{a1},v_{b1},v_{c1}]^T$ and $v_{abc2}=[v_{a2},v_{b2},v_{c2}]^T$ are expressed in terms of the switch states of the six-pulse bridge converter being employed in each arm and cells capacitors as:

$$\mathbf{v}_{abc1}(t)=\bar{\mathbf{s}}_{abc1}(t)V_{c1} \tag{2}$$

$$\mathbf{v}_{abc2}(t)=\mathbf{s}_{abc2}(t)V_{c2} \tag{3}$$

where $\boldsymbol{\Psi}=[1\quad 1\quad 1]^T$; $\bar{\mathbf{s}}_{abc1}(t)=[\bar{s}_{a1}(t)\quad \bar{s}_{b1}(t)\quad \bar{s}_{c1}(t)]^T$ and $\mathbf{s}_{abc2}(t)=[s_{a2}(t)\quad s_{b2}(t)\quad s_{c2}(t)]^T$ are switching functions of the upper and lower cells of the M2L-VSC in Fig. 1(a). The generic switching function $s_{xj}(t)$ varies between 1 and 0 (where $x=a,\ b$ and c, and $j=1$ and 2), with '1' and '0' stand for on and off states of the switching devices $\bar{S}_{a1}$, $\bar{S}_{b1}$ and $\bar{S}_{c1}$ and S_{a2}, S_{b2} and S_{c2}. As stated in (1), the correct operation of the M2L-VSC requires the upper and lower arms of the same phase-leg to be operated in complementary manner (this means, insertion of the upper cell capacitor into power path in phase 'x' requires bypass of the lower cell capacitor of the same phase and vice versa). Such operation necessitates the cell capacitors and composite switching devices of the three-phase cells to be rated at the full dc link voltage (V_{dc}). With the above operation, the M2L-VSC generates only two voltage levels per phase as in the C2L-VSC. The three-phase output voltages and currents of the M2L-VSC represent the differential mode voltages and currents as in the conventional MMC:

$$\mathbf{v}_{abco}(t)=\mathbf{v}_{abc1}(t)-\mathbf{v}_{abc2}(t) \tag{4}$$

$$\mathbf{i}_{abco}(t)=\mathbf{i}_{abc1}(t)-\mathbf{i}_{abc2}(t) \tag{5}$$

Similarly, the common-mode voltages and currents are:

$$\mathbf{v}_{com}^{abc}(t)=\tfrac{1}{2}\left[\mathbf{v}_{abc1}(t)+\mathbf{v}_{abc2}(t)\right] \tag{6}$$

$$\mathbf{i}_{com}^{abc}(t)=\tfrac{1}{2}\left[\mathbf{i}_{abc1}(t)+\mathbf{i}_{abc2}(t)\right] \tag{7}$$

It worth emphasizing that, each cell of the M2L-VSC adheres to the same operational restrictions of the conventional two-level converter such as:

- Complementary operation of the switching devices of the same leg in order to prevent shoot-through at the cell level, i.e., $s_{a1,2}(t)+\bar{s}_{a1,2}(t)=1$, $s_{b1,2}(t)+\bar{s}_{b1,2}(t)=1$ and $s_{c1,2}(t)+\bar{s}_{c1,2}(t)=1$.
- Each switching device and cell capacitor blocks the full dc link voltage (V_{dc}). Therefore, for medium and high-voltage applications, series connection of switching devices is necessary.

Although the output voltage quality remains the same as in conventional two-level converter, the proposed structure provides a viable method for increasing the capacity of HVDC converters without the need to increase the rated dc link voltage. With the three-phase modulating signals being defined as $\mathbf{m}_{abc}(t)=\left[M\sin\omega t\quad M\sin(\omega t+\frac{4}{3}\pi)\quad M\sin(\omega t+\frac{2}{3}\pi)\right]^T$, the switched output voltages in (2) and (3) could be replaced by their average values as:

$$\mathbf{v}_{abc1}(t)=\tfrac{1}{2}V_{c1}(t)\left[\boldsymbol{\psi}-\mathbf{m}_{abc}(t)\right] \tag{8}$$

$$\mathbf{v}_{abc2}(t)=\tfrac{1}{2}V_{c2}(t)\left[\boldsymbol{\psi}+\mathbf{m}_{abc}(t)\right] \tag{9}$$

Besides sinusoidal pulse width modulation (SPWM), the M2L-VSC could be control using space vector modulation (SVM) or selective harmonic elimination (SHE), with SHE could reduce the switching frequency per devices considerably as demonstrated in [8]; hence, the switching losses.

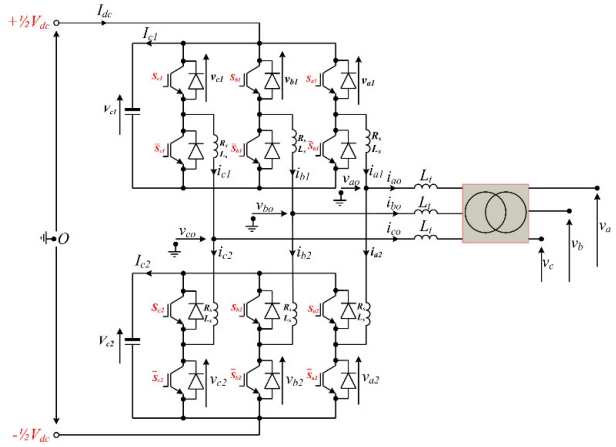


Fig. 1: Modular level voltage source converter

III. SIMULATIONS

Fig. 2 shows a M2L-VSC based point-to-point HVDC link that uses the parameters listed in Table I. Converter terminals connected to G_1 and G_2 regulate active power and dc link voltage respectively, and ac voltage at B_1 and B_2. Both converter terminals use two double tuned ac filters, targeted at 1st carrier frequency and dominant sidebands around the 1st and 2nd carrier frequencies, with the total filtering per converter is about 30% of the converter rating.

Table I: system parameters

Rated dc voltage	200kV (±100kV)
VSC_1 and VSC_2 rated apparent power	200MVA
VSC_1 and VSC_2 rated active power	180MW
VSC_1 and VSC_2 rated reactive power	±90MVAr
VSC_1 and VSC_2 rated ac voltage	100kV
Arm inductor (L_s)	10mH
Cell capacitance	100μF
Inductance of interfacing reactor	0.15pu
Transformer leakage inductance	0.1pu
Transformer rated power	200MVA
Transformer nominal voltage ratio	100kV/400kV
DC cable resistance	9mΩ/km
DC cable inductance	1.4mH/km
DC cable capacitance	0.26μF/km

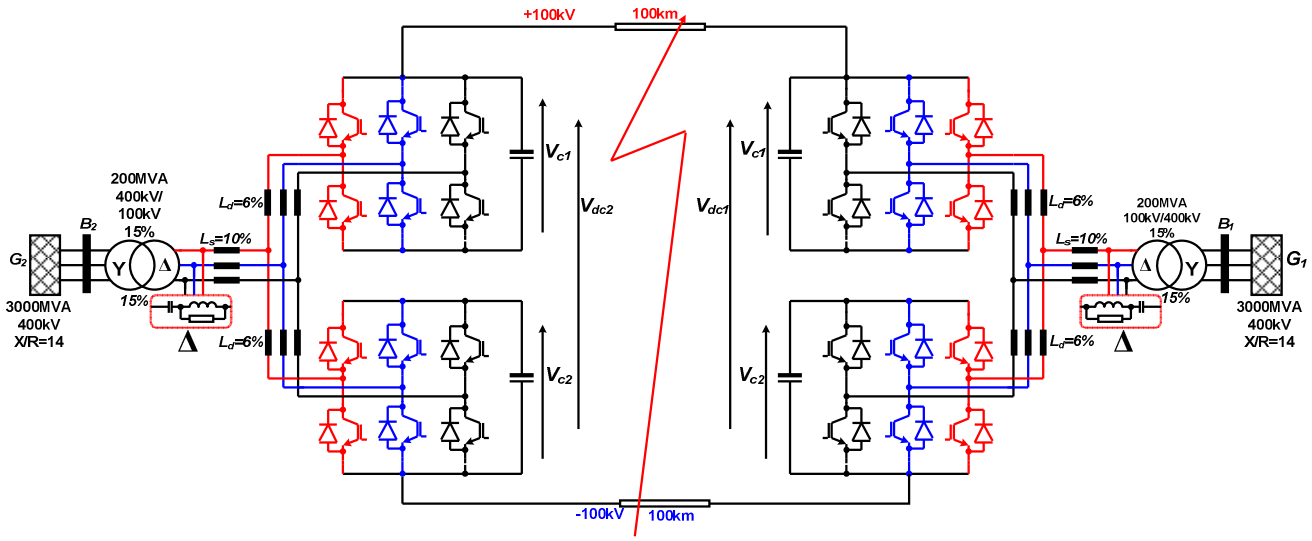


Fig. 2: two-terminal symmetrical monopolar HVDC link that employs modular two-level converters

IV. COMPARISON BETWEEN THE CONVENTIONAL AND IMPROVED TWO-LEVEL CONVERTERS

A) DC Short Circuit Fault

Fig. 3 presents a comparison between the M2L-VSC and C2L-VSC when both are simulated as terminal converters of a point-to-point HVDC link in Fig. 2, and employ the same controllers and subjected to pole-to-pole dc short circuit faults. To ensure that both converters have the same inertia and dc current ripples, the dc link capacitance of the C2L-VSC is set to be twice of the M2L-VSC shown in Table I.

Fig. 3(a) displays three-phase currents of the M2L-VSC (continuous lines) superimposed on that of the C2L-VSC (doted lines), all measured at the phase interfacing reactors. The plots in Fig. 3(a) indicate that the C2L-VSC draws larger ac currents than the M2L-VSC. The plots for the dc link currents which are measured at the dc terminals of the active power regulators in Fig. 3(b) show that the C2L-VSC contributes larger transient current to dc fault than the M2L-VSC, and this is because of discharge of its dc link capacitor. Nonetheless, the C2L-VSC retains small residual dc voltage across the dc link capacitors compared to practically zero in M2L-VSC case, and as a results, the C2L-VSC exhibits slightly lower steady-state dc fault current than the M2L-VSC. Fig. 3(c) displays the current in the switch S_{a1} of the upper cell of the M2L-VSC. Notice that the steady-state peak current of the switch S_{a1} is equal to that of the arm currents ($\frac{1}{3}I_{dc}+\frac{1}{2}I_m$), where I_{dc} and I_m are the dc link current and peak of the output current. Fig. 3(d) shows the current in the switch S_{a1} (phase '*a*' upper arm of the C2L-VSC). Observe that the peak current in the switch S_{a1} of the C2L-VSC is equal to the peak of the converter output current (I_m) during steady-state which is higher than that of the M2L-VSC, and its diodes are exposed to higher transient currents during dc fault compared to that of the M2L-VSC. When M2L-VSC is blocked during dc short circuit faults, the current contribution from ac grid to dc side flow through the diodes of the upper switches (S_{a1}, S_{b1} and S_{c1}) in the upper arms, and diodes of lower switches in the lower arms, see Fig. 3(e) and (f).

From the above discussions and results in Fig. 3, the following conclusions are drawn:

- The M2L-VSC has better transient response to dc short circuit faults than the C2L-VSC, see Fig. 3(a) and (b).
- For the same rated power, dc link voltage and ac side voltage, the switching devices 0f the M2L-VSC experience lower current stresses than the C2L-VSC, see Fig. 3(c) and (d).
- The fault currents in the freewheeling diodes of the C2L-VSC rise at slower rate than that of the M2L-VSC (as the dc link capacitors of the C2L-VSCs will prevent the rapid collapse of the dc link voltages zero, and help in retention of small residual dc voltage across the dc link), see Fig. 3(e).

B) Extension of Reactive Power Capability

This section compares the power density of the M2L-VSC to that of the C2L-VSC when both converters employ the same switching devices, assuming that the output phase current of phase '*a*' is $i_{a0}=I_m sin(\omega t+\varphi)$. Therefore, the upper and lower arm currents of the M2L-VSC will be $i_{a1}=I_d+\frac{1}{2}I_m sin(\omega t+\varphi)$ and $i_{a2}=I_d-\frac{1}{2}I_m sin(\omega t+\varphi)$ as in the conventional MMC; where, $I_d=\frac{1}{3}I_{dc}$, and I_m and I_{dc} represent the peak of the output phase currents and magnitude of the dc link current. Also, recall that the I_d could be expressed as $I_d=\frac{1}{4}mI_m cos\varphi$[9], where, m and φ are modulation index and power factor angle. Notice that the peak arm current for the C2L-VSC is the same as that of the output phase currents, while the peak arm currents of the M2L-VSC vary significantly with the power factor as illustrated above. The arm currents at two extrema, the zero and unity power factors are:

- At zero power factor, $I_d=0$, thus, $i_{a1}=+\frac{1}{2}I_m sin(\omega t+\varphi)$ and $i_{a2}=-\frac{1}{2}I_m sin(\omega t+\varphi)$, with $-\frac{1}{2}I_m \le i_{a1,2} \le \frac{1}{2}I_m$. This permits doubling of the reactive power capability of the M2L-VSC compared to that of the C2L-VSC.
- At unity power factor and unity modulation index, the arm currents of the M2L-VSC are $i_{a1}=\frac{1}{2}I_m(\pm\frac{1}{2}+sin(\omega t+\varphi))$ and $i_{a2}=\frac{1}{2}I_m(\pm\frac{1}{2}-sin(\omega t+\varphi))$ respectively, with $-\frac{3}{4}I_m \le i_{a1,2} \le \frac{3}{4}I_m$. These arm currents' inequalities indicate that the M2L-VSC is capable of generating more active power compared to C2L-VSC, without overstressing its switching devices.

To substantiate the above discussions, waveforms for zero power factor case when the M2L-VSC exchanges twice the rated apparent power of the C2L-VSC are presented in Fig. 4 and Fig. 5 respectively. The plots in Fig. 4 (a), (b) and (c) and Fig. 5 (a), (b) and (c) confirm the above discussions, with arm currents of both converters being compared have similar peak currents even though the M2L-VSC exchanges twice the reactive power of the C2L-VSC, with the output current of the M2L-VSC is twice that of the C2L-VSC.

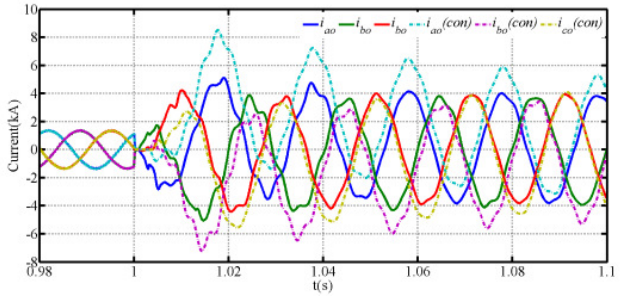
C) Semiconductor Losses

Table II presents semiconductor loss comparison between the C2L-VSC and M2L-VSC, using system parameters summarised in Table I, and 1200A and 2.5kV IGBT(T1200TD25A) from West-code, assuming that the

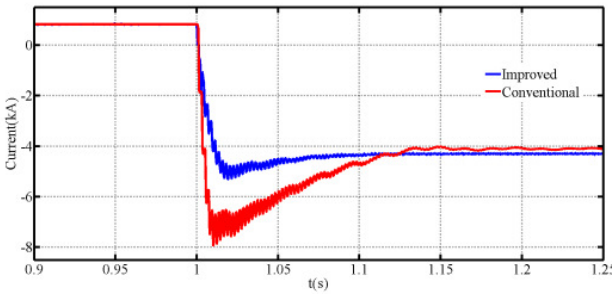
voltage stress per switch is 1.250kV. On-state and switching losses of the C2L and M2L VSCs are calculated based on the approach presented in [10-14], with some modification introduced to accommodate the asymmetry of the arm currents of the M2L-VSC as suggested in [7]. The accuracy of the analytical on-state loss calculations in Table II is confirmed using MATLAB simulation, where the switching devices average and root mean square currents are calculated directly from the simulation. It has been found that the margin of error between the two results is less than 1%. The switching losses are calculated assuming that the turn-on and turn-off energy losses are linear combination of device current at the turn on and turn off instances [15]. Table II shows that the M2L-VSC has lower on-state and switching losses compared to C2L-VSC, benefiting from the even split of the fundamental output ac current between the upper and lower arms of each phase-leg. The semiconductor losses in Table II are calculated assuming 2.1kHz switching frequency. Since these losses are predominantly switching losses, the adoption of optimized selective harmonic elimination with lower equivalent switching frequency such as 1.15kHz as employed in the conventional two-level converter of the Estlink HVDC link[16] can the overall semiconductor losses drastically.

Table II: Semiconductor power loss comparison between the C2L and M2L VSCs

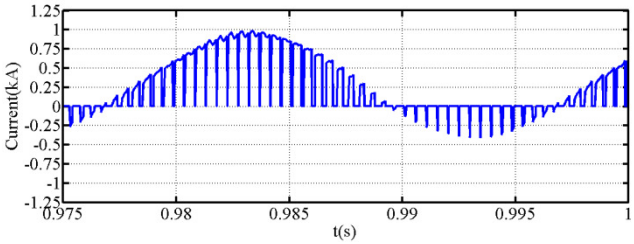
	C2L-VSC	**M2L-VSC**
Operating condition	P=180MW & Q=0	
On-state loss	1.4734 MW	1.1996MW
Switching loss	3.5016MW	3.0690MW
Total semiconductor losses	4.9750MW (2.76%)	4.2686MW (2.37%)
Operating condition	P=180MW & Q=90MVAr	
On-state loss	1.74MW	1.36MW
Switching loss	4.06MW	3.35MW
Total semiconductor losses	5.80MW (3.22%)	4.71MW (2.62%)
Operating condition	P=0 & Q=180MVAr	
On-state loss	1.38MW	1.03MW
Switching loss	3.50MW	2.71MW
Total semiconductor losses	4.88MW (2.71%)	3.74MW (2.08%)



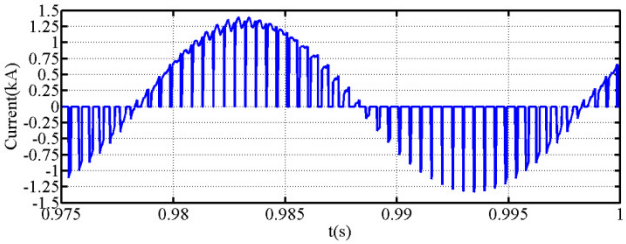
(a) Three-phase currents in the phase interfacing reactors of the M2L-VSC superimposed on that of the C2L-VSC



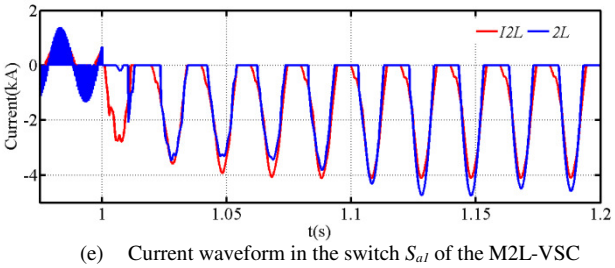
(b) dc link current at the dc terminal of M2L-VSC superimposed on that of the C2L-VSC (dc terminal of power controlling converter)



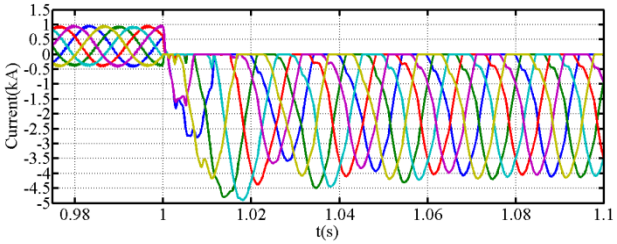
(c) Current waveform in the switch S_{a1} of the M2L-VSC, measured during steady-state



(d) Current waveform in the switch S_{a1} of the C2L-VSC, measured during steady-state

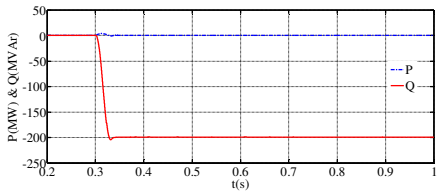


(e) Current waveform in the switch S_{a1} of the M2L-VSC superimposed on that of the C2L-VSC

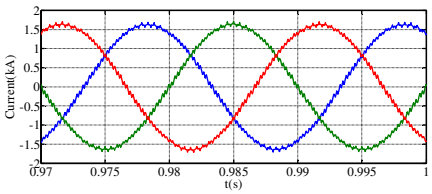


(f) six arm currents of the M2L-VSC

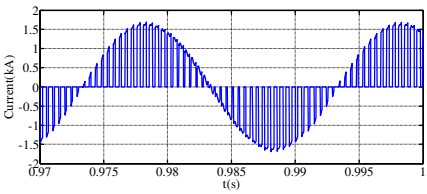
Fig. 3: Selected waveforms illustrate one-to-one comparison of the responses of the M2L-VSC against that of the C2L-VSC during pole-to-pole dc short circuit fault



(a) VSC_1 active and reactive powers

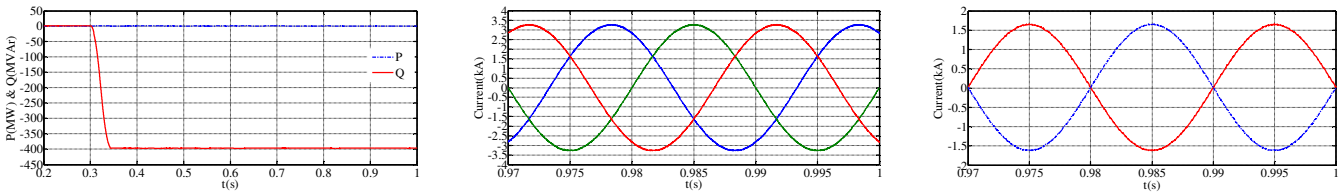


(b) VSC_1 three-phase output currents measured at converter side (low-voltage side of the interfacing transformer)



(c) Sample of the current in the upper arm of the phase a

Fig. 4: Waveforms of the conventional two-level converter when it exchanges -200MVAr with the ac grid



(a) VSC1 active and reactive powers (b) VSC_1 three-phase output currents measured at converter side (low-voltage side of the interfacing transformer) (c) Samples of the upper and lower arm' currents of the phase a

Fig. 5: Waveforms of the improved two-level converter when it exchanges -400MVAr with the ac grid

V. EXPERIMENTAL VALIDATION

This section presents experimental validation of the M2L-VSC when it is operating as grid connected inverter with 2.4kHz switching frequency, considering normal operation and dc fault. Fig. 6 displays the schematic diagram and picture of the experimental test rig of the M2L-VSC. It worth emphasizing that the total ac side reactance (phase interfacing and transformer leakage per phase) of the M2L-VSC is sized in similar way of that of the C2L-VSC, i.e., to limit the magnitude of the ac current in-feed during dc short circuit fault, and to be part of the ac side filtering (however, large value is detrimental operationally, as it narrows down the converter capability curve in over-excitation region). While the arm inductance is sized to ensure the followings: limit the *di/dt* on the diodes when converter is blocked during dc short circuit fault, and must be sufficient to prevent arm currents from becoming discontinuous and for filtering of the high frequency harmonic currents.

A) Closed loop:

Fig. 7 presents experimental waveforms of the M2L-VSC when it is injecting $i_d^*=5.5A$ and $i_q^*=0$ (equivalent to .94kW at unity power factor) into 50Hz ac grid with 140Vrms line-to-line voltage. Fig. 7 (a), (b) and (c) show the three-phase currents converter injects into ac grid superimposed on phase '*a*' voltage, phase '*a*' upper and lower arm superimposed on the converter output currents (measured at transformer secondary side which is connected to converter terminal), and upper and lower cell capacitor voltages and dc link current. The arm and phase currents in Fig. 7 (b) indicate that both arms of the M2L-VSC conduct simultaneously and consist of ac and dc components (I_d and $½i_{ao}$) as that of the conventional MMC, and as articulated in the theoretical discussions presented in section II. The experimental waveforms in Fig. 7 (c) show balanced cell capacitor voltages and exhibit no low frequency oscillations as in the conventional MMC, thanks to the use of three-phase cells that protect the cell capacitors from the fundamental currents.

Additional scenario that considers the case of zero power factor ($i_d^*=0$ and $i_q^*=5.5A$, which is equivalent to injection of 0.94kVAr inductive into ac grid) is presented in Fig. 8. The three-phase output currents (i_{ao}, i_{bo} and i_{co}) superimposed on the phase '*a*' grid voltage 'v_{ao}', upper and lower arm currents (i_{a1} and i_{a2}) overlaid on the converter side output phase current 'i_{ao}', and cell capacitor voltages (V_{c1} and V_{c2}) superimposed on the dc link current (I_{dc}) in Fig. 8 (a), (b) and (c) indicate the followings:

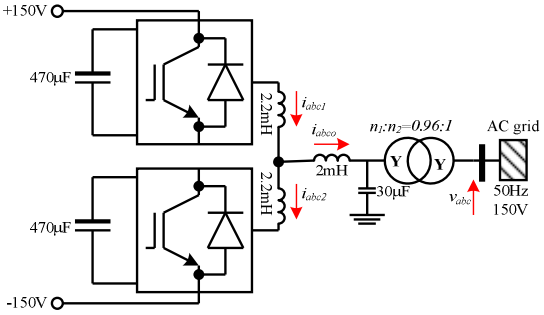
- The M2L-VSC exhibits similar behaviours as envisioned in section III, particularly, symmetry of the arm currents during zero power factor operation; hence, reduced current stresses on the switching devices compared to unity power factor case in Fig. 7 (b).
- Fig. 8 (b) and (c) show zero dc link current and zero dc component of the arm currents as $I_d=⅓I_{dc}=¼mI_m\cos 90^o=0$. These results support the accuracy of the theoretical discussions and analysis presented in previous sections.

B) Simulated dc short circuit fault:

Fig. 9 displays experimental waveforms of the M2L-VSC when it is subjected to a permanent dc short circuit fault. The dc fault is simulated by connecting 26Ω resistance across the dc link and a second resistor of 26Ω in series with the dc supply to act as voltage divider and limit the supply current. Fig. 9 (a) and (b) shows that when the M2L-VSC is blocked, the cell capacitor voltages remain flat at their pre-fault values when the dc link voltage collapses to 50% of the pre-fault value, and dc link current reverses its direction and the upper and lower arms only conduct through freewheeling diodes of the lead switches that bypass the cell capacitors as originally envisioned, and illustrated in sections II and III. These results support claim with regard to similarity of the transient response of the M2L-VSC to that of the conventional MMC.

VI. CONCLUSIONS

This paper has presented the M2L-VSC as a promising alternative the C2L-VSC for short distance HVDC transmission systems, with relatively low dc operating voltages and rated powers. The presented discussions, comparative simulations and experimental results reveal that the M2L-VSC offers the best trade-offs between semiconductor losses, waveforms quality, system complexity and superior transient response to ac and dc network faults compared to C2L-VSC.



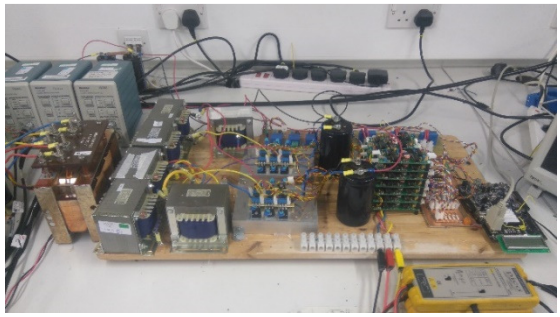
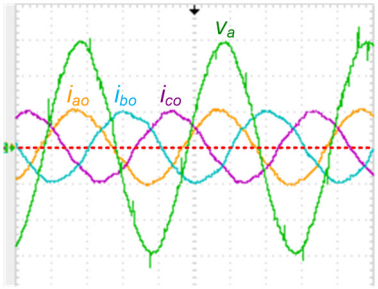
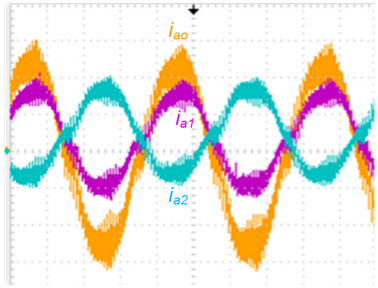


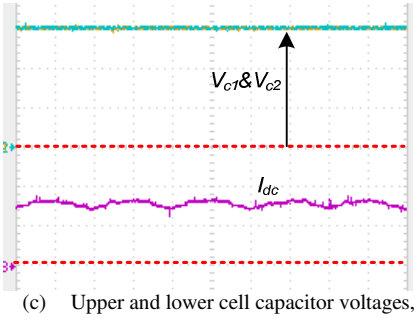
Fig. 6: Schematic diagram of the experimental test rig and its picture



(a) Three-phase currents converter injects into ac grid superimposed on phase 'a' of the grid voltage (5ms/div, 5A/div and 40V/div)

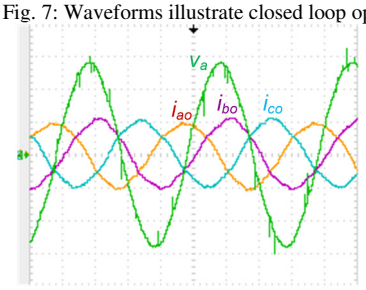


(b) Phase '*a*' upper and lower arm currents superimposed on phase 'a' output current(5ms/div, 2A/div)

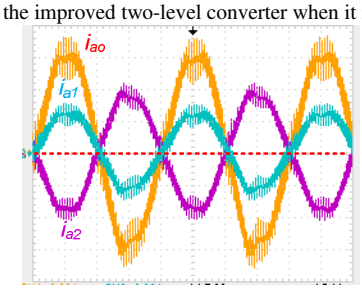


(c) Upper and lower cell capacitor voltages, V_{c1} and V_{c2}, and dc link current, I_{dc}(10ms/div, 2A/div and 100V/div)

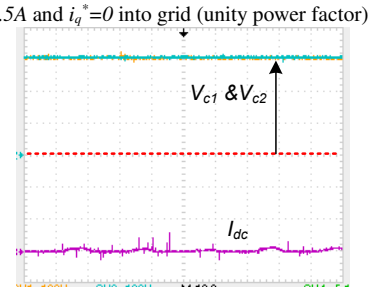
Fig. 7: Waveforms illustrate closed loop operation of the improved two-level converter when it injects $i_d^*=5.5A$ and $i_q^*=0$ into grid (unity power factor)



(a) Three-phase currents converter injects into ac grid superimposed on phase 'a' of the grid voltage (5ms/div, 5A/div and 40V/div)

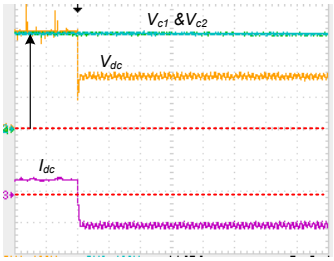


(b) Phase '*a*' upper and lower arm currents superimposed on its corresponding output phase current(5ms/div, 2A/div)

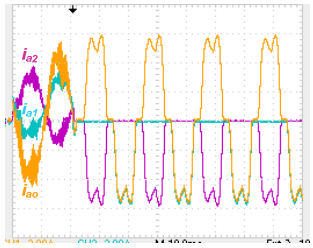


(c) Upper and lower cell capacitor voltages, V_{c1} and V_{c2}, and dc link current, I_{dc}(10ms/div, 2A/div and 100V/div)

Fig. 8: Waveforms illustrate closed loop operation of the improved two-level converter when it injects $i_d^*=0$ and $i_q^*=5.5$ into grid (zero power factor)



(a) DC link current and voltage, and cell capacitor voltages (25ms, 5A/div and 100V/div)



(b) Upper and lower arm and output phase currents (i_{a1}, i_{a2} and i_{ao})

Fig. 9: Experimental waveforms that illustrate response of the improved two-level converter to dc short circuit

VII. ACKNOWLEDGMENT

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