Efficient base driver circuit for silicon carbide bipolar junction transistors

N. McNeill✉, B.H. Stark, S.J. Finney, D. Holliday and H. Dymond

The silicon carbide bipolar junction transistor needs large transient currents supplied into and out of its base terminal for rapid switching. To realise this, it is normally desirable to have a base driver circuit supply rail at a high voltage. However, the device also needs a steady base current to hold it in the on-state. Supplying this current from a high-voltage source is inefficient. A circuit is presented that applies high transient base–emitter voltages, but with low driver circuit power consumption.

Introduction: Of the possible silicon carbide (SiC) devices for high-efficiency power conversion [1], the SiC bipolar junction transistor (BJT) [2] has attractive properties. Unlike the silicon BJT, it does not exhibit significant charge-storage time delays or current-tailing at turn-off. It has a common-emitter current gain h_{FE} of typically 100 compared to the values as low as 5–10 with the silicon power BJT. Furthermore, it does not have the safe operating area or short-circuit limitations of its silicon counterpart [3]. Although the SiC BJT still needs a steady-state base drive current in the on-state, and does not have a reverse conducting capability, it has low inter-terminal capacitances for a given on-state resistance. This feature is desirable for high efficiencies as capacitive charging and discharging currents lead to power dissipation in the power devices and driver circuitry. Its base drive requirements are robust. It can withstand a high negative base–emitter voltage of typically 30 V. Also, it does not need a carefully limited on-state voltage as the base–emitter junction is a p-n type that clamps the applied voltage to a level $V_{BE(on)}$ of ~3 V and can tolerate large transient currents. The SiC MOSFET presents challenges including gate oxide reliability [4] and susceptibility to dv/dt-induced conduction [5]. The SiC JFET is fast-switching, but is usually realised as a normally-on structure to attain a low on-state resistance. It is therefore typically connected in a cascode arrangement with a silicon MOSFET to form a normally-off switch [6].

Fig. 1 shows a standard base driver circuit [7] driving a SiC BJT TR1 in a buck converter. The driver IC U1 supplies the steady base current i_B via R1. i_B is given by

$$i_B = \frac{i_C}{h_{FE}} \quad (1)$$

where i_C is TR1's collector current. As with other power devices, a negative off-state drive voltage $-V_{DRI}$ is normally desirable to avoid dv/dt-induced conduction when the BJT is used in voltage source converter bridge-legs. The speed-up capacitance Cp supplies high transient i_B currents into and out of TR1's base terminal for rapid switching. R2 provides damping [7]. Ideally, the difference between $+V_{DRI}$ and $V_{BE(on)}$ would be small, as this means that the power is drawn from $+V_{DRI}$ and the power dissipation in R1 are both low. However, at TR1 turn-on, little voltage is therefore available for applying across the parasitic series impedances lying in the transient i_B current route encompassing Cp and R2. A high voltage is needed to establish the large peak i_B currents required for rapid, and therefore low-loss, switching.

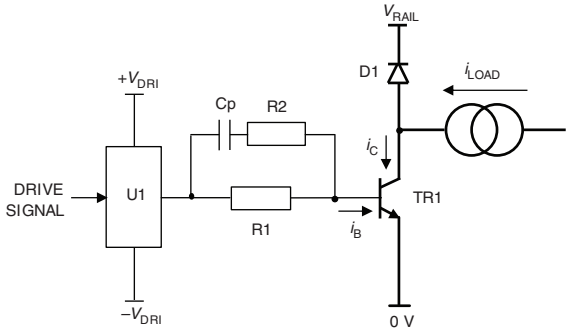

Fig. 1 *Base driver circuit*

A solution to the problem of base driver power dissipation [7] would be that outlined in Fig. 2. A high-voltage rail $+V_{DRI}$ (*high*) is used to drive the high transient i_B currents through Cp. A second driver IC U2 is supplied from a second lower voltage positive rail $+V_{DRI}$ (*low*) and sources the steady on-state i_B current through R1. A disadvantage of this circuit is the need for two positive-going driver circuit supply rails.

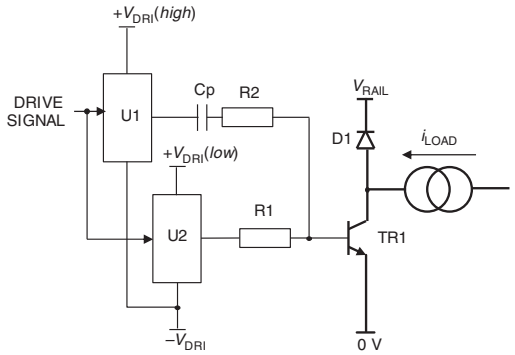

Fig. 2 *High-efficiency dual-source base driver circuit*

Proposed base driver circuit: The circuit of Fig. 3 provides high base-drive currents to achieve fast switching, along with an efficient supply of the steady-state i_B when the BJT is on. Only one positive supply rail $+V_{DRI}$ is used. Instead of a second high-voltage positive rail, the bootstrapping circuitry consisting of Cp, D3, R2, TR2 and U2 operates in conjunction with the negative supply rail $-V_{DRI}$ to apply a high transient base–emitter voltage at TR1 turn-on.

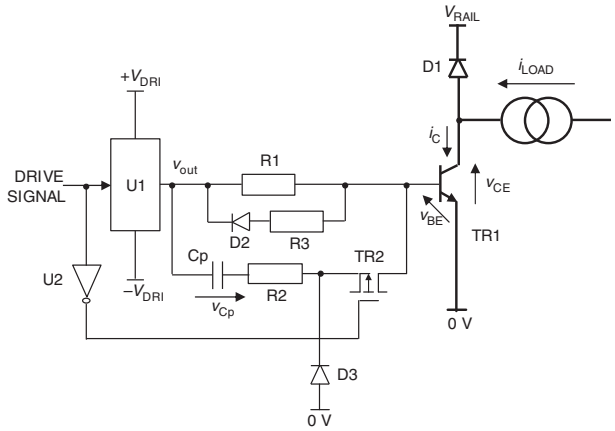

Fig. 3 *Proposed base driver circuit*

An alternative technique for efficiently driving a SiC BJT whilst using a low-voltage positive driver circuit supply rail is presented in [8]. Bootstrapping circuitry is also used in [8] and the circuit also has a negative driver circuit supply rail. No auxiliary switches such as TR2 in Fig. 3 are used. However, unlike the proposed circuit, the base terminal during the off-state is not clamped to the full negative driver circuit rail voltage via a route with a low DC impedance, as formed by D2 and R3 in Fig. 3. Also, whereas the proposed circuit applies a transient voltage equal to the aggregate supply voltage of $+V_{DRI}$–($-V_{DRI}$) to the BJT's base–emitter junction at turn-on, the voltage applied in [8] is lower.

Operation of the proposed circuit in Fig. 3 over a switching cycle is as follows, starting with TR1 in the steady on-state

(i) When TR1 is on, U1 sources the required steady i_B into the base of TR1 via R1. U1 is supplied from the voltage rails $+V_{DRI}$ and $-V_{DRI}$. The P-channel MOSFET TR2 is on, but no current flows through it in the steady on-state, as Cp is blocking. $+V_{DRI}$ is set at a voltage that is only slightly higher than $V_{BE(on)}$. Consequently, the power drawn from $+V_{DRI}$ and the power dissipation in R1 are both low.
(ii) At TR1 turn-off, its base is pulled down to $-V_{DRI}$ by U1 via D2 and damping resistor R3. $-V_{DRI}$ can be large as the SiC BJT's base–emitter junction can typically support a reverse voltage of up to 30 V and has a high DC impedance when reverse biased. A penalty due to $-V_{DRI}$ being large is higher losses associated with charging and discharging TR1's

input capacitance. However, making $-V_{DRI}$ large is desirable to mitigate susceptibility to dv/dt-induced conduction. Furthermore, a higher voltage is applied across the parasitic series impedances in the transient i_B route during TR1 turn-on, reducing switching losses. An advantage of the proposed circuit where $+V_{DRI}$ is low is that the total supply voltage $+V_{DRI}$–($-V_{DRI}$) that U1 and U2 have to be rated for is minimised for a given $-V_{DRI}$. TR2 is turned off when TR1 turns off.

(iii) When TR1 is off, Cp charges from $-V_{DRI}$ via R2 and D3 such that v_{Cp} reaches –($-V_{DRI}$). As TR2 is now off, it prevents D2, D3 and R3 from effectively presenting a short-circuit between 0 V and $-V_{DRI}$.

(iv) At TR1 turn-on, TR2 is turned on and the voltage applied across the series combination of R2, the base–emitter junction of TR1 and the associated parasitic impedances is $+V_{DRI}$–($-V_{DRI}$). Ideally, an N-channel MOSFET would be used in location TR2 and would be driven by connecting its gate to U1's output signal v_{out}. However, a gate-source voltage of only $+V_{DRI}-V_{BE(on)}$ is available to turn TR2 on. As this voltage is intentionally made low here, it is insufficient to turn on a standard N-channel MOSFET. TR2 is, therefore, a P-channel MOSFET and is driven with a complementary drive signal produced by the inverting driver IC U2. It is noted that U2 does not need to have the same high-current output capability as U1.

Experimental results: The circuit in Fig. 3 was prototyped with the components listed in Table 1. Fig. 4 shows experimental waveforms.

Table 1: Component details for experimental circuit

R1	10 Ω, film
R2, R3	4.7 Ω, film
Cp	22 nF, ceramic
D1	C2D20120
D2,3	1N4148
TR1	GA10JT12–247
TR2	FQT3P20TF
U1	IXDN614PI
U2	TC4431EPA

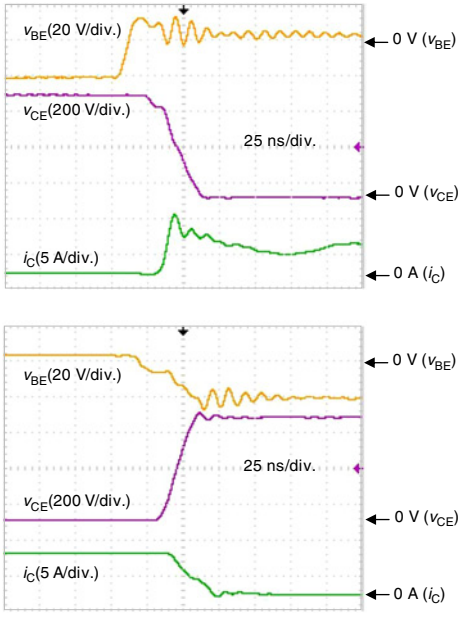

Fig. 4 *Waveforms from circuit in Fig. 3. Top: turn-on. Bottom: turn-off*

$+V_{DRI}$ and $-V_{DRI}$ were 5 and −20 V, respectively. V_{RAIL} was 600 V. TR1 was switched at 50 kHz and at a duty factor of 50%. The average load current i_{LOAD} was 4.44 A. Due to current ripple, the peak i_{LOAD} was 5.60 A. $V_{BE(on)}$ was taken as 3 V. The h_{FE} of the GA10JT12–247 device is quoted at 100, but this is only for the condition where the BJT has entered the linear region. The quoted h_{FE} was therefore de-rated by a factor of 1.5 to ensure hard on-state saturation. Also, h_{FE} is quoted at a junction temperature of 25°C but falls with temperature, so it was then further de-rated by a factor of two to allow for operation at typical temperatures of ∼100°C. The working gain was therefore taken as 33. At the peak i_C of 5.60 A in TR1, an i_B of 170 mA is required. The on-state voltage across R1 is given by $+V_{DRI}-V_{BE(on)}$. As $+V_{DRI}=5$ V and $V_{BE(on)}=3$ V, then this is 2 V. R1 was therefore set at 10 Ω to give an i_B of ∼200 mA. To minimise the diode junction capacitance charging current sourced by TR1, only one of the diodes in the dual common-cathode package in location D1 was connected. As shown in Fig. 3, the drive signal was applied directly to the inputs of U1 and U2, and no allowance was made for differing propagation delays through these driver ICs or TR2. The rise- and fall-times of v_{CE} were measured at 17.9 and 23.4 ns, respectively, using the Tektronix TDS 2014B oscilloscope measurement function. The power consumption of the driver circuit was measured at 1.37 W.

Conclusion: A high-efficiency base driver circuit for SiC BJTs has been presented. The circuit only requires one positive supply rail, which is set at a low voltage to ensure that the required steady on-state base current is sourced efficiently. Bootstrapping circuitry operating in conjunction with the negative supply rail enables a high transient base–emitter voltage to be applied at turn-on of the BJT. Experimental results are given when driving a SiC BJT switching 600 V and 4.44 A in a buck converter.

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One or more of the Figures in this Letter are available in colour online.

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