

# Design of DC-line terminating inductors for enhancement of protective functions in MTDC grids

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Dimitrios Tzelepis<sup>1</sup> ✉, Adam Dysko<sup>1</sup>, Campbell Booth<sup>1</sup>, Sohrab Mirsaiedi<sup>2</sup>, Xinzhgou Dong<sup>2</sup>

<sup>1</sup>Department of Electronic & Electrical Engineering, University of Strathclyde, Glasgow, UK

<sup>2</sup>Department of Electrical Engineering, Tsinghua University, Beijing, People's Republic of China

✉ E-mail: dimitrios.tzelepis@strath.ac.uk

**Abstract:** This study presents a detailed DC-side fault analysis considering inductive termination of lines within a high-voltage multi-terminal direct current (MTDC) grid. The analysis aims to provide design guidelines for DC-side inductors, taking into account important aspects of protection such as the required speed of operation of relays and the performance characteristics of current interruption devices (i.e. of DC circuit breakers). Moreover, the impact of current limiting inductors on the fault signatures is investigated. In particular, it has been found that DC-side inductors not only limit the fault current level, but also the resulting signatures in voltage and current, can assist to enhance the speed of operation, stability and selectivity of protective functions for DC-side faults. The analysis has been extended to include the impact of inductive termination on fast transient phenomena known as travelling waves. Specifically, DC-side inductors can form a significant reflection boundary for the generated travelling waves. A deeper insight into the faults has been achieved by utilising wavelet transform.

## 1 Introduction

High-voltage direct current (HVDC) power transmission is becoming increasingly competitive compared to high-voltage-alternating-current power transmission, especially for bulk power transmission over long distances. This is because of many technical and economical advantages introduced by HVDC-based transmission technology, utilising the most recently developed voltage source converters (VSCs). Those advantages include bulk power transfer over long distances [1] (notably from offshore wind [2]), upgrading existing AC networks [3], the interconnection of asynchronous grids and black start capability [4]. For the practical implementation and operation of multi-terminal direct current (MTDC) grids there are several outstanding issues to be solved. Major categories of these include power flow control [5], dynamic behaviour and stability [6], grid support and system integration [7] and finally, fault management [8, 9] (i.e. protection, fault location and fault ride through).

With regards to protection, DC-side faults are characterised by large inrush currents escalating over a short period of time [10, 11]. After the occurrence of a feeder fault on a transmission system, protection systems are expected to minimise its detrimental effects, by initiating clearing actions such as selective tripping of circuit breakers (CBs). As such, there is a need for transient DC-fault characterisation and subsequent development of a discriminative, fast, sensitive and reliable DC protection method. Up to now, there are a few schemes reported in the open literature for MTDC networks. For the implementation of non-communication-based schemes (i.e. non-unit) in MTDC networks, there is a noteworthy trend towards the placement of DC reactors at both ends of transmission lines. The intentional placement of such inductive components reduces the rate of rise of DC current, while it changes the resulting DC voltage signatures. Based on the fact that the voltage is different, depending on the faulted line, DC inductors can assist towards the implementation of a discriminative protection system [12–15]. In [12], a two-stage protection scheme is proposed by utilising under-voltage and voltage derivative criteria. In the reported work, the principles of non-unit protection are developed taking into account the reflection of travelling waves at an inductive termination. For the reported studies an inductor of 25 mH has been utilised, while the impact of the inductance value selection on voltage signatures has been numerically investigated. In [13], the DC voltage derivative (calculated from the line side of

the reactor) is utilised for fast detection and localisation of DC-side faults. In such studies, a 100 mH inductance is placed at line terminals. In [14], the rise rate of the DC reactor voltage with predefined voltage thresholds is utilised to provide fast and discriminative protection in a meshed MTDC system. In this work, the inductor value has been set to 200 mH. In [15], a method based on the ratio of transient voltages (calculated by voltage measurements at both sides of current-limiting inductors of 10 mH), is proposed. In the work conducted in [16], 150 mH inductors are utilised to reduce the rate of rise of DC current, and hence provide a time margin to perform high-speed differential protection.

Lumped inductors also play a major role in the design of dedicated DC breakers, which is a key facet for the clearance of DC faults and hence the realisation of meshed MTDC grids. The intentional placement of inductors within DC breaker's circuit provides a high impedance path which can reduce the rate of rise of DC current [17–20], but also facilitate the creation of current zero-crossing and arc extinction [21, 22]. The inductor placement on the HVDC transmission system is also an interesting research topic for DC fault ride-through [23], and for offshore wind farm considerations [24].

The literature review carried out on the utilisation of DC-line inductors revealed that much of the reported research does not provide solid explanations or guidelines for the choice of inductor value. This paper aims to provide such design guidelines, taking into account important aspects, including the required speed of operation of the relays and the performance characteristics of DC-CBs. Moreover, the impact of current limiting inductors on the post-fault voltage signatures is investigated.

## 2 DC inductor design

For the correct sizing of the inductor the following parameters should be taken into consideration:

- DC voltage.
- Type of fault.
- Operation time of DC-CBs.
- Maximum current the system can interrupt or sustain.
- Any other (known or estimated) time delays.

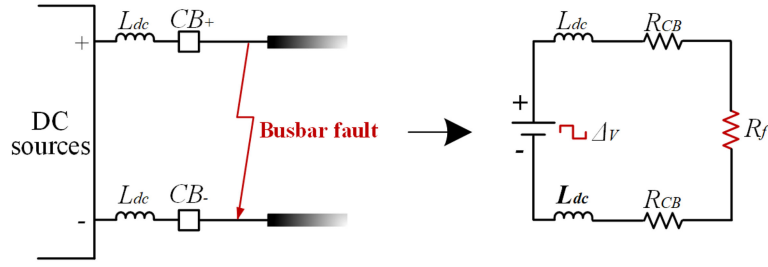


Fig. 1 Equivalent circuit of DC busbar fault for  $L_{dc}$  sizing

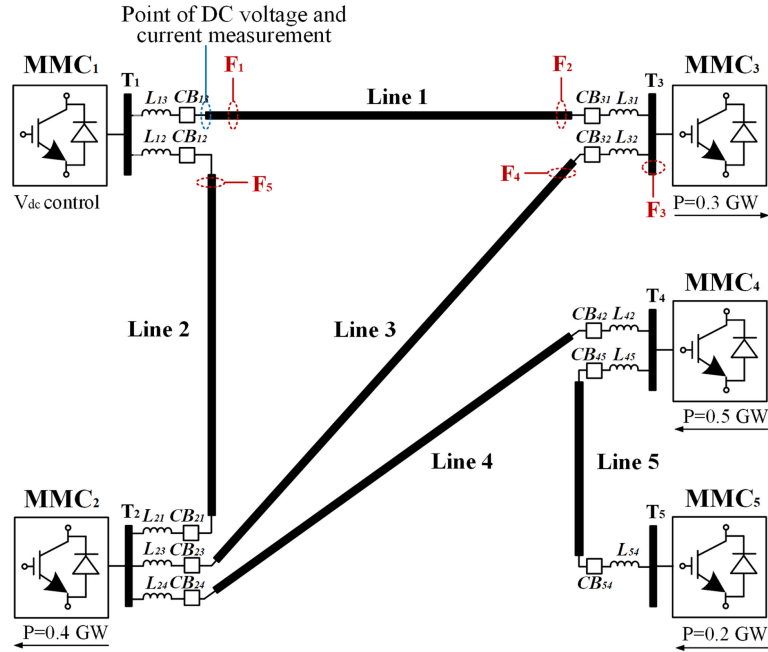


Fig. 2 Five-terminal MTDC grid

The calculation of inductance  $L_{dc}$  is performed in three steps, as described by (1)–(3). The first step is the calculation of the total operation time  $t_{op}$  of the protection system (including fault detection and isolation), given below:

$$t_{op} = t_{CB} + t_{IED} + t_{meas} \quad (1)$$

where  $t_{CB}$  is the operation time of CB,  $t_{IED}$  is the processing time delay of the IED, and  $t_{meas}$  contains any additional time delays related to the acquisition of the required measurements. Any other known or estimated delays shall also be added at this point. The total operation time  $t_{op}$  is then utilised for the calculation of the expected current rate of rise  $di_{dc}/dt$ , given by

$$di_{dc}/dt = \frac{I_{dc} - \max}{t_{op}} \quad (2)$$

where  $I_{dc-max}$  is the maximum DC current which the system can interrupt or sustain. It is recommended that for  $I_{dc-max}$ , the maximum breaking current of the available DC-CB should be used.

For the final step, the worst-case fault type and the resulting voltage drop should be considered. Typically, the worst fault scenario for VSC-based grids is a solid (i.e. fault resistance  $R_f \neq 0$ ) pole-to-pole fault at the converter terminals (see Fig. 1). In this case, the expected voltage drop would reach 100% assuming that any other resistance in the fault path (i.e. breaker resistance  $R_{CB}$  at normal operation) can be neglected. Finally, the inductance value  $L_{dc}$  can be calculated as

$$L_{dc} \geq \frac{\Delta V_{dc}}{di_{dc}/dt} \quad (3)$$

where  $\Delta V_{dc}$  is the expected maximum voltage drop. It should be noted that (3) will produce the value of the inductance  $L_{dc}$  for one pole if the single-pole voltage is used. Alternatively, if the pole-to-pole voltage is utilised, the resulting inductance will be equal to  $2L_{dc}$ .

### 3 Simulation results

#### 3.1 Modelling

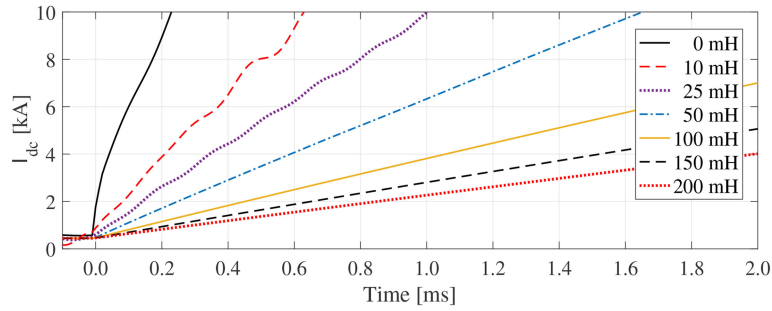
In this section, DC-side faults and their associated generated transient phenomena are analysed. For such an analysis, a five-terminal MTDC grid (illustrated in Fig. 2) has been developed. The system architecture has been adopted from the Twenties Project case study on DC grids. There are five 400-level, Modular Multilevel Converters operating at  $\pm 400$  kV (in symmetric monopole configuration), hybrid CBs (HbCBs), and current limiting inductors at each transmission line end. Transmission lines have been modelled by adopting distributed parameter model, while for the DC breaker a hybrid design by ABB [20] has been considered. The parameters of the AC and DC network components are described in detail in Table 1.

#### 3.2 Inductor sizing

An example of inductor sizing is presented here taking into account the guidelines presented in Section 2. The total operation time  $t_{op}$  has been estimated as 3.3 ms, considering that  $t_{CB} = 2$  ms (operation time of ABB HbCB),  $t_{IED} = 1$  ms and  $t_{meas} = 0.3$  ms. Values of  $t_{IED}$  and  $t_{meas}$  have been estimated taking into account that local measurements will be utilised for protection relays. The rate of rise  $di_{dc}/dt$  is calculated considering that maximum  $I_{dc-max}$  is set to 9 kA, which corresponds to the maximum breaking current

**Table 1** MTDC network parameters

Parameter	Value
DC voltage, kV	±400
DC inductor, mH	150
line resistance, Ω/km	0.015
line inductance, mH/km	0.96
line capacitance, μF/km	0.012
line lengths (1–5), km	180, 120, 500, 150, 100
AC frequency, Hz	50
AC short-circuit level, GVA	40
AC voltage, kV	400

**Fig. 3** Rate of rise of DC current with different inductance values, for a solid pole-to-pole fault at terminal  $T_1$ **Table 2** Time indices at 9 kA

inductance, mH	0	10	25	50	100	150	200
time, ms	0.22	0.60	0.93	1.49	2.70	3.97	5.31

**Table 3** Description of fault scenarios

Scenario	Description
$F_1$	close-up internal fault at Line 1 (15 km from $T_1$ )
$F_2$	remote internal fault at Line 1 (179 km from $T_1$ )
$F_3$	busbar external fault at Busbar 3
$F_4$	forward external fault at Line 3 (5 km from $T_3$ )
$F_5$	reverse external fault at Line 2 (5 km from $T_1$ )

of HbCB. As such, the rate of rise  $di_{dc}/dt = 9 \text{ kA}/3.3 \text{ ms} = 2.73 \text{ kA/ms}$ .

Inductance value  $L_{dc}$  is calculated considering the worst-case scenario, which would be a solid fault at any busbar of MTDC network illustrated in Fig. 2. Taking into account that CBs are not activated during the initial phase of the fault, their resistance  $R_{CB}$  can be taken as zero. Since the worst case is a solid fault, the corresponding fault resistance  $R_f$  can also be treated as zero. Consequently, based on the proposed ±400 kV network and for a solid fault at any busbar, the inductance value should be  $L_{dc} \geq 400 \text{ kV}/2.73 \text{ kA/ms} \rightarrow L_{dc} \geq 146.5 \text{ mH}$ .

For clarity, Fig. 3 illustrates the simulation results for a pole-to-pole solid fault at terminal  $T_1$  (see Fig. 2), triggered at  $t = 0 \text{ ms}$  with 2 ms post fault data for different inductance values.

Table 2 presents the time required to reach 9 kA for the inductances illustrated in Fig. 3. As calculated by (3), it is therefore verified that the inductance value of 150 mH is the most appropriate option.

### 3.3 Impact of DC inductors on fault generated voltage signatures

In order to investigate the impact of inductive line termination on transient phenomena, studies on five different fault scenarios have been carried out. The location of these faults is depicted in Fig. 2 and further explained in Table 3. It should be noted that for those cases, the voltage and current measurements have been captured at

the line side of  $L_{13}$ . In this convention, fault  $F_1$  is considered close-up internal,  $F_2$  is considered remote internal,  $F_3$  is a busbar fault (external),  $F_4$  is a forward external fault and  $F_5$  is a reverse external fault.

For the analysis of the fault scenarios presented in Table 3, it is of major importance to define the equivalent inductance  $L$  from point of measurement (i.e. line side of  $L_{13}$ ) to the actual fault. These have been calculated and included in Table 4.

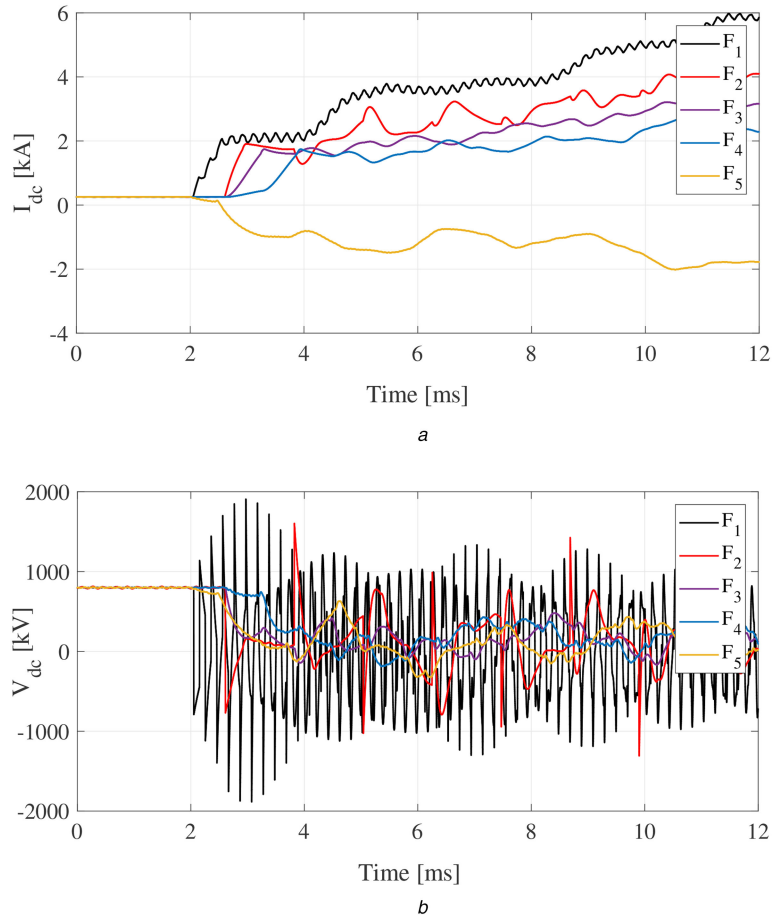
Fig. 4a illustrates the current feed of Line 1 for fault scenarios  $F_1$  to  $F_5$ . As expected, after the fault trigger at  $t_{\text{fault}} = 2.0 \text{ ms}$  high currents flow through Line 1. Even though travelling waves (and their associated propagation delays corresponding to fault location) are present in current measurements, the distinctive features for fault discrimination are visibly attenuated. The only apparent feature relates to the fault  $F_5$  where power and hence the current reversal are observed. For this reason, the nature of the fault is better investigated by utilising voltage measurements. For each fault scenario, the voltage response is depicted individually in Fig. 5. In addition, the voltage measured at terminal  $T_1$  is also included to better demonstrate the significance of current limiting inductors.

In all cases, there is a significant difference between the two captured voltage waveforms for internal faults  $F_1$  and  $F_2$  (Figs. 5a and b, respectively). These appear to have distinctive sharp edges which are more pronounced on the line side of inductor  $L_{13}$  (as the measuring point is closer to the fault and does not have any lumped reactor in-between). As for external faults  $F_3$ ,  $F_4$  and  $F_5$ , the

**Table 4** Equivalent inductance  $L$  from point of measurement to the fault (corresponding to scenarios  $F_1$  to  $F_5$  – Table 3)

Scenario	Inductance	Value, mH
$F_1$	$L_{L1} \times d_{L1}$	14.4
$F_2$	$L_{L1} \times d_{L1}$	171.84
$F_3$	$(L_{L1} \times l_{L1}) + L_{31}$	322.8
$F_4$	$(L_{L1} \times l_{L1}) + L_{31} + L_{32} + (L_{L3} \times d_{L3})$	477.6
$F_5$	$L_{13} + L_{12} + (L_{L2} \times d_{L2})$	304.8

$L_{L1}, L_{L2}, L_{L3}$  are the inductances per kilometre of Lines 1–3, respectively,  $l_{L1}, l_{L2}, l_{L3}$  are the total lengths of Lines 1–3, respectively and  $d_{L1}, d_{L2}, d_{L3}$  are the distances to fault for faulted Lines 1–3, respectively

**Fig. 4** DC voltage and current response corresponding to fault scenarios  $F_1$  to  $F_5$ 

(a) DC currents, (b) DC voltages

voltage response is more gradual and there are no sharp edges on the voltage waveforms. This is expected since, for any external fault, the equivalent inductance included in the fault current path is always significantly larger than for the internal fault due to the installed lumped reactors (see Table 4).

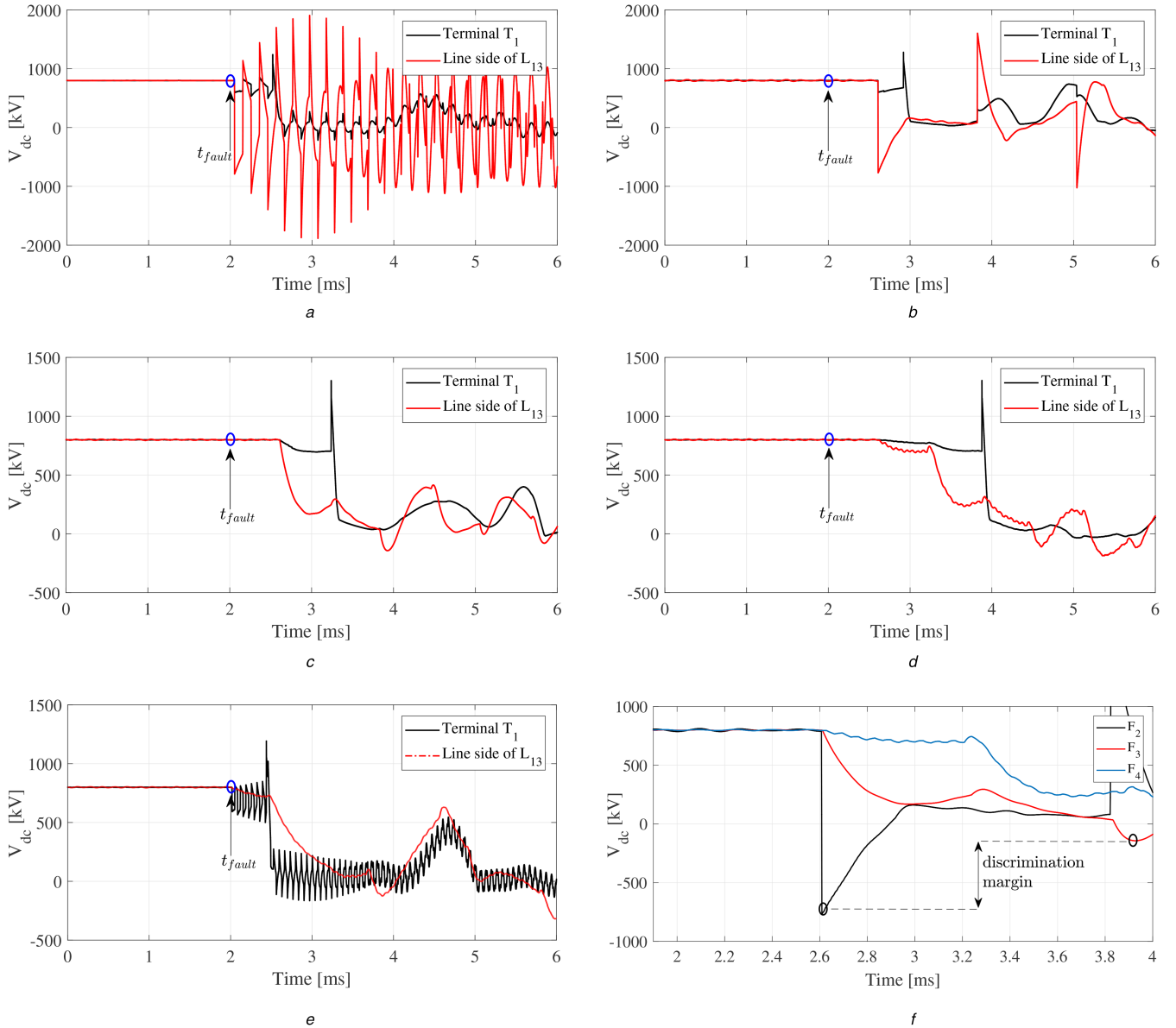
A challenge for those five fault scenarios would be the discrimination between  $F_2, F_3$  and  $F_4$  as they are practically in the same location separated by different values of lumped inductors. Such discrimination would be very useful in the context of protection. By observing the expanded view area depicted in Fig. 5f for faults  $F_2, F_3$  and  $F_4$ , it can be seen that for the remote internal fault (i.e.  $F_2$ ) the magnitude of the first voltage travelling wave reaches the lowest value ( $\sim 700$  kV). However, for any external faults (i.e.  $F_3$  and  $F_4$ ), DC voltage falls down until  $-170$  kV. This gives 2000 a relatively wide margin to achieve reliable discrimination based on under-voltage criteria. The same logic could be applied by adopting rate of change of DC voltage, but challenges related to noise are expected to arise.

Even though the level of DC voltage can assist towards the discrimination of faulted feeders, there is a significant challenge related to fault resistance  $R_f$ . Specifically, the highly-resistive fault can impose a smaller voltage drop and hence it would be difficult

to set voltage thresholds. As such, the wavelet transform is a possible solution to mitigate these challenges.

### 3.4 Impact of DC inductors on travelling wave based detection

It has been demonstrated in Section 3.3 that the inductive termination of transmission lines forms a significant boundary between DC voltage and current signatures; this was demonstrated both for internal and external faults. The difference is more significant for the DC voltage traces than for the current. However, difficulties may arise regarding voltage threshold selection under highly-resistive faults. To address this issue and further investigate the impact of inductive termination on the detection of travelling waves, the DC voltage measurements captured for fault scenarios  $F_1$  to  $F_5$  presented in Section 3.3, have been analysed through wavelet transform. The wavelet transform of a function  $v(t)$  can be expressed as the integral of the product of  $v(t)$  and the daughter wavelet  $\Psi_{a,b}^*(t)$ . The daughter wavelet  $\Psi_{a,b}^*(t)$  is a scaled and shifted version of the mother wavelet  $\Psi_{a,b}(t)$ . Scaling is implemented by  $a$  which is the binary dilation (also known as scaling factor) and shifted by  $b$ , which is the binary position (also known as shifting or



**Fig. 5** Voltage response (measured both at Terminal  $T_1$  and line side of  $L_{13}$ ) for fault scenarios described in  $F_1$  to  $F_5$   
 (a) Fault scenario  $F_1$ , (b) Fault scenario  $F_2$ , (c) Fault scenario  $F_3$ , (d) Fault scenario  $F_4$ , (e) Fault scenario  $F_5$ , (f) Discrimination margin between  $F_2$ ,  $F_3$  and  $F_4$

translation). If the function  $v(t)$  and mother wavelet  $\Psi_{a,b}(t)$  are real functions then the resulting  $WT_{\Psi_{a,b}}v(t)$  is also a real function. In any other case, the mother wavelet  $\Psi_{a,b}(t)$  and the resulting  $WT_{\Psi_{a,b}}v(t)$  are complex functions.

$$WT_{\Psi_{a,b}}v(t) = \int_{-\infty}^{+\infty} v(t) \underbrace{\frac{1}{\sqrt{a}}\Psi\left(\frac{t-b}{a}\right)}_{\text{daughter wavelet } \Psi_{a,b}^*(t)} dt \quad (4)$$

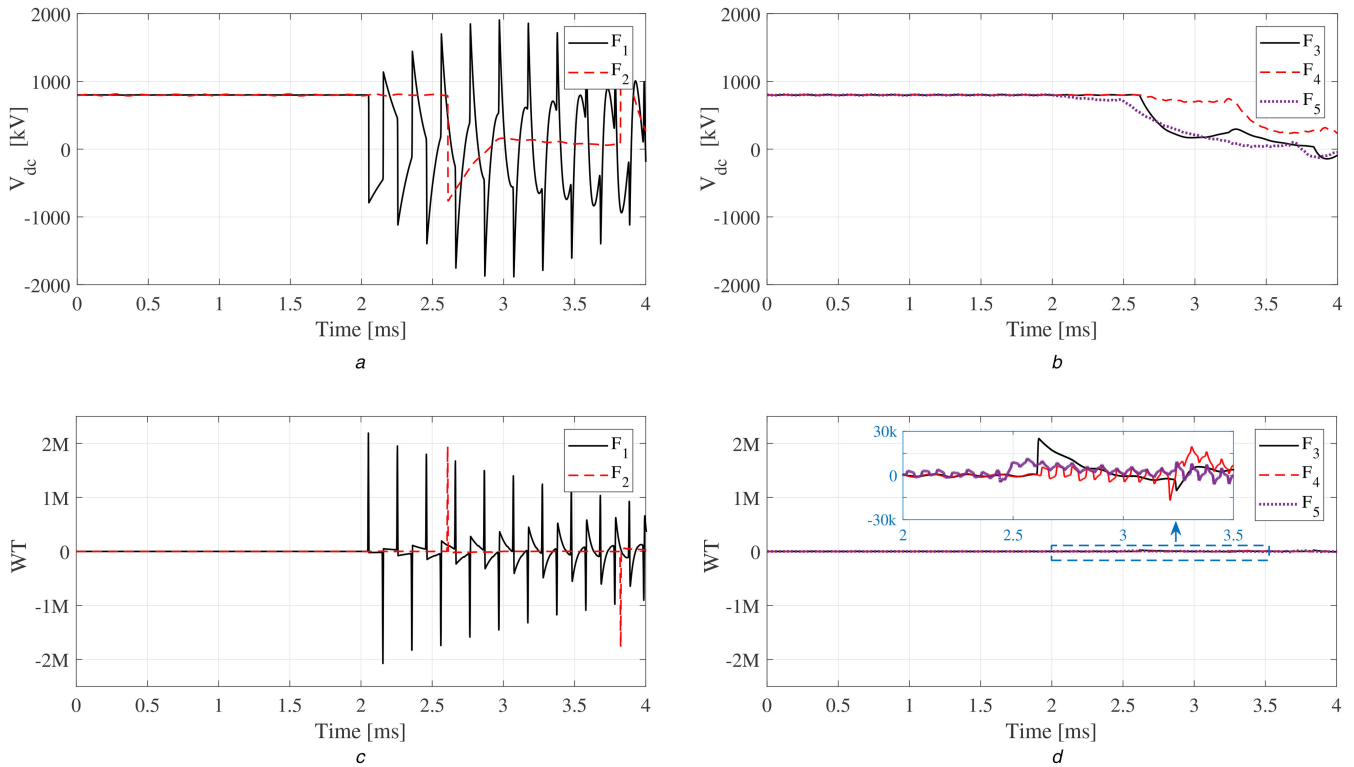
Figs. 6a and b illustrate the DC voltage signatures (captured at the line side of the inductor) for internal and external faults, respectively. The corresponding wavelet transform is depicted in Figs. 6c and d.

In the case of internal faults  $F_1$  and  $F_2$ , the resulting wavelet transforms reach high values up to  $2 \times 10^6$  (Fig. 6c). This is due to the fact that the measuring point is closer to the fault and does not have any lumped reactor in-between. As for external faults  $F_3$ ,  $F_4$  and  $F_5$ , the resulting magnitude of wavelet transforms are highly attenuated (Fig. 6d). This is expected since, for any external fault, the equivalent inductance included in the fault current path is always significantly larger than for the internal fault due to the installed lumped reactors (see Table 4).

The difference in magnitude of wavelet transform between and external faults provides a significant safety margin for fault discrimination and hence to the design of a reliable protection system. Such margin is much wider than the one presented in Fig. 5f where DC voltage magnitude was utilised. Moreover, simple under-voltage criteria can be jeopardised by other transients or excessive noise in voltage measurements. Consequently, as it has been demonstrated, the wavelet transform can be a very effective tool for designing MTDC protection schemes, especially when travelling wavefronts are attenuated by the terminating inductors.

## 4 Conclusions

This paper presented a detailed DC-side fault analysis considering inductive termination of lines within an MTDC grid. The analysis provided design guidelines for DC-side inductors, taking into account important aspects of protection such as the required fault detection time and the performance characteristics of the associated CBs. It has been demonstrated that the utilisation of inductive terminations in DC lines not only limits the rate-of-rise of current but also provides very useful voltage signatures which assist in reliable discrimination between internal and external faults. In particular, in the case of a multi-terminal network, such discrimination can be achieved by continuously monitoring the



**Fig. 6** Post fault DC voltage and the resulting WT

(a) DC voltage – internal faults  $F_1$  and  $F_2$ , (b) DC voltage – external faults  $F_3$ ,  $F_4$  and  $F_5$ , (c) WT – internal faults  $F_1$  and  $F_2$ , (d) WT – external faults  $F_3$ ,  $F_4$  and  $F_5$

status of DC voltage on the line side of the installed inductor. Moreover, it has been demonstrated that inductive termination of lines forms a significant boundary for voltage travelling waves. As such, by utilising a wavelet transform applied on the resulting post-fault voltage signatures, further and more reliable discrimination of faults can be achieved. Finally, it had been demonstrated that the point of measurement significantly affects the captured fault signatures. As a result, depending on the point of measurement, different fault-related functions (e.g. protection) can be designed accordingly. The work presented in this paper can act as a tool for inductor sizing but also for developing discriminative fault detection schemes based on travelling waves incorporating well-tuned wavelet transform.

## 5 Acknowledgments

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