

A NOVEL APPROACH FOR PROTECTION OF RADIAL AND MESHED MICROGRIDS

S. Mirsaedi*, X. Dong*, D. Tzelepis[†], and C. Booth[†]

*Department of Electrical Engineering, Tsinghua University, Beijing, People's Republic of China,
{m_sohrab, xzdong}@mail.tsinghua.edu.cn

[†]Department of Electronic and Electrical Engineering, University of Strathclyde, Glasgow, United Kingdom
{dimitrios.tzelepis, campbell.d.booth}@strath.ac.uk

Keywords: Micro-grid, grid-connected mode, islanded mode, protection scheme, positive-sequence component.

Abstract

During grid-connected operation mode of microgrids, since the main grid provides a large short-circuit current to the fault point, the protection can be performed by the conventional protective devices, but in islanded mode, fault currents are drastically lower than those of grid-connected mode. Hence, employment of traditional overcurrent-based protective devices in micro-grids is no longer valid and some alternative protection schemes should be developed. This paper presents a micro-grid protection scheme based on positive-sequence component using Phasor Measurement Units (PMUs) and a Central Protection Unit (CPU). The salient feature of the proposed scheme in comparison with the previous works is that it has the ability to protect both radial and meshed micro-grids against different types of faults. Furthermore, since the CPU is capable of updating its pickup values (upstream and downstream equivalent positive-sequence impedances of each line) after the first change in the micro-grid configuration (such as transferring from grid-connected to islanded mode and or disconnection of a line, bus, or DER either in grid-connected mode or in islanded mode), it can protect micro-grid against subsequent faults. In order to verify the effectiveness of the proposed scheme and the CPU, several simulations have been undertaken by using DIgSILENT PowerFactory and MATLAB software packages.

1 Introduction

The manifested merits of Distributed Energy Resources (DERs) in power systems have given rise to significant interests in microgrid development at regional levels. The generation of microgrid had a great influence on the protection of distribution network. The two-way flow characteristics makes it difficult to ensure the selectivity of the protection. The short circuit fault current is also drastically different between grid connected and islanded mode, which makes the conventional schemes unable to protect microgrids [1, 2]. The structure of a typical micro-grid is shown in Figure 1.

The research of microgrid protection has been a hot topic in recent years. In a study by Oudalov and Fidigatti [3], an

adaptive protection strategy was suggested, applying digital relaying and advanced communication technique. In the presented technique, the protection settings were updated periodically by means of Micro-Grid Central Controller (MGCC) in accordance with micro-grid operating modes. However, the proposed strategy necessitated updating or upgrading the protection devices which are presently applied in the distribution networks; moreover, fault calculations were relatively sophisticated for a micro-grid functioning in different modes. Dewadasa and his research group [4] proposed an additional methodology for inverter-based micro-grids using an admittance relay with inverse time tripping characteristics. Despite the fact that the methodology had the ability to protect micro-grids either in grid-connected or in stand-alone mode, it was unable to protect micro-grids including rotating-based DERs. The further shortcoming of the strategy was that it was designed for only radial micro-grids. Tumilty et al. and Redfern and H. Al-Nasseri [5] put forward a new protection approach based upon voltage measurements to protect autonomous micro-grids against different kinds of faults. Nevertheless, the suggested approach did not take account of grid-connected operating mode and High-Impedance Faults (HIFs). In a study by Sortomme et al. [2], a differential-based protection strategy was introduced which was able to protect micro-grids including radial or looped feeders in both modes of operation. However, the suggested strategy was only effective for the protection of lines and had not the ability to protect buses connected to DERs or loads. Nikkhajoei et al. [6] established an alternative protection method based upon symmetrical components. The authors applied zero- and negative- sequence currents to protect micro-grids against asymmetrical faults. However, the suggested technique was ineffective in detection of three-phase faults. Subsequently, in a research by Zamani et al. [7] another protection strategy was devised using zero- and negative-sequence components which had the ability to protect micro-grids against different kinds of faults; also, the proposed strategy did not require communication system. The main problem associated with the proposed method was that it was dependent on the micro-grid configuration, because the method had been designed for only radial micro-grids and was not capable of protecting micro-grids containing looped feeders; furthermore, due to the need for zero-sequence current in the proposed method, its implementation necessitated the application of a specific type of transformer (only grounded

transformers) inside the micro-grid. This paper presents a micro-grid protection scheme based on positive-sequence component using PMUs and a CPU. The proposed scheme has the ability to protect both radial and looped micro-grids against different types of faults. Furthermore, since the CPU is capable of updating its pickup values (upstream and downstream equivalent positive-sequence impedances of each line) after the first change in the micro-grid configuration, it can protect micro-grid against subsequent faults.

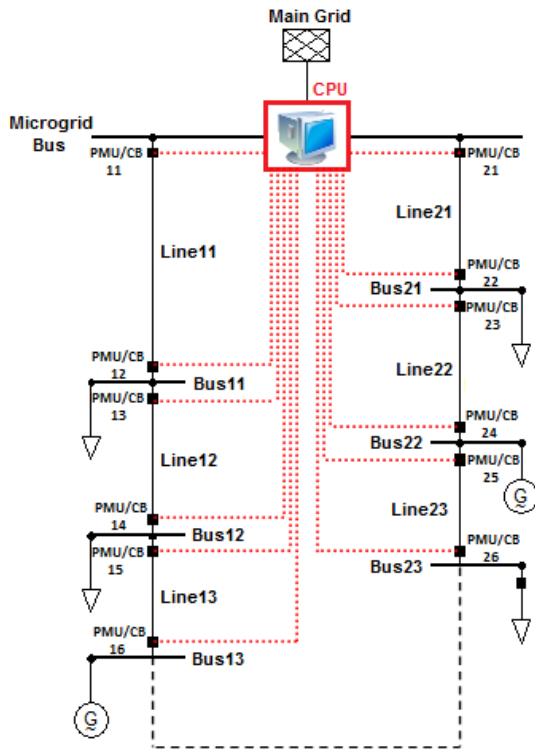


Figure 1: Structure of a typical micro-grid

2 The proposed protection scheme

This paper presents a protection scheme for micro-grids using PMUs and a CPU, thereby detecting different kinds of faults in both grid-connected and islanded modes of operation. In the proposed protection scheme, PMUs which are responsible for extracting voltage and current phasors (magnitudes and their respective phasor angles) based upon digital sampling of Alternating Current (AC) waveforms, are installed at both ends of each line of micro-grid. Subsequently, the information extracted by PMUs of each line is transferred to the CPU through a digital communication system. After a fault incident within the micro-grid, the information received by PMUs in the CPU is analyzed, and then the fault occurrence, location of fault, and faulted phases are recognized. Finally, depending on the fault type, proper tripping signals are issued to the relevant circuit breakers.

2.1 Detection of fault incident

In order to detect different types of faults, this paper presents a protection scheme based on symmetrical components

approach. The approach, developed by C. L. Fortescue, is one of the most effective ones, applied to transform a three-phase unbalanced system into three sets of symmetrical balanced phasors, namely positive-, negative- and zero- sequence components. In case a fault strikes within a network, these symmetrical components are formed depending on the fault type. However, the positive-sequence is the only component which exists in all types of faults. For this reason, in this study, the positive-sequence component is employed to detect different kinds of faults.

2.2 Detection of fault location

As mentioned earlier, the majority of the proposed methods to date are strongly dependent on the micro-grid configuration. In order to possess an appropriate method having the ability to protect different micro-grids with different configurations, micro-grid feeders should be sectionalized in such a way that each section (micro-grids line or bus) is protected independent of other sections. To fulfill this, the upstream and downstream of each line are replaced with its upstream and downstream equivalent circuits, respectively. Both of these equivalent circuits include a voltage source in series with impedance. Figure 2 indicates the upstream and downstream equivalent circuits of Line12 of Figure 1 during a fault.

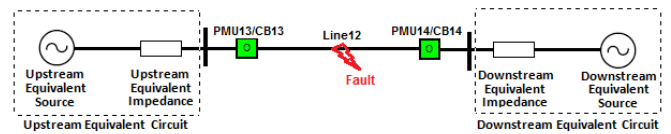


Figure 2: Upstream and downstream equivalent circuits of Line12 of Figure 1 during a fault

During a fault occurrence in Line 12 of Figure 1, different symmetrical components are created depending on the fault type. By replacing the equivalent impedance of negative- and zero- sequence networks between terminals AB of positive-sequence network for all types of faults, a general model for the analysis of different kinds of faults can be developed. The developed model is demonstrated in Figure 3, in which impedance $Z_{eq2,0}$ is the representative of negative- and zero-sequence networks.

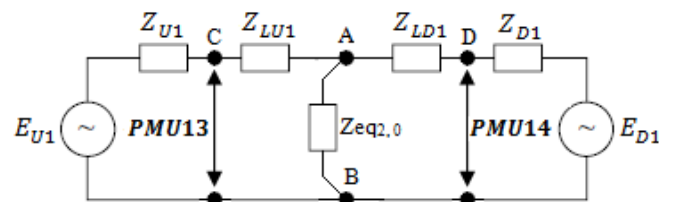


Figure 3: Developed general model for the analysis of different kinds of faults

Depending on the fault type, the value of this impedance is different. Equation (1) expresses the value of impedance $Z_{eq2,0}$ for different types of faults:

$$Z_{eq2,0} = \begin{cases} Z_{eq0} + Z_{eq2} & \text{for single line to ground faults} \\ Z_{eq2} & \text{for line to line faults} \\ Z_{eq0} \parallel Z_{eq2} & \text{for line to line to ground faults} \\ 0 & \text{for three phase faults} \end{cases} \quad (1)$$

where,

$$Z_{eq0} = (Z_{U0} + Z_{LU0}) \parallel (Z_{D0} + Z_{LD0})$$

$$Z_{eq2} = (Z_{U2} + Z_{LU2}) \parallel (Z_{D2} + Z_{LD2})$$

In the proposed protection scheme, after the detection of fault incident, the faulted section is recognized by the developed model of Figure 3 in such a way as to compare the value of upstream and downstream equivalent positive-sequence impedances, before and after the fault. In fact, when a fault occurs inside a line, impedance $Z_{eq2,0}$ is created between points C and D. Therefore, the values of both upstream and downstream equivalent positive-sequence impedances after the fault (Z_{U1}, Z_{D1}) remain equal to the values of those impedances before the fault ($Z_{U1(pre)}, Z_{D1(pre)}$), but in case a fault occurs at the upstream or downstream of a line, respectively, only the value of Z_{D1} or only the value of Z_{U1} remains constant after the fault.

3 Structure of the Central Protection Unit (CPU)

In order to implement the proposed protection scheme, a digital CPU has been designed. The schematic diagram of the CPU for the micro-grid shown in Figure 1 is demonstrated in Figure 4. As can be seen in the figure, for the protection of each line and its adjacent buses, a specific Protection Module (PM) is dedicated. Each PM receives the voltage and current phasors from the installed PMUs at both ends of the respective line. If the fault occurs inside that line or its adjacent buses, the proper tripping signal commands are sent to the respective circuit breakers, and then the faulted section is isolated from the rest of the micro-grid. Each PM consists of two main parts, namely, fault incident detector and fault locator, which are described in detail in the following subsections:

3.1 Fault incident detector

As explained earlier, the positive-sequence component is the only component which exists in all types of faults. Therefore, in the proposed protection scheme, the component is used to detect different kinds of faults. When a fault occurs in a micro-grid section (line or bus), the positive-sequence current magnitude of that section is drastically increased; hence, the fault occurrence can be detected by comparing the magnitude before and after the fault. In the CPU, this function is performed by fault incident detector. It should be noted that the settings of the fault incident detector should be such a way as to avoid the mal-operation of the PMs in case of a small change in the positive-sequence current magnitude. Moreover, since a fault in one section may increase the positive-sequence current magnitude of other sections, PMs related to non-faulted lines in the CPU may issue fault trip signals mistakenly. Hence, the

deployment of an additional detector (Fault locator) is necessary.

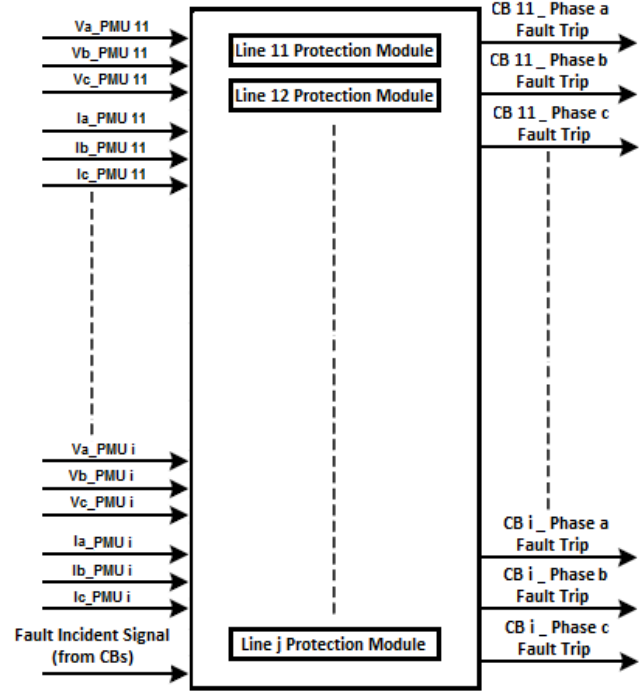


Figure 4: Schematic diagram of the CPU for the micro-grid shown in Figure 1

3.2 Fault locator

As mentioned in Subsection 2.2, the faulted section is identified based on changes in the values of upstream and downstream equivalent positive-sequence impedances before and after the fault. In the CPU, this function is performed by fault locator. Prior to fault incident, the fault locator respective to each line, first, calculates the values of Thevenin's Equivalent Positive-Sequence Impedances (TEPSIs) at both ends of that line, and then it deploys the values to determine the values of impedances $Z_{U1(pre)}$ and $Z_{D1(pre)}$. Finally, the faulted section can be recognized by comparing the values of upstream and downstream equivalent positive-sequence impedances before ($Z_{U1(pre)}, Z_{D1(pre)}$) and after (Z_{U1}, Z_{D1}) the fault.

In order to determine the TEPSI of each point within the micro-grid, this paper introduces an online methodology by using three consecutive voltage and current measurements of PMUs at different time instants. Since any changes in the frequency of the micro-grid system will lead to slip between micro-grid frequency system and the PMU sampling frequency, phase angles of voltage and current for these three measurements will be different. Figure 5 illustrates the equivalent circuit diagram of the positive-sequence network for Line 12 (of Figure 1) prior to fault occurrence.

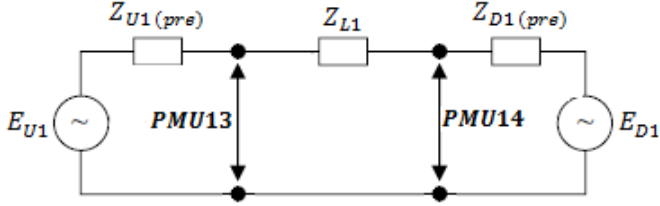


Figure 5: Equivalent circuit diagram of the positive- sequence network for Line 12 (of Figure 1) prior to fault occurrence

Based on Thevenin's model, the node positive-sequence voltage equation is defined as:

$$V_1 = E_{t1} - Z_{t1} \cdot I_1 \quad (2)$$

According to Equation (2), the positive-sequence voltage equation for PMU13 terminals becomes:

$$V_{1PMU13} = E_{t1PMU13} - Z_{t1PMU13} \cdot I_{1PMU13} \quad (3)$$

Where,

$E_{t1PMU13}$ =Thevenin's equivalent positive-sequence voltage source at PMU13 terminals

$Z_{t1PMU13}$ =Thevenin's equivalent positive-sequence impedance at PMU13 terminals

Positive-sequence phasor diagrams of Equation (3) for two different measurements at PMU13 terminals are indicated in Figure 6. Since $E_{t1PMU13}$ is the Thevenin's positive-sequence equivalent voltage source, its magnitude for both measurements are identical, but its angle in the IInd measurement is shifted by an angle equal to the phase drift. Referring to Figure 6, $E_{t1PMU13}$ equation for the Ist measurement can be written as:

$$E_{t1PMU13}^2 = V_{1PMU13I}^2 + I_{1PMU13I}^2 \cdot Z_{t1PMU13}^2 + 2V_{1PMU13I} \cdot I_{1PMU13I} \cdot Z_{t1PMU13} \cdot \cos(\theta + \phi_I) \quad (4)$$

By expanding $\cos(\theta + \phi_I)$, Equation (4) can be expressed as follows:

$$E_{t1PMU13}^2 = V_{1PMU13I}^2 + I_{1PMU13I}^2 \cdot Z_{t1PMU13}^2 + 2P_{1PMU13I} \cdot R_{t1PMU13} - 2Q_{1PMU13I} \cdot X_{t1PMU13} \quad (5)$$

Where $R_{t1PMU13}$ and $X_{t1PMU13}$ denote the resistance and reactance of the Thevenin's equivalent positive-sequence impedance, as well as $P_{1PMU13I}$ and $Q_{1PMU13I}$, which respectively represent active and reactive powers flowing through Line 12. Likewise, the $E_{t1PMU13}$ equation for the IInd measurement can be written as:

$$E_{t1PMU13}^2 = V_{1PMU13II}^2 + I_{1PMU13II}^2 \cdot Z_{t1PMU13}^2 + 2P_{1PMU13II} \cdot R_{t1PMU13} - 2Q_{1PMU13II} \cdot X_{t1PMU13} \quad (6)$$

By subtracting Equation (6) from Equation (5):

$$V_{1PMU13I}^2 - V_{1PMU13II}^2 + (I_{1PMU13I}^2 - I_{1PMU13II}^2) \cdot Z_{t1PMU13}^2 + 2(P_{1PMU13I} - P_{1PMU13II}) \cdot R_{t1PMU13} - 2(Q_{1PMU13I} - Q_{1PMU13II}) \cdot X_{t1PMU13} = 0 \quad (7)$$

Equation (7) can be arranged as follows:

$$\left(R_{t1PMU13} + \frac{P_{1PMU13I} - P_{1PMU13II}}{I_{1PMU13I}^2 - I_{1PMU13II}^2} \right)^2 + \left(X_{t1PMU13} - \frac{Q_{1PMU13I} - Q_{1PMU13II}}{I_{1PMU13I}^2 - I_{1PMU13II}^2} \right)^2 = \frac{V_{1PMU13II}^2 - V_{1PMU13I}^2}{I_{1PMU13I}^2 - I_{1PMU13II}^2} + \left(\frac{P_{1PMU13I} - P_{1PMU13II}}{I_{1PMU13I}^2 - I_{1PMU13II}^2} \right)^2 + \left(\frac{Q_{1PMU13I} - Q_{1PMU13II}}{I_{1PMU13I}^2 - I_{1PMU13II}^2} \right)^2 \quad (8)$$

This is the equation of a circle in the positive-sequence impedance plane which indicates a locus for the Thevenin's equivalent positive-sequence impedance seen from PMU13 terminals. As it does not specify a certain value for $Z_{t1PMU13}$, a third measurement is required so that it is used with the first and second measurements to create two other circles for $Z_{t1PMU13}$. According to Thevenin's theorem, Thevenin's equivalent impedance for any two-terminal of the network is the impedance seen from those terminals when the sources are set to zero. Hence, $Z_{t1PMU13}$ for PMU13 terminals of Figure 5 is equivalent to $Z_{U1} \parallel (Z_{L1} + Z_{D1})$. By setting this equal to the calculated $Z_{t1PMU13}$ from the intersection point of the three circles:

$$Z_{t1PMU13cal.} = Z_{U1(pre)} \parallel (Z_{L1} + Z_{D1(pre)}) \quad (9)$$

By following the same procedure for PMU14 terminals of Figure 5:

$$Z_{t1PMU14cal.} = Z_{D1(pre)} \parallel (Z_{L1} + Z_{U1(pre)}) \quad (10)$$

By solving Equations (9) and (10), the values of $Z_{U1(pre)}$ and $Z_{D1(pre)}$ are obtained. Subsequently, the fault locator respective to each line compares the values of $Z_{U1(pre)}$ and $Z_{D1(pre)}$ with the values of Z_{U1} and Z_{D1} after the fault incident and identifies the faulted section.

4 Simulation results

The single-line diagram of the test micro-grid is illustrated in Figure 7. As can be seen in the figure, it is connected to the main grid by means of a 69 kV/24.9 kV Dyn transformer. It also includes two photovoltaic parks (640 kW) and one wind farm (504 kW) which are interfaced with the network through respective YNyn transformers.

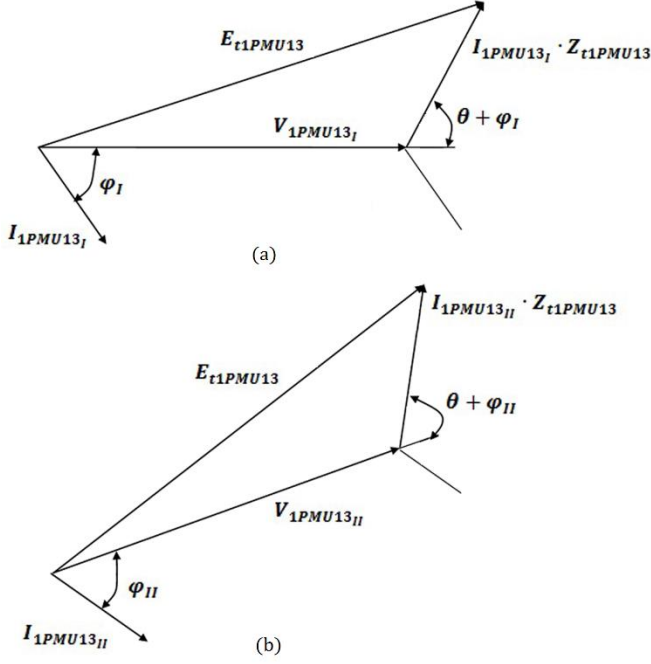


Figure 6: Positive- sequence phasor diagrams for two different measurements at PMU13 terminals: (a) Ist measurement (b) IInd measurement

To prove the efficacy of the CPU in the grid-connected and islanded operating modes, the performance of several PMs was simulated using DIgSILENT PowerFactory and MATLAB software packages, but due to space restriction and format requirements of this publication, only the simulation results of Line 203 Protection Module is included in this paper. According to the simulation results, the calculated values of upstream and downstream equivalent positive-sequence impedances (from the intersection of circles) for Line 203 before the fault incidents in both grid-connected and islanded operating modes are as follows:

$$Z_{U1L203(pre)cal.} : \begin{cases} 8.7499 (\Omega) & \text{for grid - connected mode} \\ 47.1347 (\Omega) & \text{for islanded mode} \end{cases}$$

$$Z_{D1L203(pre)cal.} : \begin{cases} 8.5499 (\Omega) & \text{for grid - connected mode} \\ 77.0590 (\Omega) & \text{for islanded mode} \end{cases}$$

where,

$Z_{U1L203(pre)cal.}$ = Upstream equivalent positive-sequence impedance of PMU203 (U)

$Z_{D1L203(pre)cal.}$ = Downstream equivalent positive-sequence impedance of PMU203 (D)

Tables 1 and 2 indicate the simulation results of Line203 Protection Module during different kinds of faults at the midpoint of Lines 203 and 302 (F1 and F2 in Figure 7) in both grid-connected and islanded operating modes, respectively.

As can be seen from the tables, the positive- sequence current magnitudes during different types of faults in islanded mode are drastically lower than those of grid-connected mode. It is due to the fact that the Thevenin's impedance viewed from the fault points (F1 and F2) in islanded operating mode is much

higher than that in the grid-connected mode; therefore, traditional over-current strategies with a single setting group will not be able to provide a selective trip for all types of faults in both grid-connected and islanded modes of operation. Once fault F1 or F2 occurred either in grid-connected or islanded mode, Line 203 Protection Module calculates the values of Z_{U1L203} and Z_{D1L203} and then compares them, respectively, with the values of $Z_{U1L203(pre)cal.}$ and $Z_{D1L203(pre)cal.}$. According to Tables 1 and 2, since Fault F1 has occurred inside of Line 203, the values of Z_{U1L203} and Z_{D1L203} are respectively equal to the values of $Z_{U1L203(pre)cal.}$ and $Z_{D1L203(pre)cal.}$, whereas fault F2 has occurred at the downstream of Line 203 and therefore, only the value of Z_{U1L203} is equal to the value of $Z_{U1L203(pre)cal.}$

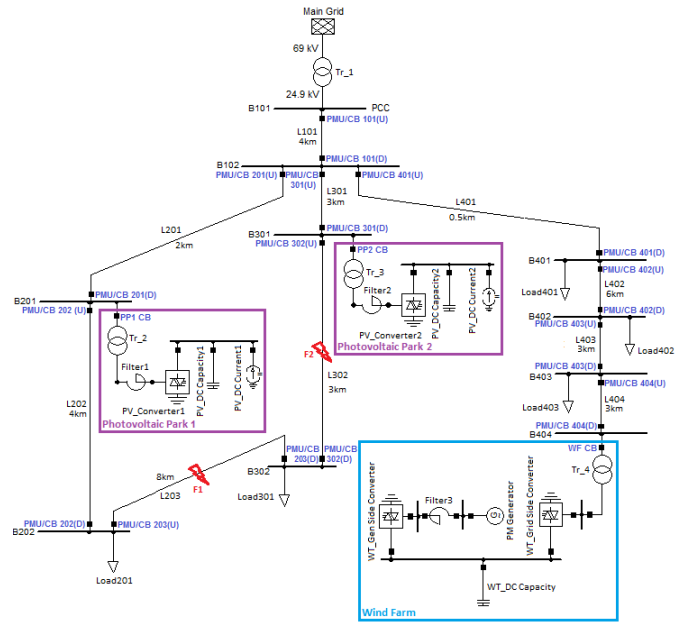


Figure 7: Single-line diagram of the test micro-grid

5 Conclusion

This paper proposed a protection scheme based on positive-sequence component for micro-grids. In spite of the majority of the developed protection strategies to date which are strongly dependent on the network architecture, the suggested scheme is capable of protecting different micro-grids with different configurations. In fact, the proposed scheme has the ability to protect either radial or meshed micro-grids against different types of faults. Moreover, Since the designed CPU is capable of updating their pickup values after the first change in the micro-grid configuration, it can protect micro-grid lines and buses against subsequent faults.

Acknowledgements

This work is funded in part by the National Natural Science Foundation of China (Grant No. 51120175001), and in part by the National Key Research and Development Plan of China (Grant No. 2016YFB0900600).

Fault Type		AG		BC		BCG		ABC	
Fault Location		F1	F2	F1	F2	F1	F2	F1	F2
PMU203 (U)	$ \bar{V}_{1PMU203(U)} $ (kV)								
	$ \bar{E}_{U1} - \bar{V}_{1PMU203(U)} $ (kV)	11.5966	11.9350	9.6348	10.3793	8.4334	9.3542	5.5298	7.0634
	$ \bar{I}_{1PMU203(U)} $ (A)	2.7971	2.4659	4.7554	4.0319	5.9731	5.0408	8.8869	7.3347
	$ \bar{I}_{APMU203(U)} $ (A)	319.6722	281.8203	543.4804	460.7938	682.6478	576.0980	1015.6570	838.2610
	$ \bar{I}_{BPMU203(U)} $ (A)	930.9764	782.8649	3.1912	3.18577	3.1100	3.1634	1023.2251	840.8320
	$ \bar{I}_{CPMU203(U)} $ (A)	3.2012	3.2266	940.2354	794.6089	1001.0088	821.6507	1032.0562	847.7558
PMU203 (D)	$ \bar{V}_{1PMU203(D)} $ (kV)								
	$ \bar{E}_{D1} - \bar{V}_{1PMU203(D)} $ (kV)	3.2109	3.2204	940.8970	796.4964	1002.0910	826.4506	1014.3305	836.2392
	$ \bar{I}_{1PMU203(D)} $ (A)	11.6082	10.7275	9.6623	8.0940	8.4671	6.4597	5.5934	2.4528
	$ \bar{I}_{APMU203(D)} $ (A)	2.7872	3.6819	4.7308	6.3265	5.9364	8.0298	8.8155	11.9826
	$ \bar{I}_{BPMU203(D)} $ (A)	325.9221	489.6217	553.3164	863.8151	694.3239	1118.3574	1031.0646	1756.9881
	$ \bar{I}_{CPMU203(D)} $ (A)	930.5706	1410.6070	3.1866	3.1499	3.1760	3.0042	1032.2881	1750.8619
$Z_{U1L203} = \frac{ \bar{E}_{U1} - \bar{V}_{1PMU203(U)} }{ \bar{I}_{1PMU203(U)} }$ (Ω)		$\cong 8.7499$	$\cong 8.7499$	$\cong 8.7499$	$\cong 8.7499$	$\cong 8.7499$	$\cong 8.7499$	$\cong 8.7499$	$\cong 8.7499$
$Z_{D1L203} = \frac{ \bar{E}_{D1} - \bar{V}_{1PMU203(D)} }{ \bar{I}_{1PMU203(D)} }$ (Ω)		$\cong 8.5499$	$\neq 8.5499$	$\cong 8.5499$	$\neq 8.5499$	$\cong 8.5499$	$\neq 8.5499$	$\cong 8.5499$	$\neq 8.5499$
Operated CBs in Line 203	Phase A								
	Phase B	Yes	No	No	No	No	No	Yes	No
	Phase C	No	No	Yes	No	Yes	No	Yes	No

Table 1: The simulation results of Line 203 Protection Module during the grid-connected mode

Fault Type		AG		BC		BCG		ABC	
Fault Location		F1	F2	F1	F2	F1	F2	F1	F2
PMU203 (U)	$ \bar{V}_{1PMU203(U)} $ (kV)								
	$ \bar{E}_{U1} - \bar{V}_{1PMU203(U)} $ (kV)	11.0988	11.3099	9.1148	9.7430	7.7168	8.4308	4.7300	5.9963
	$ \bar{I}_{1PMU203(U)} $ (A)	3.2179	2.9887	5.1640	4.5415	6.5494	5.8419	9.5093	8.2544
	$ \bar{I}_{APMU203(U)} $ (A)	68.2702	63.4076	109.5583	96.3515	138.9507	123.9405	201.7473	175.1235
	$ \bar{I}_{BPMU203(U)} $ (A)	175.7082	159.1533	3.3477	3.3381	3.2157	3.2750	201.6867	175.1680
	$ \bar{I}_{CPMU203(U)} $ (A)	3.4469	3.4506	183.5472	166.1232	190.4675	172.8879	203.8263	175.1037
PMU203 (D)	$ \bar{V}_{1PMU203(D)} $ (kV)								
	$ \bar{E}_{D1} - \bar{V}_{1PMU203(D)} $ (kV)	3.5419	3.4532	183.7441	166.7269	192.0183	172.7766	199.8883	175.2337
	$ \bar{I}_{1PMU203(D)} $ (A)	11.1005	10.1237	9.1258	7.9855	7.7301	6.0760	4.7564	2.3284
	$ \bar{I}_{APMU203(D)} $ (A)	3.2345	4.2114	5.2147	6.3656	6.6143	8.2511	9.5962	12.0032
	$ \bar{I}_{BPMU203(D)} $ (A)	41.9743	60.1499	67.6715	92.8073	85.8342	123.2330	124.5305	183.1621
	$ \bar{I}_{CPMU203(D)} $ (A)	111.1246	152.4975	3.4451	3.5545	3.1905	3.1798	124.4060	183.7132
$Z_{U1L203} = \frac{ \bar{E}_{U1} - \bar{V}_{1PMU203(U)} }{ \bar{I}_{1PMU203(U)} }$ (Ω)		$\cong 47.1347$	$\cong 47.1347$	$\cong 47.1347$	$\cong 47.1347$	$\cong 47.1347$	$\cong 47.1347$	$\cong 47.1347$	$\cong 47.1347$
$Z_{D1L203} = \frac{ \bar{E}_{D1} - \bar{V}_{1PMU203(D)} }{ \bar{I}_{1PMU203(D)} }$ (Ω)		$\cong 77.0590$	$\neq 77.0590$	$\cong 77.0590$	$\neq 77.0590$	$\cong 77.0590$	$\neq 77.0590$	$\cong 77.0590$	$\neq 77.0590$
Operated CBs in Line 203	Phase A								
	Phase B	Yes	No	No	No	No	No	Yes	No
	Phase C	No	No	Yes	No	Yes	No	Yes	No

Table 2: The simulation results of Line 203 Protection Module during the islanded mode

References

- [1] A. Hooshyar and R. Iravani, "Microgrid Protection," *Proc. of the IEEE*, vol. 105, no. 7, pp. 1332-1353, (2017).
- [2] E. Sortomme, S. S. Venkata and J. Mitra, "Microgrid Protection Using Communication-Assisted Digital Relays," in *IEEE Transactions on Power Delivery*, vol. 25, no. 4, pp. 2789-2796, (2010).
- [3] A. Oudalov and A. Fidigatti, "Adaptive network protection in microgrids," *International Journal of Distributed Energy Resources*, 5, pp. 201-225, (2009).
- [4] M. Dewadasa, R. Majumder, A. Ghosh and G. Ledwich, "Control and protection of a microgrid with converter interfaced micro sources," *International Conference on Power Systems*, Kharagpur, pp. 1-6, (2009).
- [5] H. Al-Nasseri and M. A. Redfern, "Harmonics content based protection scheme for Micro-grids dominated by solid state converters," *12th International Middle-East Power System Conference*, Aswan, pp. 50-56, (2008).
- [6] H. Nikkhajoei and R. H. Lasseter, "Microgrid Protection," *2007 IEEE Power Engineering Society General Meeting*, Tampa, FL, pp. 1-6, (2007).
- [7] M. A. Zamani, T. S. Sidhu and A. Yazdani, "A Protection Strategy and Microprocessor-Based Relay for Low-Voltage Microgrids," in *IEEE Transactions on Power Delivery*, vol. 26, no. 3, pp. 1873-1883, (2011).