Lyapunov-Based High Performance Controller for Modular Resonant DC/DC Converters for Medium Voltage DC Grids

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Abstract: This paper presents a high performance controller based on Lyapunov stability criterion that enhances dynamic performance and disturbance rejection capability of resonant DC/DC converters when compared with classical PI control. The series-parallel resonant converter (SPRC) is used as the candidate converter to which this controller design is applied but the design can be generalized to other types of resonant DC/DC converters. By using a multiple module approach, low power modules of this resonant converter are stacked to enable operation at medium voltage DC. The proposed controller design is applied to modular structure of the SPRC to verify its high performance output in conjunction with active sharing control loops that ensure uniform current/voltage distribution across the multiple interconnected modules. Detailed controller design, closed loop stability criteria, robustness and parameter sensitivity are investigated and controller performance is compared and verified against classical PI control in simulation and low-scaled experimental prototype. Operations in single-module and two-module input-series output-parallel modes are both studied. The paper affirms the selection of the modular DC/DC converter architecture and its associated proposed controls for high performance medium voltage DC applications.

1. Introduction

Demand for medium voltage DC (MVDC) transmission is becoming higher due to emergence of microgrids and integration requirements of renewable energy sources, medium voltage drives and new transportation systems in smart cities. Offshore wind farms and photovoltaic parks utilize MVDC in collection grids as an intermediate stage to HVDC transmission [1,2]. Where transmitted power is not significantly high, medium voltage becomes an economical solution for transmission to shore [3]. More recently, electrification of offshore oil and gas platforms is also dictating the use of MVDC for subsea power distribution networks and to power subsea nodes from shore [4,5]. MVDC is yet acting as a cornerstone for emerging smart transportation systems including electric vehicles, all-electric trains, ships and planes [6-9]. Industrially, initial designs for the UK's first MVDC link in North Wales have been recently revealed [10]. The ANGLE DC project will connect the island of Anglesey at the Llanfair PG sub-station to the North Wales mainland at Bangor operating at ±27 kV DC with 30.5 MW rating.

A key element in MVDC systems is the DC/DC converter which acts as a transformer in AC systems [11-13]. Two-stage DC/DC converters are commonly applicable in medium and high voltage applications due to the favourable characteristics they offer such as galvanic isolation, better switch utilization and high

conversion efficiency [14,15]. This paper focuses on one of the popular topologies of two-stage DC/DC resonant converters; viz the series-parallel resonant converter (SPRC) [16]. The converter allows soft switching and offers high efficiency for a wide load range. It is seen as a promising technology in medium voltage applications if appropriately scaled up by stacking multiple low-power low-voltage modules. In addition to higher overall power and voltage operation, the modular approach allows for redundancy implementation hence improved fault tolerance, expandability and ease of maintenance [17]. Also, since individual converter modules handle lower power, component stresses are reduced and thermal design is easier [18]. In this paper, the input-series output-parallel (ISOP) connection [19-21] of SPRC will be considered for its potential use in step down DC/DC conversion with high input-voltage high output-current characteristics.

A high performance controller based on Lyapunov stability criterion is proposed for SPRC to enhance its dynamic performance and disturbance rejection capability compared to PI control. Controller design is model based and is, therefore, generically applicable to other types of resonant converters which can be derived from the general SPRC version of resonant converters. This proposed Lyapunov-based controller is then applied in the modular ISOP connected converter for output voltage regulation. Additional controls to ensure uniform sharing of voltages and currents among the interconnected modules are also applied. This proposed Lyapunov-based controller design with its associated active sharing loops provides a promising modular DC/DC converter architecture for MVDC grids.

The remaining sections of the paper will be organized as follows. Sections two to six will detail the SPRC converter modelling and proposed Lyapunov controller design, stability, robustness and parameter sensitivity issues for a single-module SPRC converter. These will include simulation and low-scaled experimental prototype results comparing proposed controller performance against PI control. Section seven will detail the modular ISOP connected operation of SPRC with the proposed controller and active sharing loops. Simulation and experimental results are also provided for a two-module system operation.

2. SPRC modelling

Fig. 1 shows the circuit diagram for a typical SPRC. It consists of a tank of passive elements; namely an inductor (L_s) and two capacitors one in series (C_s) and one in parallel (C_p). The tank is fed by a voltage source inverter which could be half-bridge or full-bridge and controlled using the inverter's frequency, duty ratio or both to achieve voltage control across the parallel capacitor C_p. To achieve DC output, the voltage across the capacitor is rectified and the higher harmonic AC components are filtered out using an LC filter. Power is transferred to load through fundamental AC frequency and according to the relation of

this fundamental frequency to tank resonance frequency- at different load (quality) factors- the converter can achieve different voltage gains.

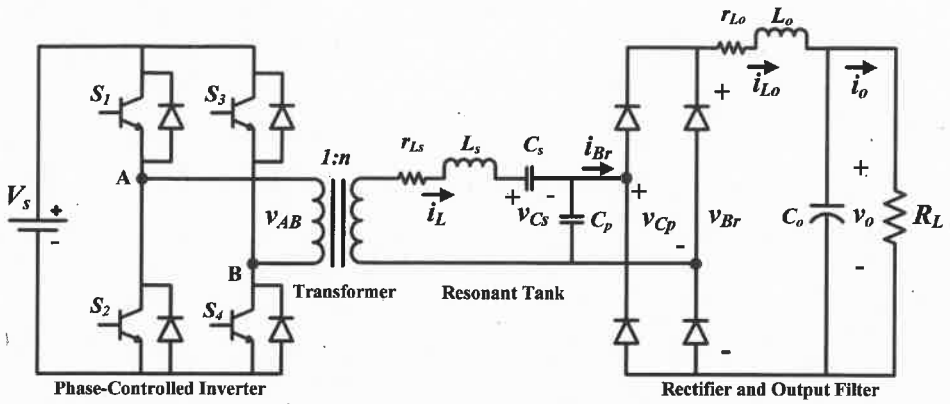

Fig. 1. *Circuit diagram for the SPRC.*

A unified model merging the AC and DC state variables of the resonant tank and the output filter respectively, into one large signal model has been detailed by the authors in [22]. In this model, the AC link state variables were transformed to equivalent DC quantities using the fundamental frequency approximation of the harmonic balance theory [23] which converts the AC state variables to d-q quantities. The resulting DC state variables from the resonant tank are combined with the natural DC state variables of the output filter side (with average state-space modelling) using a linearization scheme to overcome the diode rectifier non-linearity. The result is an aggregate large signal linear model for the SPRC,

$$\begin{aligned} \dot{\vec{x}}(t) &= A\vec{x}(t) + B\vec{u}(t) \\ y(t) &= C\vec{x}(t) \end{aligned} \tag{1}$$

$$\vec{x}(t) = [i_{Ld}\ i_{Lq}\ v_{Csd}\ v_{Csq}\ v_{Cpd}\ v_{Cpq}\ i_{Lo}\ v_o]^T \qquad \vec{u}(t) = [v_c\ i_o]^T \qquad y(t) = v_o$$

$$A = \begin{bmatrix} -\frac{r_T}{L_T} & \omega_s & -\frac{1}{L_T} & 0 & -\frac{1}{L_T} & 0 & \frac{4k_3}{\pi L_T} & 0 \\ -\omega_s & -\frac{r_T}{L_T} & 0 & -\frac{1}{L_T} & 0 & -\frac{1}{L_T} & \frac{4k_7}{\pi L_T} & 0 \\ \frac{1}{C_s} & 0 & 0 & \omega_s & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_s} & -\omega_s & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_p} & 0 & 0 & 0 & 0 & \omega_s & -\frac{4}{\pi C_p} & 0 \\ 0 & \frac{1}{C_p} & 0 & 0 & -\omega_s & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{2}{\pi L_o} & 0 & -\frac{r_{Lo}}{L_o} & -\frac{1}{L_o} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_o} & 0 \end{bmatrix} \quad B = \begin{bmatrix} \frac{k_1}{L_T} & 0 \\ \frac{k_5}{L_T} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & -\frac{1}{C_o} \end{bmatrix} \quad C = [0\ \ 0\ \ 0\ \ 0\ \ 0\ \ 0\ \ 0\ \ 1]$$

where the parameters used in the model are circuit parameters in Fig. 1 in addition to other derived parameters defined in [22]. The control v_c is used to regulate converter output voltage.

Using the derived model, control-to-output voltage transfer function can be approximated by the second order output filter dynamics thanks to its slower dynamics (compared to the resonant tank) which therefore dominates converter output voltage response.

$$\frac{v_o(s)}{v_c(s)} \approx \frac{2}{\pi}\frac{v_o(s)}{\bar{v}_{Br}(s)} \approx \frac{2}{\pi}\frac{1}{L_oC_os^2 + r_{Lo}C_os + 1} \tag{2}$$

Since the main objective of the SPRC is output voltage control; therefore, the control-to-output voltage transfer function (2) is necessary and appropriate for control design. Fig. 2(a) shows the full structure of the closed loop output voltage control [22]. The control is implemented in such a way to enable peak resonant tank capacitor voltage ($v_{Cp(peak)}$) to track and follow control v_c. This facilitates approximation of the control diagram to the simplified version in Fig. 2(b) as the diode rectifier output average voltage $\bar{v}_{Br}$ is directly achieved from peak resonant tank capacitor voltage by the ($2/\pi$) averaging factor. The controller derived in [22] for the output voltage control of SPRC was simple PI control. However, the objective of this paper is to design a more robust Lyapunov-based controller with the view of enhancing closed loop stability and dynamic performance.

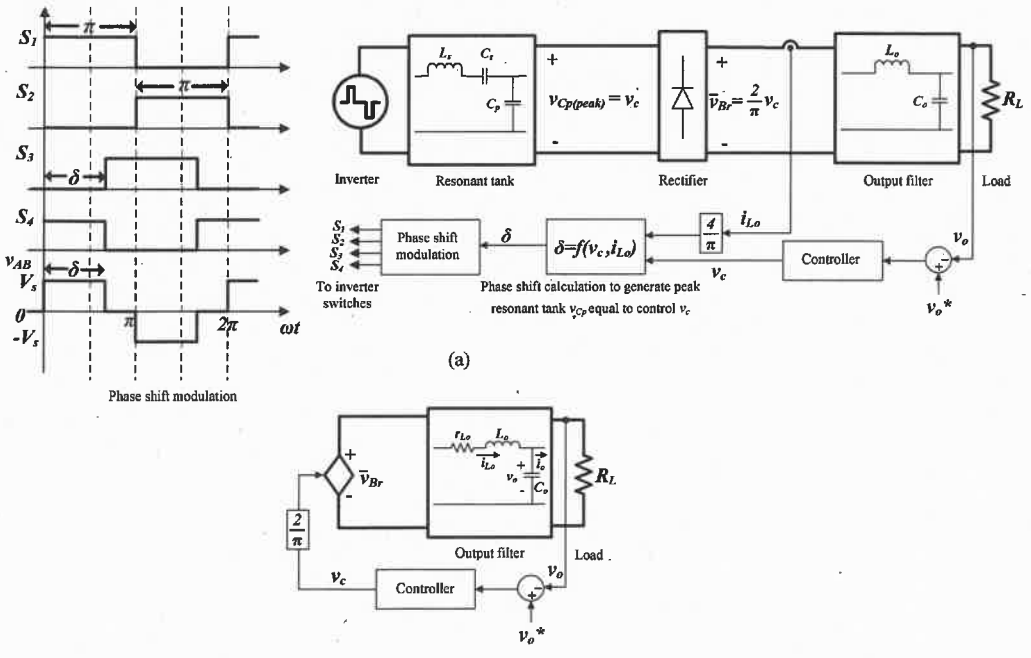

Fig.2: *Closed loop output voltage control of SPRC*

(a) Full structure

(b) Reduced equivalent model.

From Fig. 2(b) the output filter equations can be written as

$$\frac{di_{Lo}}{dt} = \frac{1}{L_o}\left(-r_{Lo}i_{Lo} - v_o + \frac{2}{\pi}v_c\right)$$
$$\frac{dv_o}{dt} = \frac{1}{C_o}(i_{Lo} - i_o) = \frac{1}{C_o}\left(i_{Lo} - \frac{1}{R_L}v_o\right) \quad (3)$$

3. Construction of proposed Lyapunov control law

Lyapunov controller uses Lyapunov's stability theory to find if there exists a control $u(x,t)$ such that the system can be made asymptotically stable, that is, a system starting in a state $x \neq 0$ in some domain D will eventually return to $x=0$. A control Lyapunov function $V(x,u)$ is a function that [24]

- is positive definite, i.e. $V(x,u) > 0 \quad \forall x \neq 0$
- its derivative is negative definite, i.e. $\dot{V}(x,u) < 0 \quad \forall x \neq 0$
- is proper, i.e. $V(x) \to \infty \quad |x| \to \infty$

The second condition is the key condition; which if satisfied means that for each state x, a control input u exists that will reduce V. For the SPRC described by (3), define an error signal e for output voltage control such that

$$e = v_o^* - v_o \quad (4)$$

where v_o^* is the reference output voltage. A positive definite first order control Lyapunov function $V(x)$ is defined as

$$V = \frac{1}{2}(\dot{e} + \alpha e)^2 \quad (5)$$

where α is a proportionality constant. According to Lyapunov's second condition, the derivative of V has to be negative definite to enable stable operation

$$\dot{V} = (\dot{e} + \alpha e)(\ddot{e} + \alpha \dot{e}) < 0 \quad (6)$$

Since V is positive definite, to achieve the second condition (6), the required negative derivative of V is assumed such that

$$\dot{V} = -\beta V \quad (7)$$

where β is strictly a positive proportionality constant. Substituting (5) and (7) into (6) yields

$$(\ddot{e}+\alpha\dot{e})=-\frac{\beta}{2}(\dot{e}+\alpha e) \tag{8}$$

Assuming v_o^* to be constant, then

$$\begin{aligned}\dot{e}&=-\dot{v}_O\\ \ddot{e}&=-\ddot{v}_O\end{aligned} \tag{9}$$

Substituting (9) into (8) yields

$$\ddot{v}_O+\alpha\dot{v}_O=\frac{\beta}{2}\left(\alpha v_o^*-\alpha v_O-\dot{v}_O\right) \tag{10}$$

Substituting the converter dynamic equations (3) into (10) yields

$$v_C=\frac{\pi\alpha\beta L_O C_O}{4}\left(v_o^*-v_O\right)-\frac{\pi L_O C_O}{2}\left(\alpha+\frac{\beta}{2}-\frac{1}{R_L C_O}\right)\dot{v}_O+\frac{\pi}{2}\left(r_{Lo}i_{Lo}+v_O\right) \tag{11}$$

The control law (11) can be re-written as

$$v_C=\left(\frac{\pi\alpha\beta L_O C_O}{4}\right)e+\left(\frac{\pi L_O C_O}{2}\left(\alpha+\frac{\beta}{2}-\frac{1}{R_L C_O}\right)\right)\dot{e}+\frac{\pi}{2}\left(r_{Lo}i_{Lo}+v_O\right) \tag{12}$$

where α and β are tuneable parameters. From (12), the first and second terms of the controller represent a proportional-derivative (PD) controller. These terms eventually decay with the control action to zero as the system converges to the steady-state reference value. The third term of the controller represents the steady-state value of v_c which can be confirmed from equating the system derivatives in (3) to zero. Hence, this term can be considered as a *'feedforward'* term to stabilize controller action and speed transient response.

4. Closed loop stability and design

The control law (12) can be written in the form of a PD controller with feedforward

$$v_C=k_p e+k_d\dot{e}+\frac{\pi}{2}\left(r_{Lo}i_{Lo}+v_O\right) \tag{13}$$

where k_p is the proportional gain and k_d is the derivative gain. The closed loop structure is illustrated in Fig.3.

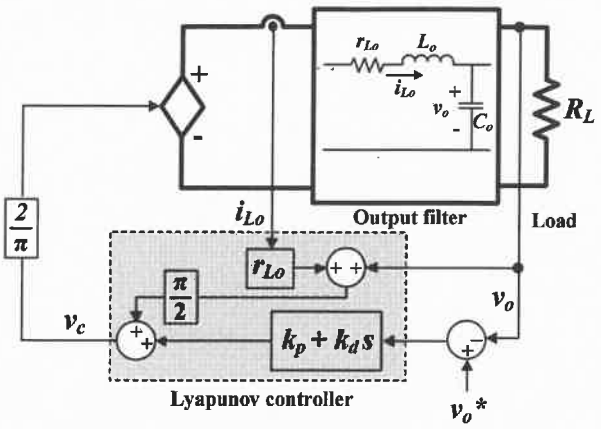

Fig.3: *Closed loop output voltage control using the proposed Lyapunov controller (reduced SPRC equivalent model).*

The open-loop transfer functions for the output filter described by (3) can be expressed as

$$V_O(s) = \frac{\frac{2}{\pi}}{L_O C_O s^2 + r_{LO} C_O s + 1} V_c(s) - \frac{L_O s + r_{LO}}{L_O C_O s^2 + r_{LO} C_O s + 1} I_O(s) \tag{14}$$

Considering the control-to-output voltage transfer function only (I_o=0), the proposed Lyapunov controller can be represented as shown in Fig.4.

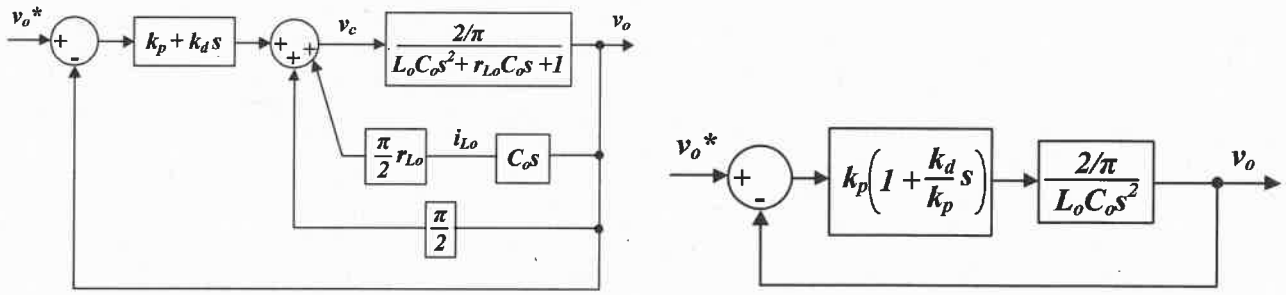

Fig. 4: *Closed loop system with Lyapunov controller*

(a) Full structure

(b) Reduced equivalent structure due to feedforward scheme.

The stability criteria can be obtained using the traditional Routh-Hurwitz criterion or in terms of the original Lyapunov controller parameters α and β defined in (12). Comparing (12) and (13):

$$\begin{aligned} k_p &= \frac{\pi \alpha \beta L_O C_O}{4} \\ k_d &= \frac{\pi L_O C_O}{2}\left(\alpha + \frac{\beta}{2} - \frac{1}{R_L C_O}\right) \end{aligned} \tag{15}$$

Solving (15) simultaneously for β yields

$$\beta^2 - \left(\frac{4k_d}{\pi L_o C_o} + \frac{2}{R_L C_o}\right)\beta + \frac{8k_p}{\pi L_o C_o} = 0 \tag{16}$$

The Lyapunov stability is strictly attainable only if β is positive as outlined by (7). According to (16), this is true if

$$\begin{aligned} \left(\frac{4k_d}{\pi L_o C_o} + \frac{2}{R_L C_o}\right) &> 0 \\ \frac{8k_p}{\pi L_o C_o} &> 0 \end{aligned} \tag{17}$$

which reduces to

$$\begin{aligned} k_p &> 0 \\ k_d &> -\frac{\pi L_o}{2R_L} \end{aligned} \tag{18}$$

This shows that the system is infinitely stable for all values of k_p and k_d. Since digital control is used, therefore discretizing the characteristic equation (derived from Fig. 4(b)) becomes crucial. Applying Euler's forward method yields

$$\left(\frac{1}{T_s^2}\right)z^2 + \left(\frac{2}{\pi L_o C_o T_s}k_d - \frac{2}{T_s^2}\right)z + \left(\frac{2}{\pi L_o C_o}k_p - \frac{2}{\pi L_o C_o T_s}k_d + \frac{1}{T_s^2}\right) = 0 \tag{19}$$

where T_s is the sampling period. According to Jury's stability criterion for discrete systems, conditions for closed loop stability can be expressed as

$$\begin{aligned} k_p &< \frac{k_d}{T_s} \\ k_p &> \frac{2k_d}{T_s} - \frac{2\pi L_o C_o}{T_s^2} \end{aligned} \tag{20}$$

Solving (20) simultaneously yields

$$\begin{aligned} k_p^* &= \frac{2\pi L_o C_o}{T_s^2} \\ k_d^* &= \frac{2\pi L_o C_o}{T_s} \end{aligned} \tag{21}$$

where k_p^* and k_d^* are the points of equality. Fig.5 illustrates a map of possible operating values for k_p and k_d to satisfy discrete closed loop system stability. Fig. 5(a) shows the k_p-k_d map with the closed loop output voltage transfer function solely, while the effect of the load is included in Fig. 5(b).

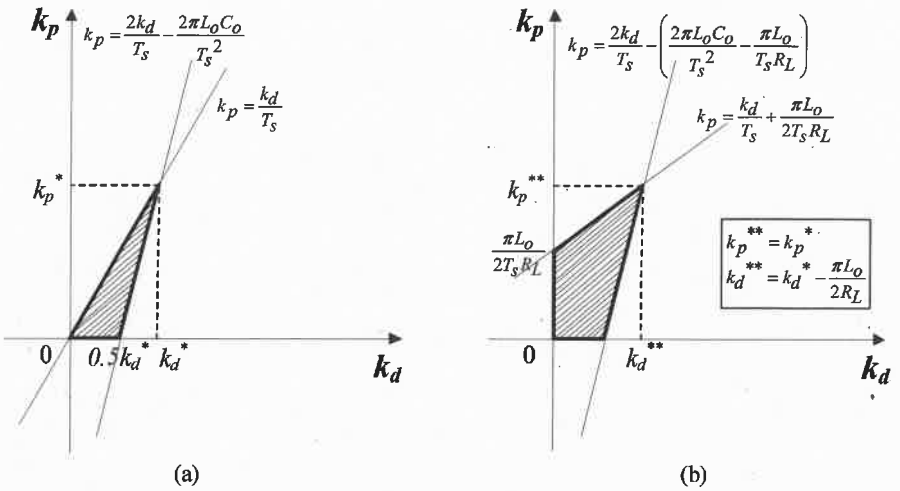

Fig. 5: *kp-kd map for closed-loop output voltage control stability margins*

(a) At no load

(b) With load

5. Performance comparison with PI control

Fig. 6 shows the proposed Lyapunov control algorithm implementation both experimentally and in Matlab simulation. Table 1 summarizes the circuit and control parameters used. All inverter switches are switched with a fixed 50% duty cycle; the only control variable being the phase shift angle δ between S_1 and S_3 as shown in Fig. 2(a). This controls the effective inverter output voltage duty cycle. The phase shift angle is updated every switching cycle (25μs) by the output control v_c from the Lyapunov controller.

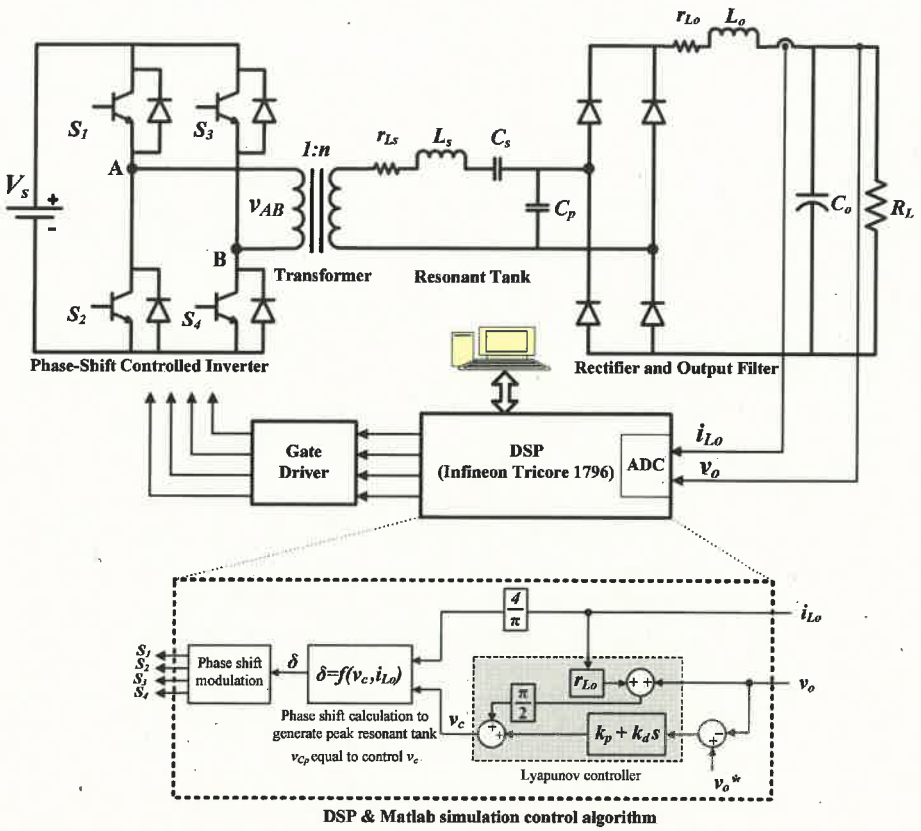

Fig. 6: Closed loop structure for phase-controlled SPRC using proposed Lyapunov controller

Table 1 *Circuit and controller parameters used in simulation and experiment*

Parameter	***Value***
Parasitic resistance of resonant tank inductor r_{Ls}	0.1916 Ω
Resonant tank inductance L_s	100.13 μH
Parasitic transformer resistance referred to secondary r_l	0.6 Ω
Transformer Leakage inductance referred to secondary L_l	9.12 μH
Resonant tank series capacitance C_s	0.255 μF
Resonant tank parallel capacitance C_p	0.255 μF
Parasitic resistance of output filter inductor r_{Lo}	0.5 Ω
Output filter inductance L_o	12.5 mH
Output filter capacitance C_o	120 μF
Resonant tank fundamental frequency f_s	40 kHz
Supply voltage V_s	60V
Transformer turns ratio n	0.5
Full-load power rating of experimental test rig	40W
Minimum load R_{Lmin}	40.5 Ω
Maximum load R_{Lmax}	14.4 Ω
Reference output voltage V_o^*	24V
Lyapunov controller proportional gain k_p	11.3313
Lyapunov controller derivative gain k_d	0.0047

Fig. 7 shows output voltage results for classical PI control and proposed Lyapunov controller comparing responses under step reference voltage (t=0) and step load disturbance from minimum load

(R_{Lmin}=40.5Ω) to maximum load (R_{Lmax}=14.4 Ω) at t=0.5s. Fig. 8 shows the Lyapunov controller response to a step input voltage disturbance from full supply voltage (V_s=60V) to half supply voltage (V_s=30V) at t=0.5s, at fixed minimum load.

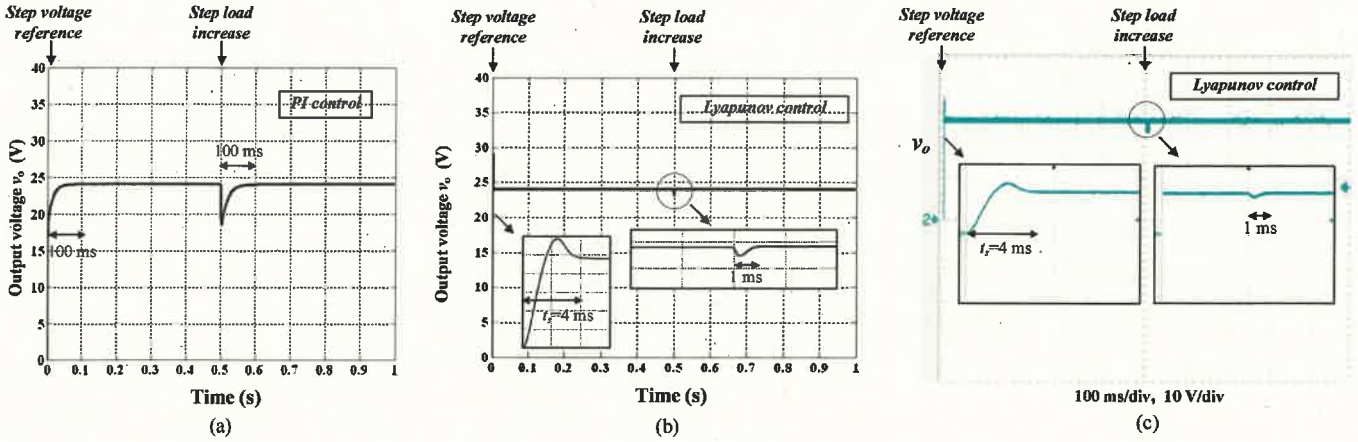

Fig. 7: *Results with step voltage reference and step load disturbance*

(a) Classical PI controller (simulation)

(b) Proposed Lyapunov controller (simulation)

(c) Proposed Lyapunov controller (experiment)

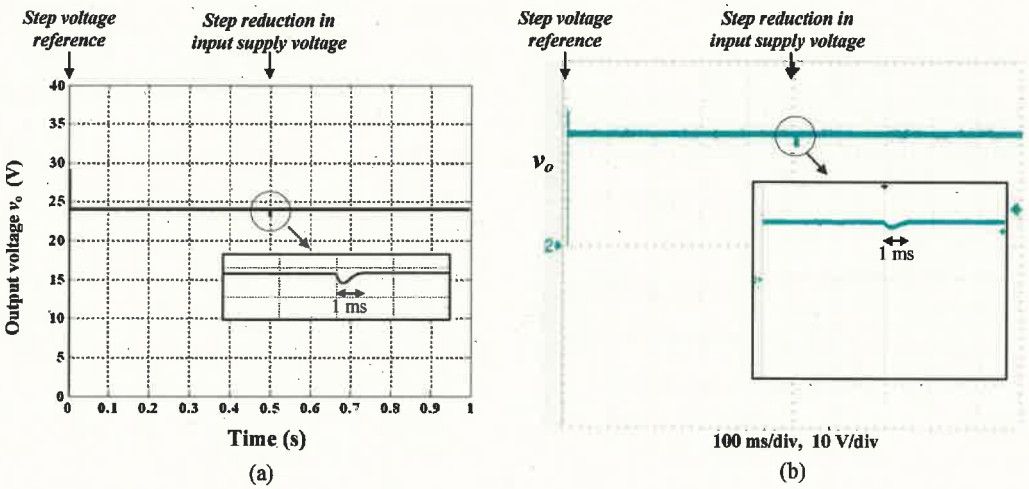

Fig. 8: *Results with step input voltage disturbance using the proposed Lyapunov controller*

(a) Simulation

(b) Experiment

Compared to PI control, the Lyapunov controller offers superior closed loop performance with a faster and more robust response to the applied disturbances. At startup, output voltage reaches desired reference value (V_o^*=24V) in 4ms compared to 100ms using PI control. This is due to the inherent feed forward mechanism that the Lyapunov controller implements. Existence of feed forward leads to stabilization of

controller response enabling the use of high loop gains to speed up response and increase disturbance rejection capability. Improved robustness and disturbance rejection are apparent from Fig. 7(b) and Fig. 8(a). It takes the Lyapunov controller 1ms to restore output voltage to reference value after application of both step load and step input voltage disturbances compared to 100ms for the PI control. Voltage dip is higher with PI control.

Table 2 summarizes the standard step response parameters, obtained in simulation, for the open loop converter compared to the closed loop performance with both the classical PI and the proposed Lyapunov-based controllers. Circuit and controller parameters used are highlighted in Table 1, and for the PI controller the proportional and integral gains are designed to achieve the fastest stable possible response as means of comparing best performance of PI with the proposed controller.

Table 2 *Step response performance parameters*

	Open loop system	*Lyapunov-based controller*	*PI controller*
Rise time (5% to 95%) [ms]	2.0	0.588	19.6
Peak time [ms]	4.1	1.2	9.0
Settling time [ms]	12.9	2.2	42.6
Peak overshoot [%]	28.34	18.54	327.4

Table 2 verifies the superior performance achieved by the Lyapunov-based controller.

6. Controller robustness and parameter sensitivity

The proposed controller is system parameter based and hence, variation of such parameters during operation will inevitably affect the closed loop response. Filter inductance, capacitance and parasitic resistances are all subject to variation due to various operational and environmental factors such as temperature, core saturation and cable overloading. It is therefore crucial to study how changes in these parameters would affect closed loop stability and dynamic response. Boundaries for system stability are derived and also the effect on dynamic performance is analysed.

Fig. 9 illustrates how the variation of system parameters affects the closed loop stability boundaries. Controller operating parameters $\hat{k}_p$ and $\hat{k}_d$ are fixed and designed according to the time domain operating requirements. As system parameters vary during operation, the stability region boundaries shift and if the selected controller parameters fall outside this region, the system becomes unstable. It is therefore necessary to calculate the ranges of change in system parameters that guarantee safe and stable operation.

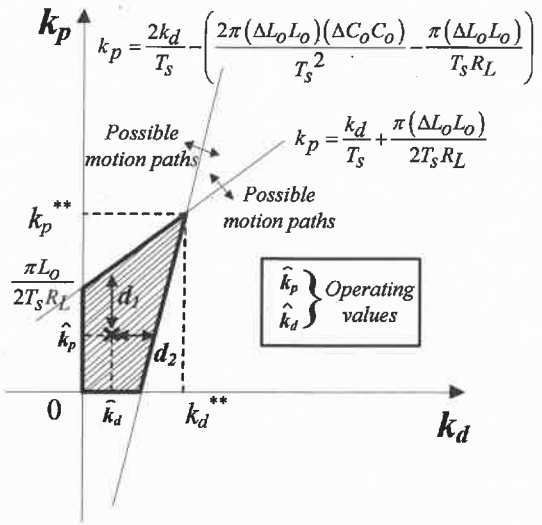

Fig. 9: *Closed loop stability margins for system parameter variation.*

Fig. 9 shows the possible motion paths for the stability region boundaries as the two main circuit parameters (L_o and C_o) change. ΔL_o and ΔC_o are per unit gains representing the change in L_o and C_o such that $\Delta L_o>0$ and $\Delta C_o>0$. It is worth noting that varying these parameters affects only the axis intercepts of the region boundaries, not the line gradients which are constant since T_s is fixed. As the region boundaries shift, the main conditions, from Fig. 9, required for closed loop stability to be maintained are

$$\begin{aligned} d_1 &> 0 \\ d_2 &> 0 \end{aligned} \tag{22}$$

where d_1 and d_2 are the clearances separating the operating points ($\hat{k}_p$ and $\hat{k}_d$) from the stability boundaries. Assuming C_o is constant (i.e. ΔC_o=1), the conditions for ΔL_o to satisfy stability can be expressed as

$$\begin{aligned} \Delta L_o &> \frac{1}{L_o}\frac{2R_L}{\pi}\left(T_s\hat{k}_p - \hat{k}_d\right) \\ \Delta L_o &> \frac{1}{L_o}\frac{2R_L}{\pi}\left(\frac{T_s\hat{k}_d - 0.5T_s^2\hat{k}_p}{2C_oR_L - T_s}\right) \end{aligned} \tag{23}$$

Equation (23) shows that for both region boundaries there exists a minimum value of L_o below which the system is unstable. This can be explained from Fig. 9 where, as L_o increases, both boundaries move further away from the operating points $\hat{k}_p$ and $\hat{k}_d$ and the system is more stable. However, an increase in L_o will produce a more sluggish dynamic response. The larger of the two values in (23) provides the global

condition for stability with regards to a change in L_o. Similarly, the condition for ΔC_o to satisfy stability can be obtained assuming L_o is constant (i.e. ΔL_o=1)

$$\Delta C_O > \frac{1}{C_O} T_S \frac{2R_L\hat{k}_d - T_S R_L \hat{k}_p + \pi L_O}{2\pi L_O R_L} \tag{24}$$

7. Modular input-series output-parallel operation

Fig. 10(a) shows the structure of n SPRC modules in ISOP connection. Detailed controller structure using the proposed Lyapunov controller for output voltage regulation is depicted in Fig. 10(b). Additional inner loops are included to ensure equal sharing of voltages and currents among the modules. Fig. 10(b) shows that the output from the Lyapunov-based controller is corrected by average input voltage sharing (IVS) loop which is indispensable to ensure equal distribution of voltages among the series input capacitors. With IVS, output current sharing (OCS) is achieved automatically for ISOP configurations without the need for dedicated OCS loops [25,26].

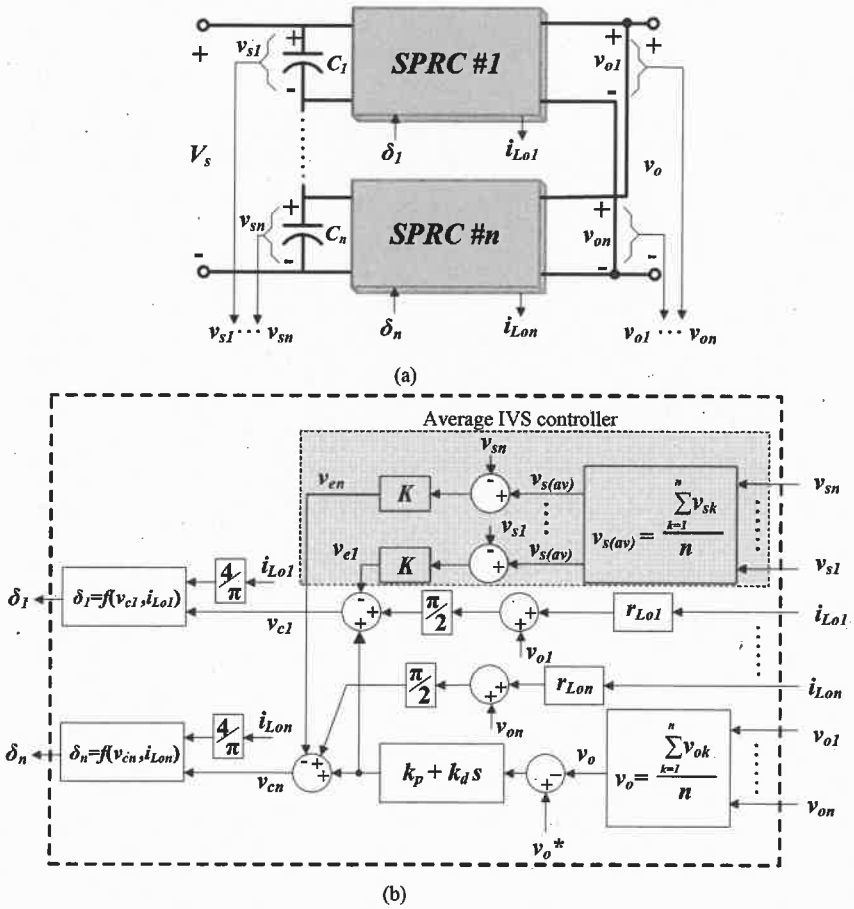

Fig. 10: ISOP connection of n SPRC modules

(a) Overall diagram

(b) Control structure with Lyapunov-based controller and input voltage sharing

Fig. 11 shows the implementation circuit for a two-module (n=2) ISOP connected SPRC. The two-module converter system operates in an interleaved mode to minimize load voltage and current ripple. Circuit parameter values per module are defined in Table 1. The two-module system will operate at 80W rated power (40W per module). In addition to the naturally unavoidable circuit parameter mismatches between the two converter modules, different input series capacitances and resonant tank transformer turns ratios are used to assess controller performance. Additional parameters values used in the simulation and experimental prototype are given in Table 3.

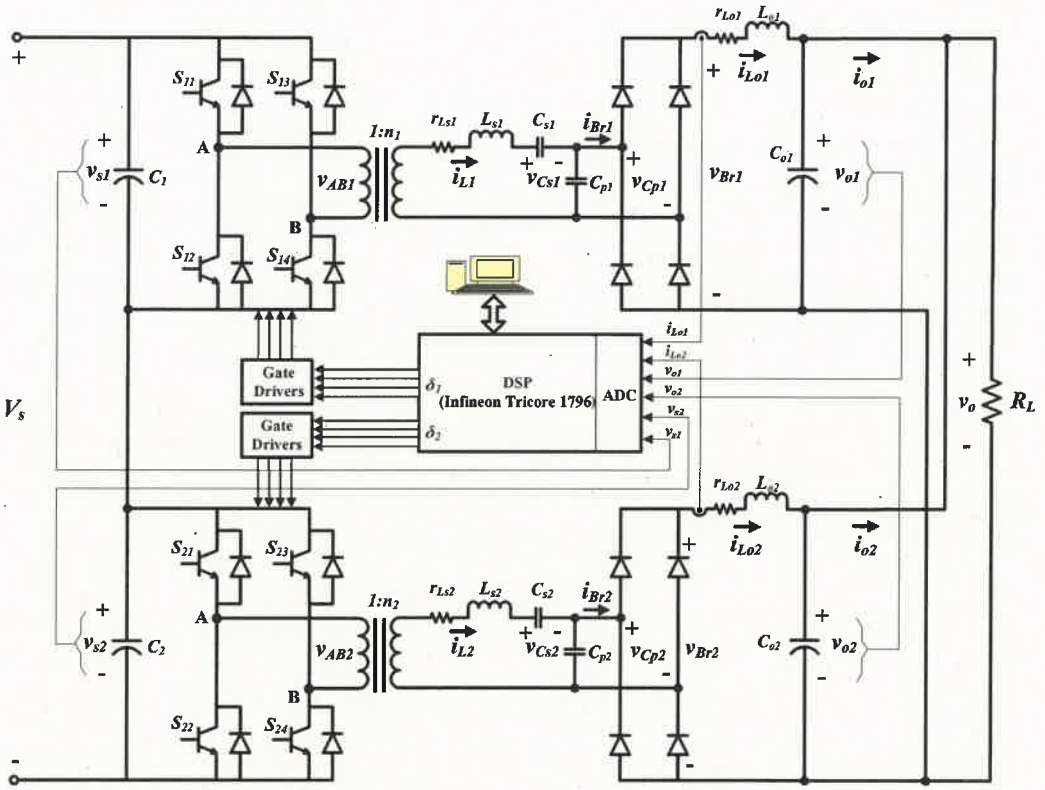

Fig. 11: *Circuit implementation for two-module ISOP connected SPRC.*

Table 3 *Operational and control values for the two-module ISOP system*

Parameter	***Value***
Full-load power rating of experimental test rig	80W
Input supply voltage V_s	120V
Reference load voltage v_o^*	24V
Switching frequency f	40 kHz
Minimum load R_{Lmin}	20.25 Ω
Maximum load R_{Lmax}	7.2 Ω
Lyapunov controller proportional gain k_p	11.3313
Lyapunov controller derivative gain k_d	0.0047
Average IVS control loop gain K	10
Input capacitance for module #1 C_1	30 μF
Input capacitance for module #2 C_2	60 μF
Transformer turns ratio for module #1 n_1	0.5
Transformer turns ratio for module #2 n_2	0.555

Fig. 12 shows results for the ISOP connected SPRC. A step disturbance from minimum load to full-load is applied at t=0.4s and a step input voltage reduction from V_s=120V to V_s=100V is applied at t=0.8s.

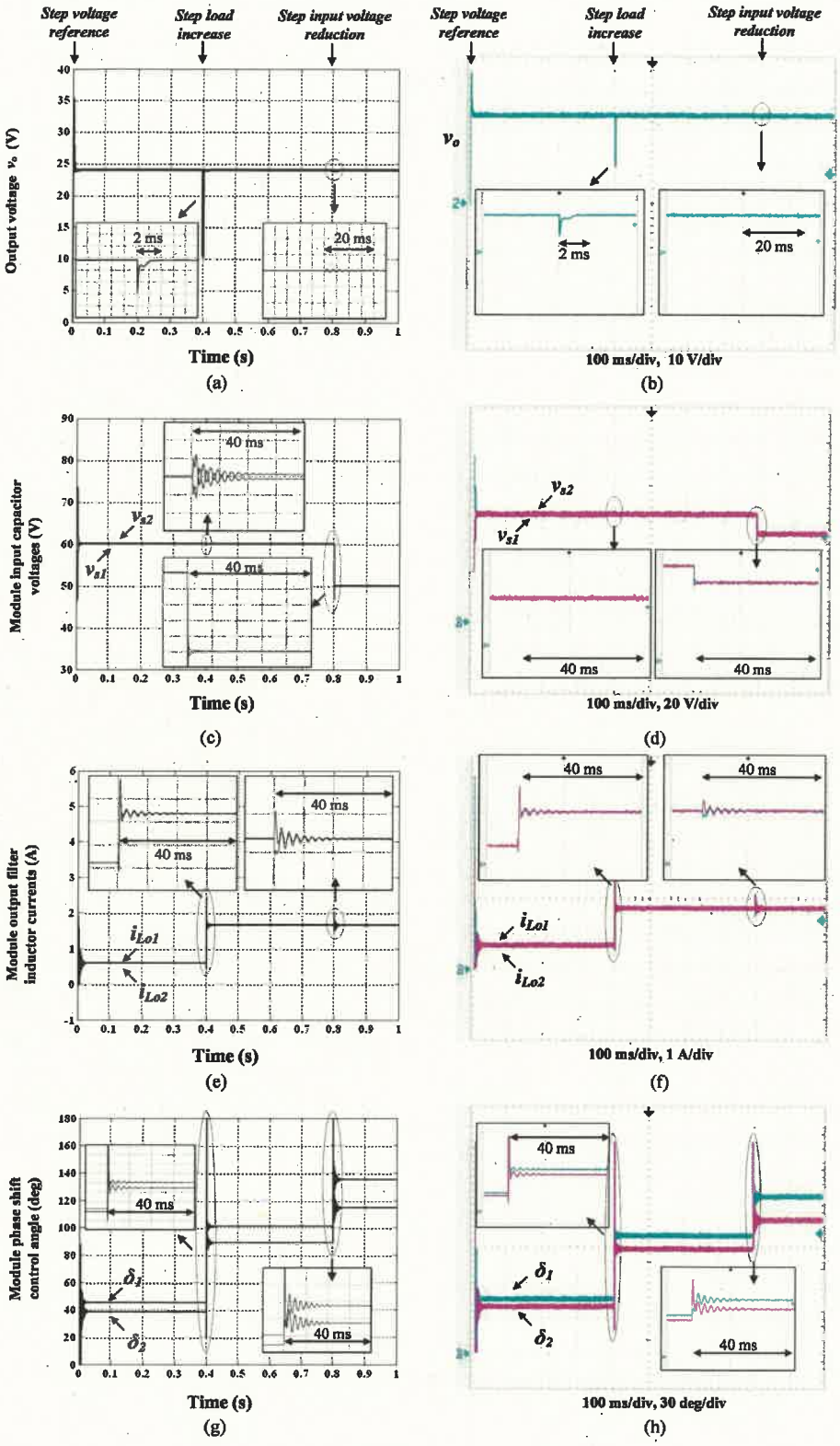

Fig. 12: *Results for the ISOP connected SPRC (a),(c),(e), (g) simulation, and (b),(d),(f), (h) experiment.*

The output voltage v_o in Fig. 12(a) and (b) follows the desired reference voltage v_o^*=24V. The robust Lyapunov controller rejects the step load disturbance in a fast and stable manner with a voltage dip lasting 2ms. Perturbation due to the step input voltage reduction is minimal. Fig. 12(c) and (d) shows equal sharing between the input series capacitor voltages, during full and reduced supply voltages, inspite the differences in input capacitances. IVS control provides fast and stable voltage distribution. Equal output current sharing is achieved automatically between the modules without dedicated OCS control. This confirms that for ISOP systems, IVS is sufficient to obtain stable operation. This is clear from results for i_{Lo1} and i_{Lo2} in Fig. 12(e) and (f), which show uniform current sharing in spite of non-uniform transformer turns ratios.

The phase shift control angles δ_1 and δ_2 are adjusted by control action to compensate for the mismatched transformer turns ratios. Module input voltages v_{s1} and v_{s2} are equal, therefore, module #2 with the higher turns ratio (n_2=0.555 > n_1=0.5) will always have a lower phase shift angle ($\delta_2<\delta_1$) so that both modules produce equal effective voltages. Fig. 12(g) and (h) illustrate the phase shift angles with $\delta_2<\delta_1$. Phase shift angles increase at t=0.4s due to increased loading, reflecting the need for more energy to be delivered to load to keep it at desired reference value. Also, when the input voltage is reduced at t=0.8s, further increases in δ_1 and δ_2 are required to compensate for the input voltage reduction.

8. Conclusion

This paper presented a high performance controller based on Lyapunov stability criterion for resonant DC/DC converters. The proposed controller inherently adopts a proportional-derivative + feedforward mechanism, giving superior dynamic performance as well as high disturbance rejection to step changes in load and input supply voltages compared to classical PI control. Analysis has also shown the high robustness of the proposed controller in response to converter circuit parameter changes. When applied in multiple module structure, the controller used additional active sharing control loops to ensure uniform current/voltage distribution across the multiple interconnected modules. The combined operation showed stable sharing of voltage and currents with excellent load voltage control characteristics. The modular DC/DC converter architecture and its associated proposed controls are a promising candidate for high performance medium voltage DC/DC converters.

9. References

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