Steady-state performance of state-of-the-art Modular Multilevel and Alternate Arm Converters with DC fault-blocking capability

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Abstract

This paper presents a comparison of the steady-state behaviour of four state-of-the-art HVDC converters with DC fault-blocking capability, based on the modular multilevel and alternate arm converter topologies. AC and DC power quality, and semiconductor losses are compared, whilst considering different operating conditions and design parameters, such as the number of cells and component sizing. Such comparative studies have been performed using high-fidelity converter models which include detailed representation of the control systems, and of the converter thermal circuit. The main findings of this comprehensive comparison reveal that, the mixed cell modular converter offers the best design trade-off in terms of power losses and quality, and control range. Moreover, it has been established that the modular converter with a reduced number of cells per arm and with each cell rated at high voltage (i.e. 10-20 kV), tends to exhibit higher switching losses and relatively poor power quality at the DC side.

Keywords: HVDC, power losses, power quality, converter modelling

1. Introduction

The rapid growth of renewable energy production, particularly from remote offshore wind farms, requires efficient transmission system technology, which can transmit power and support both offshore and onshore grids. Existing multilevel voltage source converter based High Voltage Direct Current (HVDC) transmission systems, have received universal acceptance from the power industry. This is due to the fact that they satisfy the aforementioned requirements, offer high efficiency and high power quality at both AC and DC sides, and provide internal fault management which is critical for facilitation of continuous operation during cell failure [1, 2, 3].

Reverse-blocking converters (or simply converters with DC fault blocking) are increasingly important as they provide a means to ride-through solid DC short-circuit faults, with only short periods of power

interruption between the connected AC grids. This is achieved without significant impact on voltage stability as the reverse-blocking converters can prevent or control the AC-side contribution to the DC fault current. Hence, reactive power within connected AC grids, will be no longer flowing uncontrollably. In multi-terminal HVDC networks which utilise reverse-blocking converters, DC-link voltage remains at zero after fault clearance, as long as the converter terminals remain blocked. This clearly provides the opportunity for complete replacement of expensive DC circuit breakers with lower-cost DC disconnectors [4]. Typical modern multilevel HVDC converters, have complex power circuit structures with complex internal dynamics (inter-cell, inter-arm and inter-phase dynamics), that require a number of well-designed dedicated controllers to ensure converter stability over the entire operation range [5, 6, 7, 8]. Analytical performance evaluation of such converters is time-consuming and could be ineffective. For example, it is cumbersome to account for the effect of complex Capacitor Balancing Algorithms (CBAs) in average models. This is due to the fact that CBAs affect the average switching frequency per switching device (switching loss), arm energy balance and inter-arm dynamics, and hence, average models are unable to reproduce such effects [9, 10].

Several attempts have been made to estimate semiconductor conduction and switching losses in modular multilevel converters [11, 12, 13, 14], however, numerous calculation of losses found in the open literature, differ significantly. For example, estimation of semiconductor losses for a half-bridge modular converter varies from 0.3% to 1% [11, 12]. This is because some of these studies do not account correctly for important considerations such as the CBA and modulation, redundancy, and temperature effects. In contrast, detailed estimation of semiconductor losses for several modular and hybrid converters, including mixed-cell MMC and AAC, have been presented in [13] including the impact of different modulation methods. However, this study neglects thermal effects and the possibility of incorporating redundant cells. As in previous studies, the loss estimations presented in [14] are extremely low, and opposite to widely accepted figures for conversion losses in modular and hybrid type converters [11, 13].

At present, there are two competing approaches to the realisation of modular multilevel converters. The first approach utilises a large number of cells per arm, where the blocking capability of each cell is small and is defined by the rating of a single switching device (i.e. 2-3 kV). The second approach adopts a reduced number of cells per arm, with each cell rated for high DC operating voltage, ranging between 16-20 kV. Thus, the latter approach requires the adoption of series-connected semiconductor devices. To date, no detailed studies available in the open literature have investigated the potential impact of a reduced number of cells on power quality, both on AC and DC sides but also on semiconductor losses in the MMC. Similar

research gaps have been identified on the analysis of the AAC, particularly with regard to power quality on the DC side.

This paper presents a novel research approach which utilises detailed converter models (developed in EMTP-RV [9, 15]) and a well-designed set of test scenarios. The ultimate goal is to compare the performance of different converters, with emphasis given to Alternate Arm Converter (AAC) [16] and Modular Multilevel Converter (MMC) [17] and its derivatives, namely the Mixed-Cell MMC (MC-MMC) [18]. The main performance indicators used in the comparison are i) capacitor voltage ripple, ii) cell capacitance or energy storage requirement per converter, and iii) semiconductor losses. Both MMC and AAC topologies include full-bridge cells which can reverse the cell voltage polarity and therefore block DC current [19, 20]. Both Full-Bridge MMC (FB-MMC) and Half-Bridge MMC (HB-MMC) are investigated [5], even though the HB-MMC does not have blocking capability. Also this paper presents a concise description of the operating principles and modelling of each converter topology, including the formulae which govern operation, and accurately reflects the internal and external dynamics, thermal behaviour and semiconductor losses. The main results obtained from these models are thoroughly discussed and the main factors that affect the power quality on the AC and DC sides, losses and potential design trade-offs are identified.
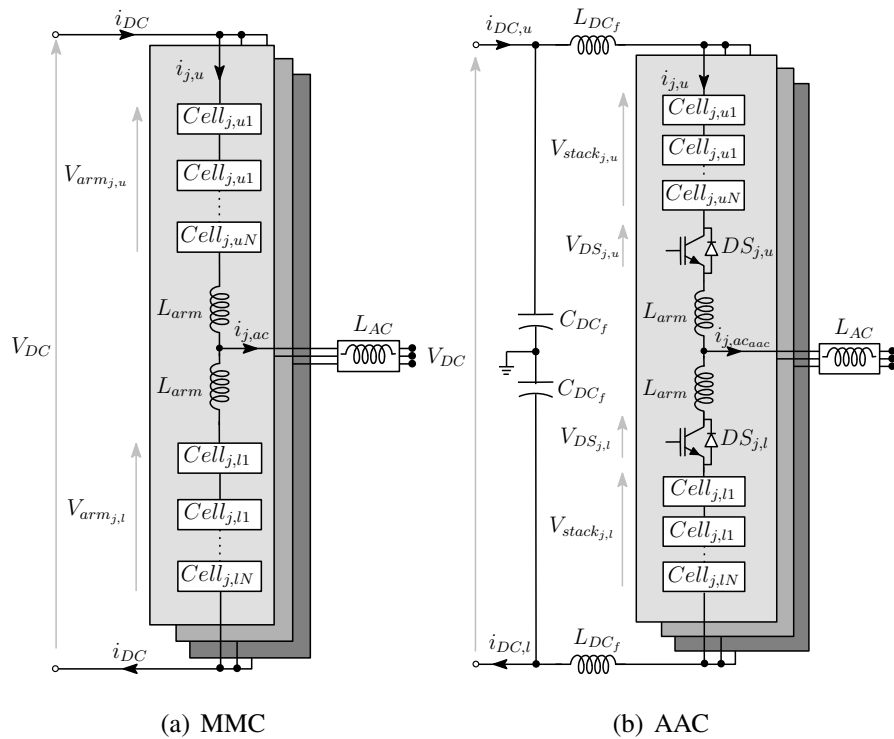

(a) MMC   (b) AAC

Figure 1: Phase representation of converter topologies.

2. Converter modelling

This section briefly reviews the theoretical background which underpins the operating principles, control, and modelling of the MMC and AAC. A generic method for estimating semiconductor losses, which takes into account the effect of temperature on conduction and switching losses, is also presented.

Fig. 1 shows one phase leg, each for generic MMC and AAC circuits with N_{cell} number of cells per arm with subscript j defines the phase index (i.e. $j = a, b, c$) and k defines the upper and lower position of the arm (i.e. $k = u$ for the upper arm and $k = l$ for the lower arm).

2.1. Brief review of MMC

From Fig. 1 the cell capacitor current of each individual cell can be described in terms of arm current $i_{j,k}$ and the switching function $s_{cell-n_{j,k}}$ {-1,0,1} as stated in (1):

$$i_{cell-n_{j,k}} = (1 - s_{cell-n_{j,k}}) \cdot i_{j,k} \tag{1}$$

Each arm voltage $v_{arm_{j,k}}$ (3) is formed by the summation of individual cell voltages $v_{cell-n_{j,k}}$ as described in (2):

$$v_{cell-n_{j,k}}(t) = \frac{1}{C_{cell}} \cdot \int_{t-\Delta t}^{t} \left(i_{cell-n_{j,k}}(t) \right) dt \tag{2}$$

where Δt is the time step of the discrete integration.

$$v_{arm_{j,k}} = \sum_{i=1}^{N_{cell}} \left[(1 - s_{cell-n_{j,k}}) \cdot v_{cell-n_{j,k}} \right] \tag{3}$$

The voltage across the DC link can be expressed in terms of the instantaneous upper and lower arm voltages ($v_{j,u}$, $v_{j,l}$) of the same phase leg:

$$V_{DC} = v_{j,u} + v_{j,l} \tag{4}$$

Considering Fig. 1(a), the following voltage equations can be defined:

$$\frac{V_{DC}}{2} = v_{j,u} + \frac{L_{arm}}{2} \cdot \frac{di_{j,u}}{dt} - L_{AC} \cdot \frac{di_{j,AC}}{dt} + e_j \tag{5}$$

$$\frac{V_{DC}}{2} = v_{j,l} + \frac{L_{arm}}{2} \cdot \frac{di_{j,l}}{dt} + L_{AC} \cdot \frac{di_{j,AC}}{dt} - e_j \tag{6}$$

where L_{arm} and L_{AC} are the arm and AC-side inductances respectively (as shown in Fig. 1a) and e_j is the AC-side grid phase voltage. The upper and lower arm currents in each phase can be expressed by (7) and (8) respectively [21]:

$$i_{j,u} = \frac{i_{j,AC}}{2} + i_{j,diff} \tag{7}$$

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$$i_{j,l} = -\frac{i_{j,AC}}{2} + i_{j,diff} \tag{8}$$

where $i_{j,AC}$ and $i_{j,diff}$ are the AC output phase and differential currents respectively. Current $i_{j,diff}$ flows through the upper and lower arms (however does not contribute to the AC output current) and can be defined by (9):

$$i_{j,diff} = \frac{i_{j,u} + i_{j,l}}{2} = i_{j,DC} + i_{j,cc} \tag{9}$$

$$i_{DC} = i_{a,DC} + i_{b,DC} + i_{c,DC} \tag{10}$$

where $i_{j,DC}$ and $i_{j,cc}$ are the DC and circulating currents respectively and the latter occurs due to the unbalanced voltages between the upper and lower arms in each phase.

$$v_{j,diff} = \frac{V_{DC}}{2} - v_{j,u} = -\frac{V_{DC}}{2} + v_{j,l} = \frac{v_{j,l} - v_{j,u}}{2} \tag{11}$$

where $v_{j,diff}$ is the differential voltage between the upper and lower arms and can be considered as the electromotive force (EMF) generated in each phase.

2.2. Brief review of AAC

As illustrated in Fig. 1(b), each AAC arm consists of series-connected FB cells and a director switch (DS). Cell capacitor current and voltage can be described similarly to (1) and (2), and therefore voltage $v_{stack_{j,k}}$ is considered to be identical to arm voltage as described by (3). The operation principle of an AAC is a combination of an MMC and a two-level converter, and can be described by the following three distinctive stages[19]:

- Stage I: Single arm conduction

- Stage II: Overlap

- Stage III: Off-state

During Stage I, the arm voltage is equal to $v_{stack_{j,k}}$ and the arm current is equal to $i_{j,AC}$. In Stage II, the AAC operates as an MMC where both the upper and lower arms conduct simultaneously for a very short period of time, in order to re-balance the voltage across the upper and lower stacks. In Stage III, the DS in the outgoing arm is turned off to stop the current flow, and enable the outgoing arm to block the full DC

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voltage. The time frames in (12) summarize the operation of the AAC during Stages I, II and III.

$$\begin{cases} t_{j,u_1} = -\frac{T}{2} + \frac{t_{over}}{2} + T \cdot s_{DS_{j,u}} \\[2mm] t_{j,u_2} = \frac{T}{2} - \frac{t_{over}}{2} + \frac{T \cdot s_{DS_{j,u}}}{2} \\[2mm] t_{j,l_1} = -\frac{T}{2} + \frac{t_{over}}{2} + T \cdot (1 - s_{DS_{j,l}}) \\[2mm] t_{j,l_2} = \frac{T}{2} - \frac{t_{over}}{2} + \frac{T \cdot (1 - s_{DS_{j,l}})}{2} \end{cases} \tag{12}$$

where T is the fundamental period, t_{over} is the overlap time and $s_{DS_{j,k}}$ is the switching function of DS. Considering (12), the output DC voltage can be expressed in terms of the average voltage of the upper and lower arms, as in shown in (13).

$$\begin{aligned} V_{DC} = {} & \frac{1}{T} \cdot \int_{t_{j,u_1}}^{t_{j,u_2}} v_{stack_{j,u}}(t) + v_{DS_{j,l}}(t) dt \\ & + \frac{1}{T} \cdot \int_{t_{j,l_1}}^{t_{j,l_2}} v_{stack_{j,l}}(t) + v_{DS_{j,u}}(t) dt \end{aligned} \tag{13}$$

It is evident from (14) that the AC current is mainly composed by the conducting arm current $i_{j,k}$. It can be deduced that this is taking place during Stage I and II.

$$\begin{aligned} i_{j,AC_{aac}} = {} & \frac{1}{T} \cdot \int_{t_{j,u_1}}^{t_{j,u_2}} i_{j,u_{aac}}(t) dt \cdot s_{DS_{j,u}} + \\ & + \frac{1}{T} \cdot \int_{t_{j,l_1}}^{t_{j,l_2}} i_{j,l_{aac}}(t) dt \cdot (1 - s_{DS_{j,l}}) \\ = {} & i_{j,u_{aac}} + i_{j,l_{aac}} \end{aligned} \tag{14}$$

The instantaneous $\frac{V_{DC}}{2}$ can be expressed by (15) and (16) for upper and lower arm respectively:

$$\frac{V_{DC}}{2} = v_{stack_{j,u}} + v_{DS_{j,l}} + L_{arm} \cdot \frac{di_{j,u_{aac}}}{dt} - L_{ac} \cdot \frac{di_{j,AC_{aac}}}{dt} \tag{15}$$

$$\frac{V_{DC}}{2} = v_{stack_{j,l}} + v_{DS_{j,u}} - L_{arm} \cdot \frac{di_{j,l_{aac}}}{dt} + L_{AC} \cdot \frac{di_{j,AC_{aac}}}{dt} \tag{16}$$

At AAC the DC currents i_{DC_u} and i_{DC_l} are composed according to (17). Due to the fact that AAC arm currents conduct similar to a two-level converter, inherently DC currents contain a 6th harmonic ripple component, which will be demostrated in Section 4.1.

$$\begin{cases} i_{DC_u} = i_{a,u_{aac}} + i_{b,u_{aac}} + i_{c,u_{aac}} \\[2mm] i_{DC_l} = i_{a,l_{aac}} + i_{b,l_{aac}} + i_{c,l_{aac}} \end{cases} \tag{17}$$

2.3. Semiconductor loss calculation

Since semiconductor losses represent the major portion of the total converter station losses, all the other losses such as transformer windings, passive components etc. have been excluded. The IGBT losses consist of conduction losses during the ON state, and switching losses during the transition between ON and OFF states and vice versa. Tables 1 and 2 show the switching transitions and conduction paths corresponding to FB and HB cells shown in Fig. 2.
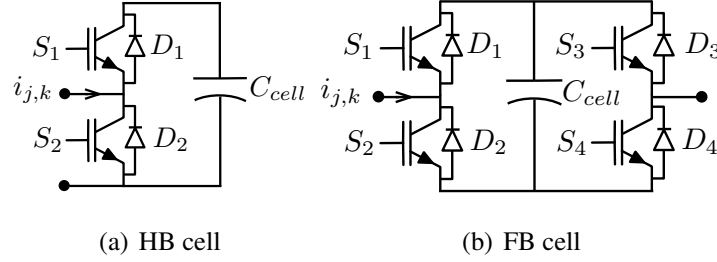

(a) HB cell   (b) FB cell

Figure 2: Cell topologies.

IGBTs exhibit both conduction and switching power losses. Typically, a piecewise representation (see $'data'$ in (18), (21)) of switching energy during turn-on and turn-off events is used to calculate IGBT switching losses, while the IGBT voltage drop is used to estimate conduction losses. The losses are calculated based on an initial junction temperature that is similar to ambient T_{amb}. The voltage drop during IGBT conduction can be defined as a function of arm current and operating temperature, as shown in (18):

$$\begin{cases} V_{ce_{data}} = Vce\left(\frac{|i_{arm}|}{n_p}, \vartheta_S\right)_{data} \\ V_{f_{data}} = Vf\left(\frac{|i_{arm}|}{n_p}, \vartheta_D\right)_{data} \end{cases} \tag{18}$$

$$V_{loss_{cell}} = V_{ce_{data}} + V_{f_{data}} \tag{19}$$

Temperature calculation is carried out using a steady-state thermal model, considering the thermal resistances for each part of an IGBT, according to (20).

$$\begin{cases} \vartheta_S = P_{cond_S} \cdot (R_{j_S} + R_{c_S} + R_{hs}) + T_{amb} \\ \vartheta_D = P_{cond_D} \cdot (R_{j_D} + R_{c_D} + R_{hs}) + T_{amb} \end{cases} \tag{20}$$

Table 1: HB cell operation

Current	Cell state	Transition	Conduction
Positive	0 to Vc	$D_{1_{ON}}, S_{2_{OFF}}$	D_1
	Vc to 0	$D_{1_{OFF}}, S_{2_{ON}}$	S_2
Negative	0 to Vc	$D_{2_{OFF}}, S_{1_{ON}}$	S_1
	Vc to 0	$S_{1_{OFF}}, D_{2_{ON}}$	D_2

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Table 2: FB cell operation

Current	Cell state	Transition	Conduction
Positive	0 to Vc	$D_{1_{ON}}, S_{2_{OFF}}$	D_1, D_4
	Vc to 0	$D_{1_{OFF}}, S_{2_{ON}}$	S_2, D_4
	0 to -Vc	$D_{4_{OFF}}, S_{3_{ON}}$	S_2, S_3
	-Vc to 0	$S_{3_{OFF}}, D_{4_{ON}}$	S_2, D_4
Negative	0 to Vc	$D_{2_{OFF}}, S_{1_{ON}}$	S_1, S_4
	Vc to 0	$S_{1_{OFF}}, D_{2_{ON}}$	D_2, S_4
	0 to -Vc	$D_{3_{ON}}, S_{4_{OFF}}$	D_2, D_3
	-Vc to 0	$D_{3_{OFF}}, S_{4_{ON}}$	D_2, S_4

where R_j, R_c, R_{hs} are the junction-to-case, case-to-heat-sink and heat-sink-to-ambient thermal resistances respectively. IGBT and diode conduction losses are calculated according to (21):

$$
\begin{cases}
P_{cond_S} = \frac{1}{T} \int_{t-T}^{t} V_{ce_{data}} \cdot \frac{|i_{arm}|}{n_p} \cdot K_{uti} \cdot n_s \cdot n_p \, dt \\
P_{cond_D} = \frac{1}{T} \int_{t-T}^{t} V_{f_{data}} \cdot \frac{|i_{arm}|}{n_p} \cdot K_{uti} \cdot n_s \cdot n_p \, dt
\end{cases}
\tag{21}
$$

where n_s and n_p are the number of series and parallel-connected IGBTs and diodes respectively, and K_{uti} is the utilization constant described by (30). The number of series and parallel connected IGBTs is described by (22) and (23) respectively:

$$
n_s = ceil\left(\frac{V_{chain}}{V_{igbt} \cdot N_{cell}}\right)
\tag{22}
$$

$$
n_p = ceil\left(\frac{i_{j,k}}{I_{igbt}}\right)
\tag{23}
$$

where V_{chain} is the total voltage across the stack per arm, and I_{igbt} and V_{igbt} are the continuous rated current and blocking voltage of a single IGBT respectively. The energy which is dissipated during the switching process can be defined as a function of the instantaneous arm current and the switching energy of the IGBT, as shown in (24). Thereafter, the switching losses are calculated according to (25).

$$
E_{sw} = \left(\frac{|i_{arm}|}{n_p}\right) \cdot \left(E_{S_{on}} + E_{S_{off}} + E_{D_{off}}\right)_{data}
\tag{24}
$$

$$
P_{sw_S} = \frac{1}{T} \sum_{t-T}^{t} E_{sw} \cdot K_{uti} \cdot K_T \cdot n_s \cdot n_p
\tag{25}
$$

where K_T, (defined in (26)), is a thermal correction factor and is utilized to normalize the temperature according to the IGBT thermal model.

$$
K_T = \frac{\vartheta_S, \vartheta_D}{\vartheta_{max_{data}}}
\tag{26}
$$

2.4. Implementation of Arm model

Full-scale representation of AAC and MMC with large numbers of cells per arm using detailed switched models are characterised by large numbers of electrical nodes, which increase the size of the admittance

matrix; thus computation burden on the processor. The effectiveness of conventional electromagnetic transient simulation program approach in simulation acceleration of full-scale converter models is widely acknowledged; however, much faster simulation speed could be achieved if the switching function modelling approach is adopted. [9]. Fig. 3 shows the switching function representation of the cells in terms of arm current and firing order, as it was described in (1) and (2). As the discrete integration of (2) determines the fidelity of the results, a small time step of $5\mu s$ is necessary in order to achieve high accuracy.
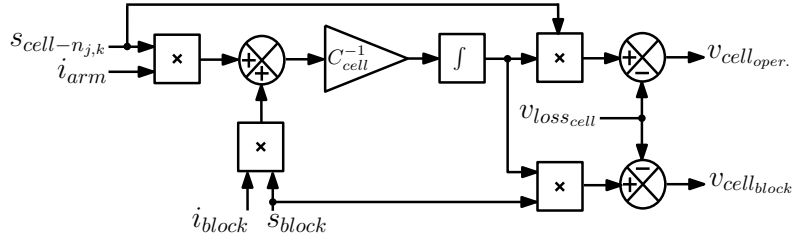

Figure 3: Cell voltage block diagram.

Moreover, an enhanced version of the switching model is used [22], by reflecting the switching losses through a calculated voltage drop v_{loss}, as described later in (19). Fig. 4 illustrates the HB, FB cell stacks as described in (3) and the DS. The controlled voltage source added into the DS model in Fig. 4(a) accounts for its switching and conduction losses, which are critical for accurate estimation of semiconductor losses in AAC. For example the chainlink in Fig. 4(a) in series with 4(c) resemble the arm of AAC, while the chainlink in Fig. 4(b) in series with 4(c) resemble the arm of MC-MMC.
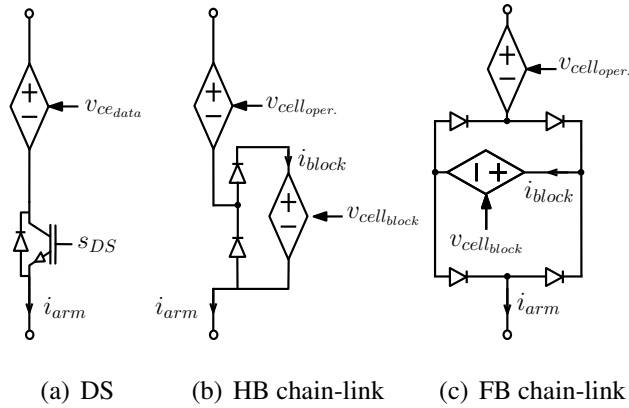

(a) DS   (b) HB chain-link   (c) FB chain-link

Figure 4: Equivalent representations of arm components.

The complete block diagram for loss calculation, integrating thermal models, switching patterns and manufacturer data sheets, is depicted in Fig. 5.
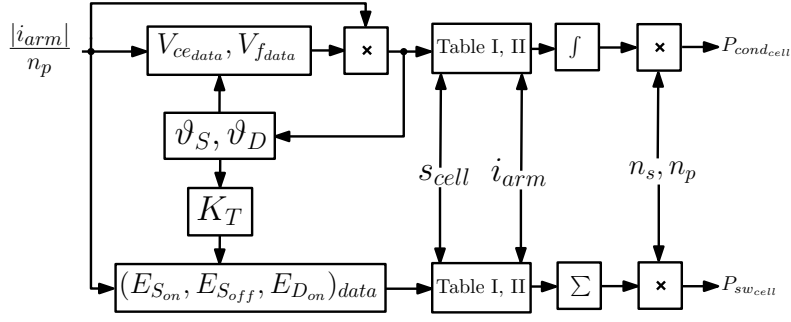
Figure 5: Block diagram of loss calculation scheme.

2.5. Controllers

The generic control structure for all MMC and AAC being considered in this paper can be reduced, as shown in 6, which consist of set-point, phase balance and arm balance controllers. The details for each component of Fig. 6 will be elaborated further. For any converter topology, the principles for designing set- point and arm balance control can be similar. However, the actual implementation of phase balance control may differ from topology to topology depending on the different operational philosophies of each converter.
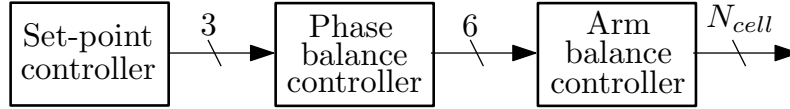

Figure 6: Generalised representation of converter control layers.

2.6. Set-point controller

Set-point controller determines the references for power, DC voltage, active and reactive current components as shown in Fig. 7. In such control scheme, there is a combination of decoupled current sub-controllers (i.e. outer and inner controller) alongside PI regulators and grid synchronization unit. The same set-point controller may be applied to any converter topology.

2.7. Phase balance controller

The phase balance controller ensures the vertical and horizontal stability of the converters internal dynamic energy imbalances. Mainly these dynamic imbalances are due to the tolerances of installed passive and active components, such as arm inductances and cell capacitors. In MMC this may lead to a fluctuation of energy in each phase which, in turn, will generate circulating currents. In AAC it may increase the magnitude of the rebalancing current in the arms during the overlap period.
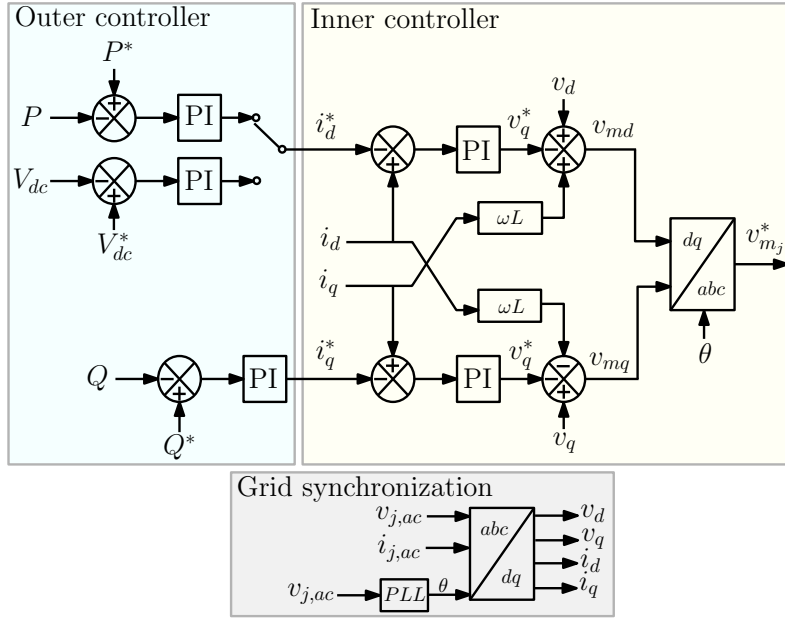
Figure 7: Set-point controller [5].

2.7.1. Circulating current controller (MMC)

There are various methods for active suppression of the circulating currents, which mainly affect the magnitude of the arm current, cell voltage ripple and the semiconductor losses. In this paper the DQ version of the Circulating Current Suppression Controller (CCSC) is used, as shown in Fig. 8 [6].
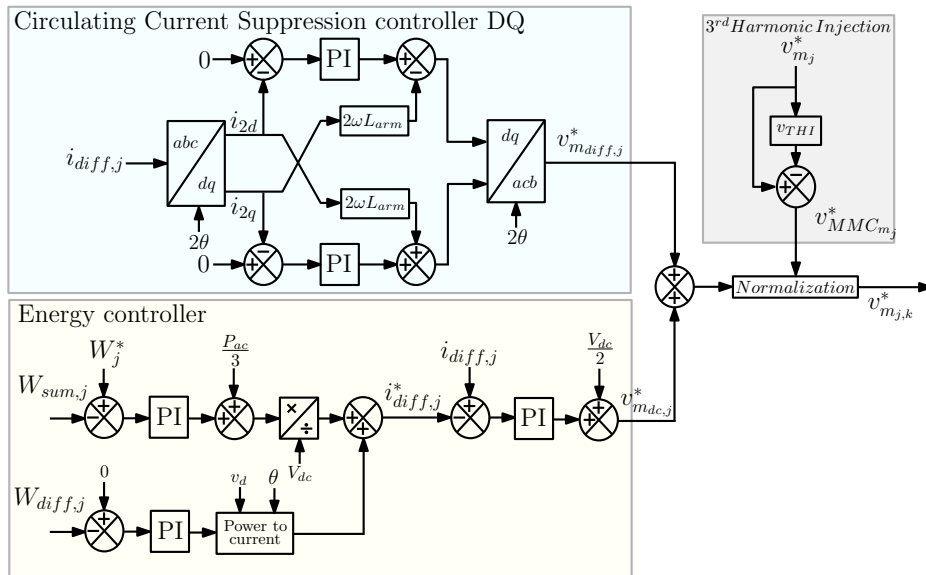

Figure 8: MMC phase controller.

2.7.2. Energy controller (MMC)

The energy controller is employed to ensure energy balance between the upper and lower arms in each phase. It also decouples cell capacitor voltage regulation, and hence the AC voltage, from the DC link. In this manner, the energy stored in the cell capacitors can be manipulated to adjust DC components of the modulation signals, and the CSCC could potentially be eliminated [7].

2.7.3. Overlap angle controller (AAC)

This type of controller exists only in AAC converters, and regulates the period during which both arms conduct simultaneously. Although different implementations of overlap angle control, such as average energy and current-based control, exist [23, 24],such implementations may be inadequate if hardware delays are also considered. In the utilised models, therefore, fixed overlap angles (which are dependent upon modulation index) are adopted, as shown in Fig. 9.
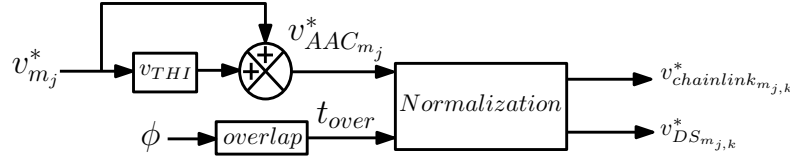

Figure 9: AAC phase controller.

2.7.4. Third Harmonic Injection (MMC/AAC)

Traditionally, the third harmonic injection (THI) technique is used to extend the modulation index linear range and improve DC link utilisation in order to improve converter PQ capability. The third harmonic voltage injected into the modulated signals of the MMC and AAC is described by (27):

$$v_{THI} = \frac{min(v^*_{m_a}, v^*_{m_b}, v^*_{m_c}) + max(v^*_{m_a}, v^*_{m_b}, v^*_{m_c})}{2} \tag{27}$$

In AAC THI extends the period where the AAC operates as an MMC by modifying the voltage profile in the region of zero voltage crossover. This results in more in a efficient operation during the overlap period, and allows better energy equilibrium between the upper and lower arms regardless of the overlap period [25]. In AAC, THI removes the necessity for current injection from a star-connected transformer [26], and reduces the DC filtering requirements [25]. THI permits MMC to operate with higher range of converter AC voltage, which is beneficiary in terms of potential reduction in transformer and arm currents for the same power transfer [27]. Equations (28) and (29) describe the implementation of THI in AAC and MMC respectively.

$$v_{AAC_{m_j}} = v_{m_j} + v_{THI_j} \tag{28}$$

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$$v_{MMC_{m_j}} = v_{m_j} - v_{THI_j} \tag{29}$$

2.8. Arm balance controller

Arm balance controller is used both MMCs and AAC, to achieve equal voltage stress on the cell capacitors and switching devices. In this paper a tolerance band CBA is utilised [8], which allows robust control operation, as it does not rely upon a complex sorting function and minimises computational effort as only the voltages that exceed the defined tolerance band need to be considered. The combination of tolerance band CBA with nearest level modulation allows well-balanced cell capacitors, as shown in Fig. 10(a) and 10(c). This is achieved by inserting or bypassing the cells which only operate for a short period during fundamental cycle, as illustrated in Fig. 10(b) and 10(d). As a result, the overall average switching frequency of the converter remains low, as depicted in Fig. 10(e).

3. Design Methodology

This section describes the procedures followed for designing the main converter facets, such as the number of cells, and the passive component values, (i.e. cell capacitor and arm inductance). For ease of comparison, the design has been accomplished assuming the same rated power, DC voltage and voltage stress per device.

3.1. Number of cells and semiconductors

The number of cells N_{cell} is defined by two factors. Firstly, the AC power quality requirements need to be fulfilled according to the grid code of each country. The higher the number of cells, the better the quality of AC voltage generated by the converter. The second factor is related to the converter's operating power and DC voltage. Each cell must be rated to support $V_{cell} = V_{chain}/N_{cell}$. The use of parallel IGBTs reduces the semiconductor losses and allows the use of lower current-rated IGBTs, while series connection reduces the number of cells, and hence power circuit and control complexity, and creepage and clearance requirements. Since series connection of IGBTs is not a straightforward task, it is more common to design cells to support voltage across single IGBT devices. Practically, the blocking voltage V_{igbt} of an IGBT is selected to enable stable operation and prolonged lifespan, and to sustain transient over-voltages. Consequently, 3.3 kV IGBTs [28] with $V_{igbt} = 1.8$ kV are used for the presented studies, and each cell switch consists of two parallel-connected IGBTs. The converters being compared are assumed to have a similar utilisation factor K_{uti} with respect to the semiconductors in each cell stack and DS, as described in (30). A higher value of utilization
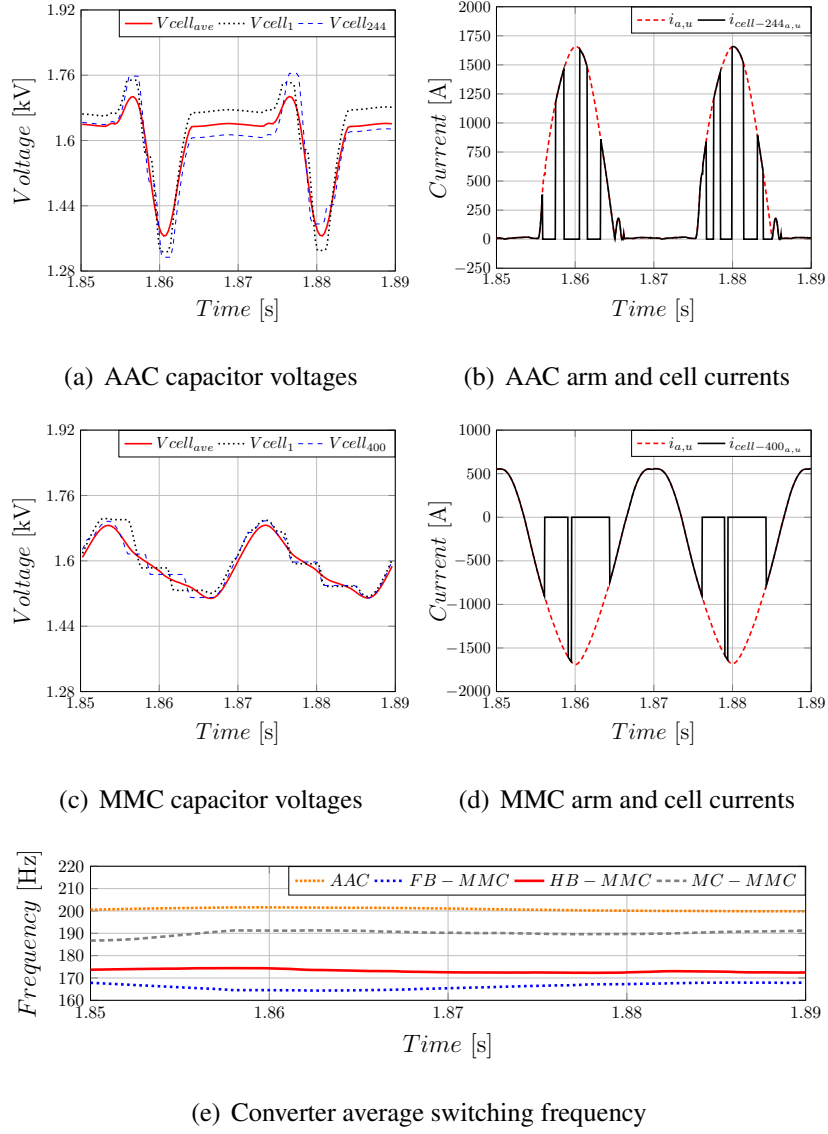
(a) AAC capacitor voltages

(b) AAC arm and cell currents

(c) MMC capacitor voltages

(d) MMC arm and cell currents

(e) Converter average switching frequency

Figure 10: The effect of tolerance band CBA.

factor K_{uti} describes the ratio between the required blocking voltage V_{chain} over the installed blocking voltage capability of the chainlink, results in lower conduction losses as the silicon is used more effectively.

$$K_{uti} = \frac{V_{chain}}{V_{igbt} \cdot n_s \cdot N_{cell}} \tag{30}$$

To facilitate continuous operation during cell failure, redundant cells should be included in each stack, so that the failed cell can be replaced during a maintenance cycle. As a result the MMC and AAC topologies are tested with 400 and 244 [25] cells per arm respectively, which includes approximately 11% extra cells in each case. Since in HVDC applications an AAC must contribute to AC voltage or reactive power control, its V_{stack} must be sized so that the modulation index can be controlled around the typical optimal operating point $(4/\pi)$, benefiting from the AC and DC voltage decoupling offered by the FB cells. By exploiting the aforementioned feature and the redundancy of FB cells, the converter AC voltage is increased to 500

$kV_{RMS_{LL}}$, in order to achieve flexible operation as the AAC varies its power exchange.

3.2. Passive components sizing

Correct sizing of passive components (such as cell capacitors and arm inductance) is critical for stable operation of AAC and MMC. Since cell capacitors in AAC and MMC experience low-frequency current, large cell capacitance will be required to ensure acceptable voltage ripple. To ensure stable operation over a wide modulation index, AAC energy storage capability is assumed to be similar to that of the MMC (i.e. 40 kJ/MW [29, 30].) The AAC arm inductance should be sufficient to enable the arm current to be transferred between arms during overlap, while providing a degree of current filtering [23]. In MMC the arm inductance (or accumulated DC side inductance [31]) can act as a filter for the circulating currents and to prolong current rise time in the event of a DC-side fault. An AAC requires a sizeable DC filter to attenuate 6th harmonic current and its multiples. However large filter capacitors may contribute to high inrush currents during DC-side faults. In the studies presented in this paper, in order to ensure good quality of DC current and voltage over a wide operating range, the AAC DC filter components are chosen to be $L_{DC_f} = 10~mH$ and $C_{DC_f} = 28.15~\mu F$.

4. Results

In order to validate the operation of the converters and their dedicated controllers, a point-to-point HVDC network has been utilised as depicted in Fig. 11. The network consists of two converters in a symmetric monopole configuration which are connected via DC cables (Wideband cable model). In each case study, Converters 1 and 2 are of the same type in order to minimise any interactions due to hardware and controller design. Table 3 presents the rating and design specifications for each converter topology.

Table 3: Rating and design specifications

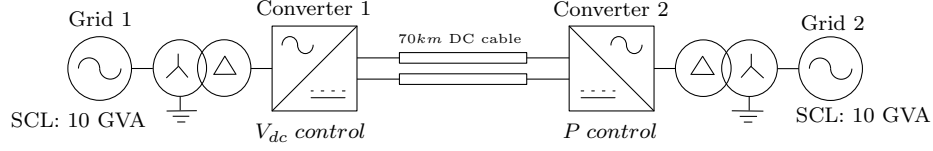|	AAC	MMC
S [MVA]	1045	1045
V_{DC} [kV]	640	640
Transformer reactance [%]	18	18
V_{chain}/V_{DS}[kV]	388/604	640/-
V_{grid}/V_{conv} [kV]	400/500	400/370
IGBT utilisation [%]	88.34	88.89
Arm inductance [mH]	11.14	65.36
Phase reactor [mH]	37.8	-
Cell capacitance [mF]	7.94	13.02

Figure 11: Simulated DC network.

4.1. Power quality results

Fig. 12 shows that both converters have high-quality AC waveforms with very low total harmonic distortion. However for future grids, which involve connections with multiple converters, DC power quality should also be considered. DC current I_{DC} determines the fluctuations in cable loading while DC voltage affects the design of cable insulation [32]. According to IEC-60287 (the standard applicable to the conditions of steady-state operation of cables at all alternating voltages), the DC current response of the cables is a function of the differential temperature variation between the conductor and ambient. Cable insulation requirements are calculated based on temperature variation, which is affected by low-frequency current ripple [33].

(a) AC converter current

(b) AC grid current

(c) DC currents

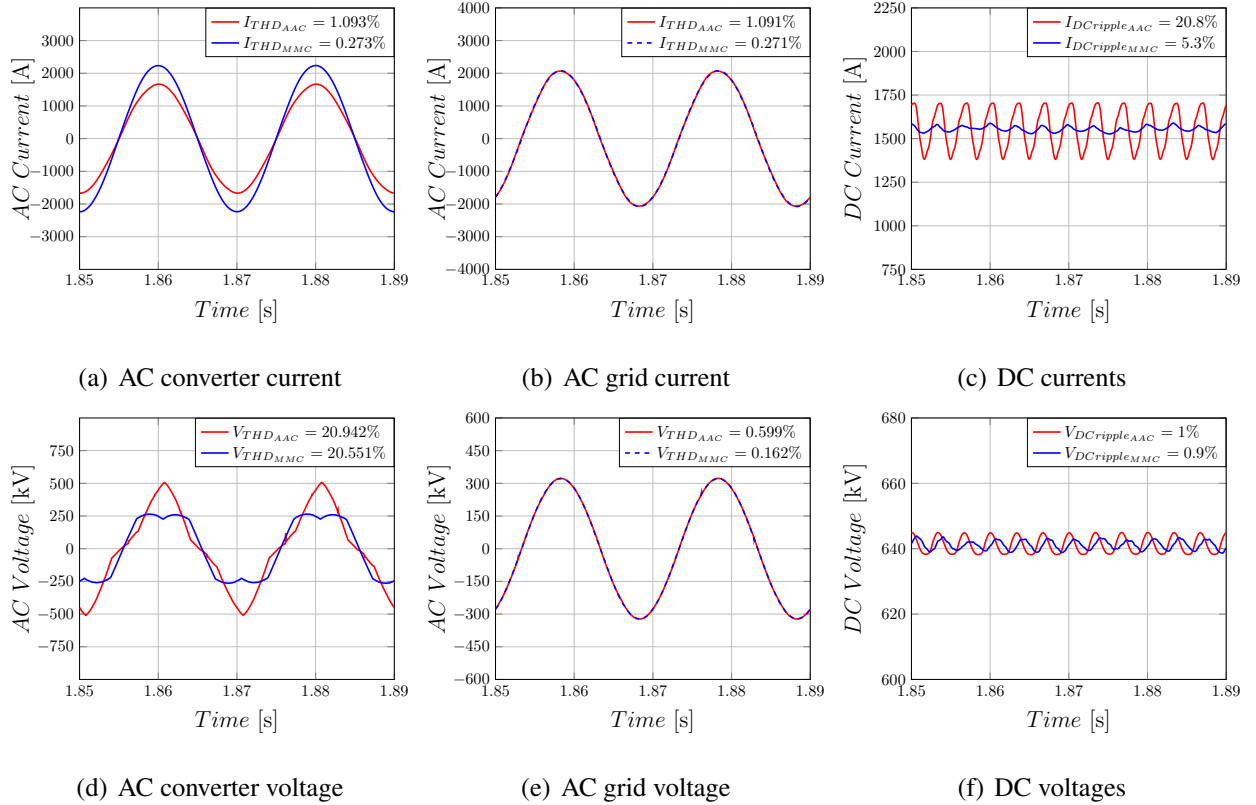(d) AC converter voltage

(e) AC grid voltage

(f) DC voltages

Figure 12: Converter voltage and current quality.

Consideration of DC current ripple is critical during the design process of DC cables, and potential integration of AAC into multi-terminal systems. From (17) and Fig. 12(e), it is evident that the DC current

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of the AAC exhibits high-magnitude of 6th harmonic ripple, which is due to the fundamental operating philosophy of AAC. Moreover, the quality of AAC and MMC DC waveforms is affected by the number of cells employed in each arm. A low number of cells per arm leads to higher voltage step transitions, and this causes larger voltage mismatches between the differential voltage $v_{j,diff}$ and DC voltage V_{DC}. By comparing the DC current and DC voltage ripple for a 40-cell and a 400-cell MMC (see Fig. 13), it can be deduced that the higher the number of cells, the lower the DC current and voltage ripple range. The voltage and current ripples shown in DC sides are primarily of 300 Hz, which are more likely due to the interactions between different controller that maintain the internal dynamics of the MMC. Typically these ripples are attenuated by installing DC filter at converter DC bus.

(a) DC current measurement   (b) 400-cell current frequency spectrum   (c) 40-cell current frequency spectrum

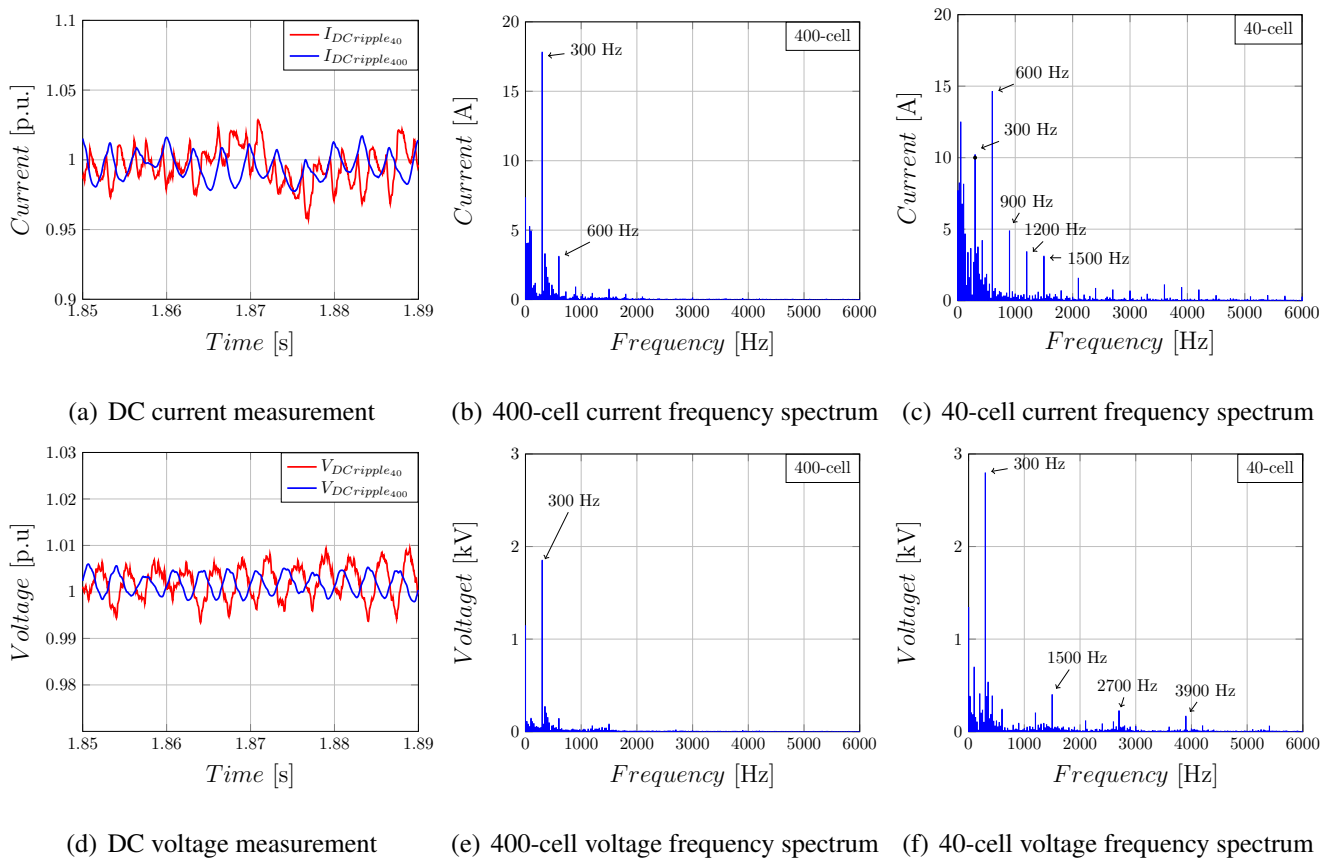(d) DC voltage measurement   (e) 400-cell voltage frequency spectrum   (f) 40-cell voltage frequency spectrum

Figure 13: DC voltage and current harmonics.

The plots for total harmonic distortions of the AC side waveforms (pre-filter line-to-line voltages and phase currents) in Fig. 14(a) and 14(b), and those of pole-to-pole DC voltage and DC link current ripples in Fig. 14(c) and 14(d), indicate the inferiority of the AAC compared to MMC in terms of AC and DC power quality. It should be noted that the AC and DC side power quality of the MMC with large and reduced number of cells, remains practically unchanged. This due to the fact that converters operate at rated active

power, with reactive power varying between rated capacitor and rated inductive. Nevertheless, the quality of the DC waveforms in AAC worsen as its reactive power output increases, while the DC voltage ripple of the AAC quickly exceeds the 3% in the under-excitation region of the P-Q chart. In contrast, the plot in Fig. 14(d) shows that the AAC exhibits acceptable level of DC current ripples, independent of its reactive power output.
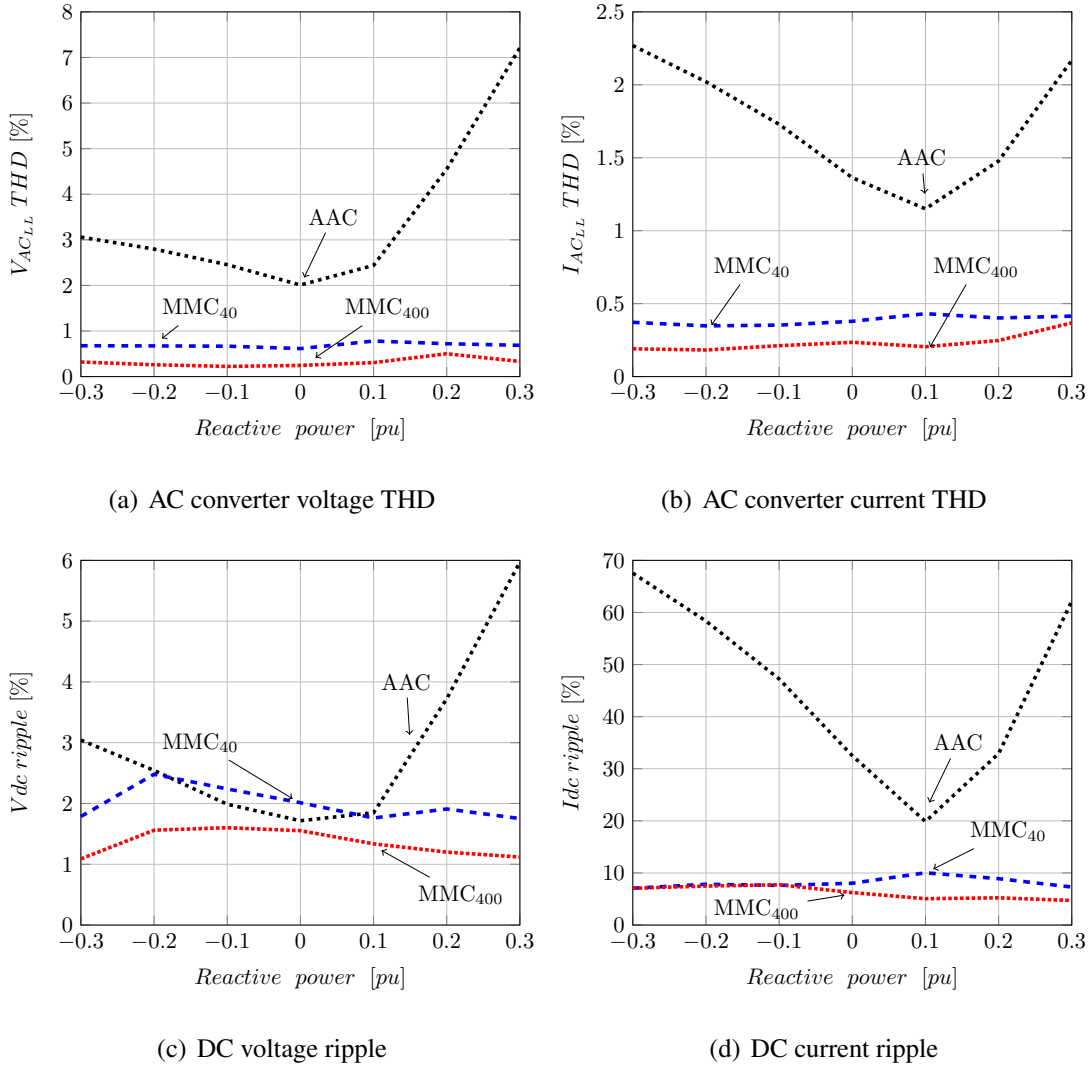

(a) AC converter voltage THD

(b) AC converter current THD

(c) DC voltage ripple

(d) DC current ripple

Figure 14: AC and DC power quality during variable Q for $P = 1\ p.u.$

The plots in Fig. 15 show the AAC DC current ripple when DC smoothing inductors with values of 10 mH, 50 mH, 100 mH and 300 mH are considered. Moreover, Fig. 15 includes the DC current ripple when an enhanced filter is used for 3rd, 6th and 12th harmonic attenuation, with lumped values $L_{DC_f} = 0.3\ mH$ and $C_{DC_f} = 147.7\ \mu F$, which is similar to the short overlap method employed in [34]. The 12.5% (100 mH) DC inductance at the DC link of the AAC, reduces the DC current ripple to 10%, which is similar to that achieved in the extended overlap method described in [35]. No reduction of great significance can

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be observed in the DC current ripple when increased inductance of 300 mH is used. DC inductance of 100 mH and 300 mH gives similar harmonic performance to the enhanced filter which included increased capacitance. It should be noted that, whilst the DC smoothing inductor reduces current ripple, it must be sized for rated DC current. Also, the increased capacitance of the enhanced filter will increase the amount of energy discharged during a DC fault.
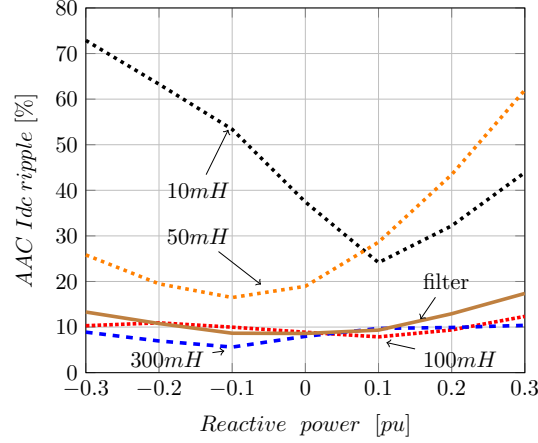

Figure 15: AAC I_{DC} ripple for various installed DC inductance and filters

4.2. Power loss results

Fig. 16 illustrates the power loss distribution on different converter cells. In an IGBT plus the anti-parallel diodes module, the IGBT part incurs more power loss than the diode part. Hence, an HB cell has lower power losses during rectification operation (i.e. power flow from the AC to the DC side which is assumed as positive power flow). This is because during rectification mode, the majority of conduction is through the lower diode. In FB cell, the loss distribution remains marginally similar during inverter and rectifier modes as shown in Fig. 16. This is due to the fact that the number of diodes and IGBTs in conduction path, remain the same in both inverter and rectifier mode. Detail loss distribution between individual switching devices of the FB and HB cells in MMC converter and between their diodes and IGBTs are shown in Fig.16(a) and Fig.16(b) respectively. Whilst the detailed loss distribution in the FB cell of the AAC exhibits different behaviour than that in MMC, despite the number of semiconductor devices in conduction path remain the same as in MMC, see in Fig.16(c).

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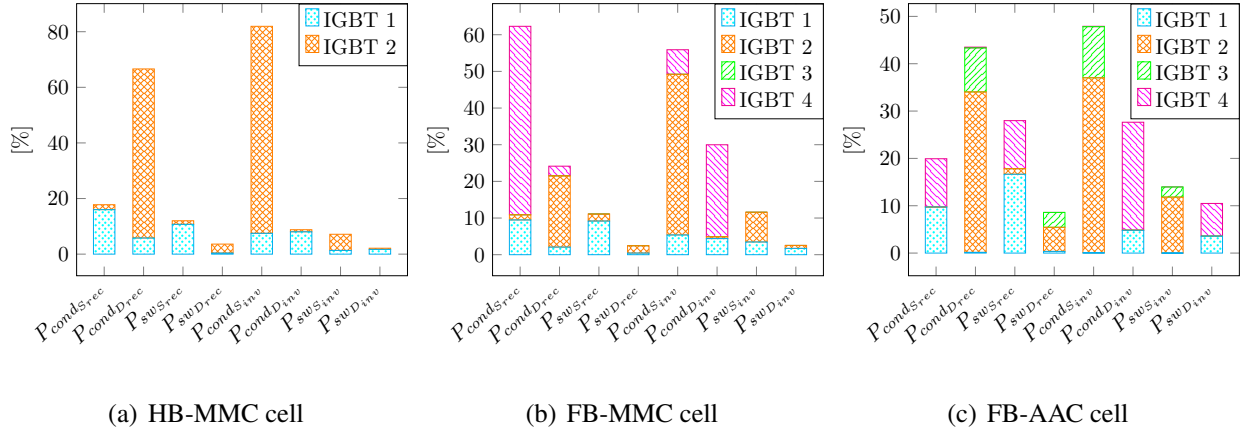(a) HB-MMC cell　　　　　(b) FB-MMC cell　　　　　(c) FB-AAC cell

Figure 16: Cell loss distribution over the total cell losses during inverter (inv) and rectification (rec) mode.

Table 4 illustrates the contribution of FB and HB cells, and DS to conduction and switching losses in each topology, (where applicable).

Table 4: Loss contributions (inverter mode: P=1 p.u., Q=0 p.u.)

[kW]	AAC	FB	HB	MC
Cond. FB	4477 (44%)	11592 (91%)	-	5794 (62%)
Cond. HB	-	-	4749 (81%)	2372 (26%)
Cond. DS	4058 (39%)	-	-	-
Sw. FB	1686 (17%)	1119 (9%)	-	595 (6%)
Sw. HB	-	-	1136 (19%)	593 (6%)
Sw. DS	0 (0%)	-	-	-

Among the MMC topologies, the switching losses remain the same as only two switches require to change their states (Tables 1 and 2), while the increased switching losses observed in the AAC case are due to operation in the over-modulation region where a cell's negative polarity voltage must be exploited. Fig. 17 shows that the total semiconductor losses when the HB-MMC operates in inverter mode are more than half that of the FB-MMC, as the majority of the conduction is through the IGBTs. However, such losses are lower in rectification mode, as the majority of conduction is through the diodes. The DS in the AAC are responsible for almost half of the conduction losses while they produce zero switching losses due to zero voltage switching.
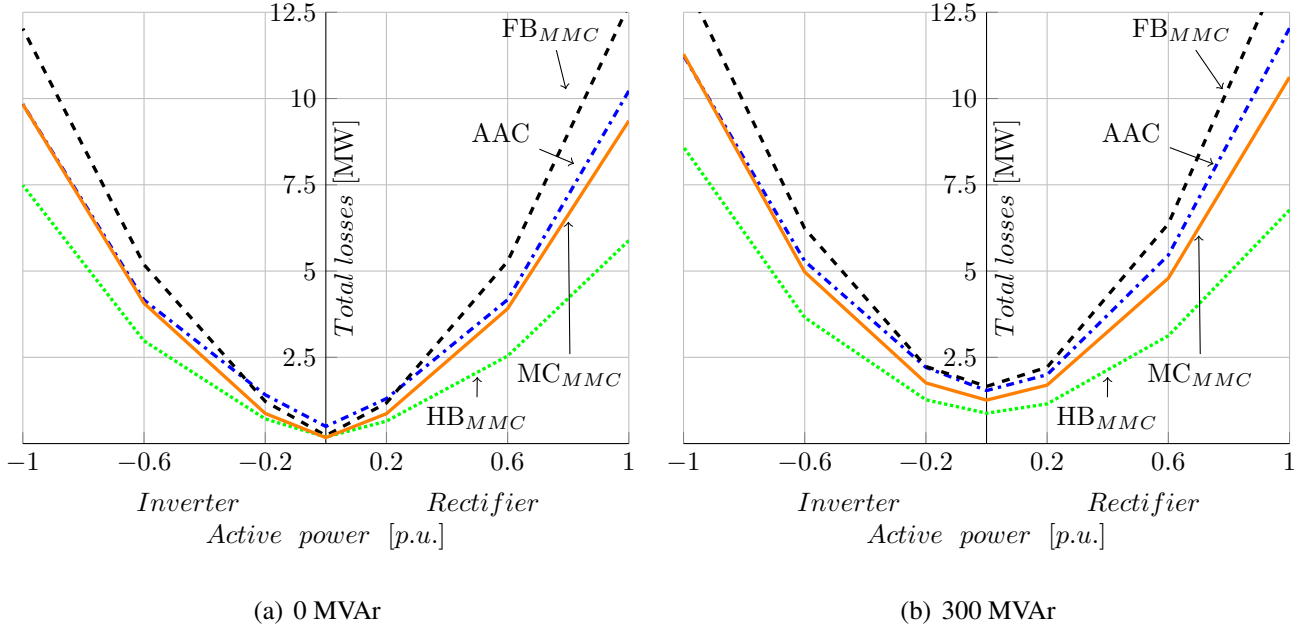
20

(a) 0 MVAr (b) 300 MVAr

Figure 17: Total semiconductor losses at various operation points for AAC and MMC.

Nonetheless, Table 5 shows that the reduction in the number of cells increases the switching losses, since a larger number of series-connected IGBTs switch for any given value of instantaneous current, while the conduction losses are only affected by the value of K_{uti}. Moreover, for a reduced number of levels, PWM is employed, which may lead to even higher switching losses as the cells switch according to the carrier switching frequency [1]. This could be prevented by adopting distributed control with phase shifted carriers, as introduced in [36].

Table 5: Effect of K_{uti} on MMC

N_{cell}	K_{uti}	$Cond.\ Losses[kW]$	$Sw.\ Losses[kW]$
20	0.99	4268	1246
100	0.89	4747	1222
400	0.89	4749	1136

5. Conclusions

This paper has presented a comprehensive comparison between AAC and MMC topologies, using high-fidelity converter models developed in the EMTP-RV simulation environment, and including all the necessary controllers for ensuring overall converter stability. The main conclusions drawn from these studies are summarised as follows.

- At unity power factor, the power quality at the DC side (DC current and voltage waveforms) of the AAC is marginally lower than that of the MMC, and that it deteriorates as power angle increases. This means that an HVDC link that employs an AAC requires substantial DC filtering to prevent penetration of the low-frequency harmonics from the converter into the DC side.

- The power quality at the AC side (AC current and voltage waveforms) of the AAC is marginally lower than that of the MMC. However, the rate of the deterioration of the AC power quality with power factor angle is much slower than that observed in the DC sides. This means smaller AC filters could be sufficient to meet the harmonic requirements at point of common coupling.

- The MMC with a reduced number of cells, exhibits lower DC-side power quality when compared to that with an increased number of cells. This implies that DC filters are necessary to prevent penetration of high-frequency harmonics from the converter into the DC link. There is only a slight difference in AC power quality between two configurations.

- The presented results revealed that in rectification mode, the AAC has higher losses than the MC-MMC, and the power losses of each converter converge as active power increases in inverter mode. Among modular designs, the FB-MMC and HB-MMC have been found to posses the highest and lowest losses respectively.

- The semiconductor power loss distributions between the individual switching devices of the FB cell in MMCs (FB-MMC, MC-MMC) and AACs, differ even when the operating conditions for both topologies are the same.

- The MMC with a reduced number of cells exhibits higher switching losses compared to an MMC with a higher number of cells. This is on the grounds that the switching losses will be greatly influenced by the number of IGBTs to be switched simultaneously during turn-on and turn-off, for a given arm current.

- Studies also demonstrated that at rated power in rectification mode, the HB-MMC semiconductor losses represents 50% of those of the FB-MMC, while in inverter mode they increase to nearly 60% of those of the FB-MMC.

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