

# Design, Fabrication, and Application of GaN-Based Micro-LED Arrays With Individual Addressing by N-Electrodes

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**Abstract:** We demonstrate the development, performance, and application of a GaN-based micro-light emitting diode ( $\mu$ LED) array sharing a common p-electrode (anode), and with individually addressable n-electrodes (cathodes). Compared to conventional GaN-based LED arrays, this array design employs a reversed structure of common and individual electrodes, which makes it innovative and compatible with n-type metal-oxide-semiconductor (NMOS) transistor-based drivers for faster modulation. Excellent performance characteristics are illustrated by an example array emitting at 450 nm. At a current density of 17.7 kA/cm<sup>2</sup> in direct-current operation, the optical power and small signal electrical-to-optical modulation bandwidth of a single  $\mu$ LED element with 24  $\mu$ m diameter are over 2.0 mW and 440 MHz, respectively. The optimized fabrication process also ensures a high yield of working  $\mu$ LED elements per array and excellent element-to-element uniformity of electrical/optical characteristics. Results on visible light communication are presented as an application of an array integrated with an NMOS driver. Data transmission at several hundred Mb/s without bit error is achieved for single- and multiple- $\mu$ LED-element operations, under an ON-OFF-keying modulation scheme. Transmission of stepped sawtooth waveforms is also demonstrated to confirm that the  $\mu$ LED elements can transmit discrete multilevel signals.

**Index Terms:** GaN, micro-light emitting diode array, Individual addressing by n-electrodes, visible light communication.

## 1. Introduction

GaN-Based light emitting diodes (LEDs), which have achieved great importance in conventional chip formats as indicators and in solid-state lighting, can also be fabricated into arrays of micro-scale LED elements with lateral dimensions of less than  $100\ \mu\text{m}$  [1]. The operating current densities and optical power densities of these micro-LED ( $\mu\text{LED}$ ) elements are significantly higher than for conventional broad-area LED devices [2] and the devices can be fabricated in high-density 1D and 2D arrays. Thanks to these properties,  $\mu\text{LED}$  arrays are attractive for applications including micro-displays ( $\mu\text{displays}$ ) [3], projection [4], optoelectronic tweezers [5] and maskless photolithography [6]. Furthermore, the high operating current density leads to a short differential carrier lifetime [7], thus making  $\mu\text{LED}$  arrays promising for high-speed visible light communications (VLC) both in free space and in polymer optical fiber [8]. VLC using LEDs offers the possibility of employing general illumination devices for data transmission, and many other advantages including license-free operation, high spatial diversity and innate security [9]. In our recent work, we demonstrated that single GaN-based  $\mu\text{LED}$  elements have typical electrical-to-optical (E-O) modulation bandwidths in the range of 100 to 400 MHz [7], and in some cases up to 800 MHz [10]. Error-free data transmission up to 1.7 Gbps [10] and 7.9 Gbps [11] has been achieved using on-off keying (OOK) and orthogonal frequency division multiplexing (OFDM), respectively, applied to such single  $\mu\text{LED}$  elements. By operating a  $\mu\text{LED}$  array in a ganged (parallel-addressed) fashion, it is possible to obtain a higher signal-to-noise ratio, and thus longer data-transmission distance, while retaining a fast data rate [12].

In recent years, with the maturation of fabrication techniques, different addressing schemes for  $\mu\text{LED}$  arrays have been demonstrated [13]–[15]. An active driving scheme can be accomplished by integrating  $\mu\text{LED}$  arrays with complementary metal-oxide-semiconductor (CMOS) active matrix drivers, using flip-chip bonding [3], [7], [15]. Compared with the alternative matrix addressing scheme, the flexible control of individual elements is of great benefit for  $\mu$  display and VLC applications. However, in the conventional embodiment, there are also some drawbacks. In a conventional  $\mu\text{LED}$  array, elements share a common n-electrode (cathode) with individually addressable p-electrodes (anodes). This configuration is shown in Fig. 1(a), and it is generally used because standard GaN LED epitaxial structures invariably have the p-side of the junction on top, which is necessitated by the relatively low conductivity of p-doped GaN [16], in addition to several growth issues.

In the configuration shown in Fig. 1(a), the n-type GaN layer functions as a shared conductive path for all  $\mu\text{LED}$  elements in the array. Therefore, different distances between the common n-electrode and the respective  $\mu\text{LED}$  elements lead to different series-resistance contributions from the n-type GaN. These differing series resistances result in non-uniform operating currents at the same applied voltage for each  $\mu\text{LED}$  element and, thus, poor optical element-to-element uniformity [14] and high crosstalk [17], which are undesirable in practical applications. Concerning the driver choice, this configuration also restricts the CMOS circuitry to designs based on p-type MOS (PMOS) transistors. It is well known that the mobility of majority carriers (holes) in PMOS transistors ( $\approx 450\ \text{cm}^2/(\text{V}\cdot\text{s})$ ) in Si doped at  $10^{15}\ \text{cm}^{-3}$  is significantly lower than that of majority carriers (electrons) in NMOS transistors ( $\approx 1500\ \text{cm}^2/(\text{V}\cdot\text{s})$ ) in Si doped at  $10^{15}\ \text{cm}^{-3}$  [16]. Thus, the operating speed of PMOS transistors is slower than comparable NMOS transistors. Additionally, in order to achieve the same impedance, a larger size is required for PMOS transistors. This, in turn, leads to a larger area requirement on the chip and also a larger capacitance, thus further reducing the operating speed of PMOS transistors [18]. These factors are highly disadvantageous for  $\mu\text{LED}$  array applications, since the achievable density of driver cells on a chip, and the modulation speed supplied from the CMOS, are both limited. Following these considerations, it is advantageous if the series resistance difference between  $\mu\text{LED}$  elements can be minimized and, simultaneously, NMOS drivers used.

In this work, we demonstrate an innovative GaN-based  $\mu\text{LED}$  array configuration combining a common p-electrode with individually addressable n-electrodes. Compared with a conventional  $\mu\text{LED}$  array, this design employs a reversed common and individual electrode structure, which minimises the series-resistance differences from conductive paths and provides compatibility with NMOS transistor-based CMOS drivers. We have furthermore developed the fabrication process and describe how the various challenges in the fabrication of GaN-based LED arrays with individual

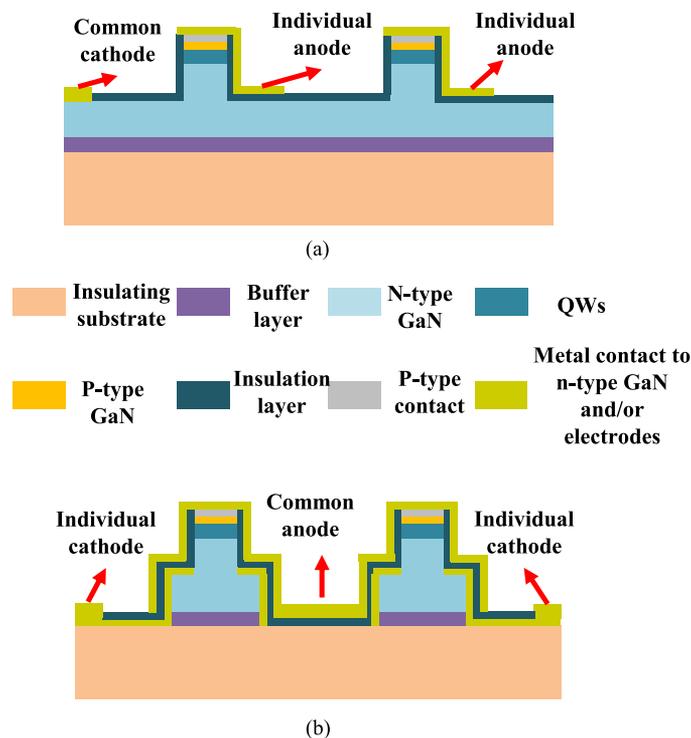


Fig. 1. Simplified cross-sectional schematic configurations of a conventional  $\mu$ LED array (a) and the innovative variant developed in this work (b). Dimensions are not to scale.

n-electrodes can be addressed. We have improved the performance, the proportion of working  $\mu$ LED elements per array (referred to as  $\mu$ LED element yield from here on) and the uniformity of electrical/optical characteristics in comparison with our earlier work [7], [15]. Example arrays fabricated from a commercial blue LED wafer on sapphire show performance characteristics confirming the potential of the approach. At 450 nm, over 2.0 mW optical power and 440 MHz E-O modulation bandwidth are achieved for a single  $\mu$ LED element of 24  $\mu\text{m}$  diameter at 17.7  $\text{kA}/\text{cm}^2$  operating current density.

We also demonstrate the integration of this array with a custom CMOS driver based on NMOS transistors. This driver is capable of operating the LEDs with various modulation schemes. While many current VLC demonstrations rely on the usage of arbitrary waveform generators, the integrated system here is a stepping stone towards more practical implementations. To demonstrate its basic functionality, the responses from single- and/or multiple- $\mu$ LED elements under an on-off-keying (OOK) data transmission scheme are presented. Open eye-diagrams are recorded at several hundred Mbps. Transmission of stepped sawtooth waveforms is also studied to illustrate the capability of this integrated system to transmit optical signals with discretely varying intensity.

## 2. Experimental Details

The  $\mu$ LED arrays were fabricated from blue III-nitride LED wafers grown on c-plane (0001) sapphire with periodically patterned surfaces. Light was extracted through the sapphire, the backside of which was polished before device fabrication. The LED epitaxial structure consists of a 3.4  $\mu\text{m}$ -thick undoped GaN buffer layer, a 2.6  $\mu\text{m}$ -thick n-type GaN layer, eleven periods of InGaN (2.8 nm)/GaN (13.5 nm) quantum wells (QWs) emitting at 450 nm, a 30 nm-thick p-type AlGaIn electron blocking layer and a 160 nm-thick p-type GaN topmost layer. The  $\mu$ LED arrays discussed in detail here contain a  $6 \times 6$  layout of  $\mu$ LED elements, each with a diameter of 24  $\mu\text{m}$  (452.2  $\mu\text{m}^2$  emitting area),

on a 300  $\mu\text{m}$  center-to-center pitch. Variants on this design were also fabricated, and are discussed further in connection with optimization of processing in Section 3-B.

As mentioned above, each  $\mu\text{LED}$  element in the array developed in this work is individually addressed by its own n-electrode with a shared p-electrode. Fig. 1 illustrates the simplified schematic configurations of the conventional  $\mu\text{LED}$  array, (a), and the one developed in this work, (b). The  $\mu\text{LED}$  elements in the conventional array are defined by element etching finished at the n-type GaN layer. By this means, all the  $\mu\text{LED}$  elements in the array are connected via n-type GaN and, thus, share a common n-electrode, while having individually addressable p-electrodes. In order to realize a  $\mu\text{LED}$  array with individually addressed n-electrodes, each  $\mu\text{LED}$  element must be fully isolated from both p- and n-type GaN layers as shown Fig. 1(b). To achieve this configuration, two steps of  $\text{Cl}_2$ -based plasma etching of GaN are involved. Fig. 2 shows the main steps. Firstly, a  $6 \times 6$  array of GaN mesas, in a square shape with sides of 130  $\mu\text{m}$ , is etched down to the sapphire substrate by inductively coupled plasma (ICP) etching [see Fig. 2(a)]. Then, a disk-shaped  $\mu\text{LED}$  element with 24  $\mu\text{m}$  diameter is created at the centre of each mesa through a second ICP etch which stops at the n-type GaN layer [see Fig. 2(b)]. This two-step etching not only enables the isolation of  $\mu\text{LED}$  elements from both p- and n-type GaN layers, but also guarantees the same contact area of metal contacts to n-type GaN for each  $\mu\text{LED}$  element. Although the square mesas have a separation of 170  $\mu\text{m}$  in the design discussed in detail, these principles have also been applied to arrays in which the mesas are separated by a gap of only 6  $\mu\text{m}$ .

After the etching steps described, a 100 nm Pd metal layer is evaporated on the p-type GaN surface and thermally annealed in a  $\text{N}_2$  ambient at 300  $^\circ\text{C}$  to form a quasi-ohmic contact to p-type GaN. The metallization on the isolated n-type GaN mesa is realized by sputtering a Ti/Au (50/200 nm) metal bilayer and a lift-off process. This bilayer is also patterned to make metal tracks from the n-type GaN mesas to individually address every  $\mu\text{LED}$  element [see Fig. 2(c)]. Specific lift-off resists used include Dow Megaposit SPR220 4.5 (positive-working) and Micro Resist Technology ma-N 1420 (negative-working). Solvent-based treatments used to remove photoresist residues in non-optimised processes involved 1-methyl-2-pyrrolidone, with heating up to 120  $^\circ\text{C}$  or ultrasonication, in addition to methanol and acetone. Then, in our optimised process, the array is cleaned by an  $\text{O}_2$ -based plasma at 200  $^\circ\text{C}$  in a plasma asher (Matrix 105 system). We have found plasma ashing is an especially critical step to optimise the  $\mu\text{LED}$  element yield and uniformity of electrical/optical characteristics. These improvements will be discussed in more detail in Section 3-B.

Following the plasma clean, a 300 nm-thick  $\text{SiO}_2$  layer is deposited by plasma enhanced chemical vapor deposition. After selectively removing  $\text{SiO}_2$  on top of each  $\mu\text{LED}$  element, another Ti/Au metal bilayer is deposited to interconnect  $\mu\text{LED}$  elements forming a shared p-electrode, as illustrated by the shaded overlays (with dashed red outlines) in Fig. 2(d). Fig. 2(e) shows a schematic layout of the whole array to emphasise the electrode configuration. Although different distances between electrodes and target  $\mu\text{LED}$  elements still exist, it is important to note that the conductive paths are formed by Ti/Au metal bilayers, rather than the n-type GaN as in the conventional configuration. Thus, the resulting series-resistance differences are minimised, owing to the significantly lower sheet resistivity of the metal layer.

The custom CMOS driver used in this work is based on NMOS transistors, and contains four independent current-steering digital-to-analog converter (DAC) driver channels with 8-bit resolution. Each driver channel is designed to sink a full-scale current up to 255 mA, and operates at an electrical-to-electrical modulation bandwidth of 250 MHz. More detailed information can be found in [19]. In order to integrate the  $\mu\text{LED}$  array with the CMOS driver, the  $\mu\text{LED}$  array is firstly wire-bonded to a commercial ceramic package, which is soldered to a daughter card. The daughter card and motherboard are connected through four high-speed connectors. The motherboard has 40 SubMiniature Version A (SMA) connectors around the edge. Four of these SMA connectors are used for supplying power, and the other connectors are used for connecting the  $\mu\text{LED}$  elements to the CMOS driver. A photograph of the assembled system is shown in Fig. 3.

Before integrating the  $\mu\text{LED}$  array with the CMOS driver, its electrical, optical and modulation performance characteristics were measured. The quoted yields of working  $\mu\text{LED}$  elements are based on measurements of several tens of individual arrays. By placing a Si photodetector in close

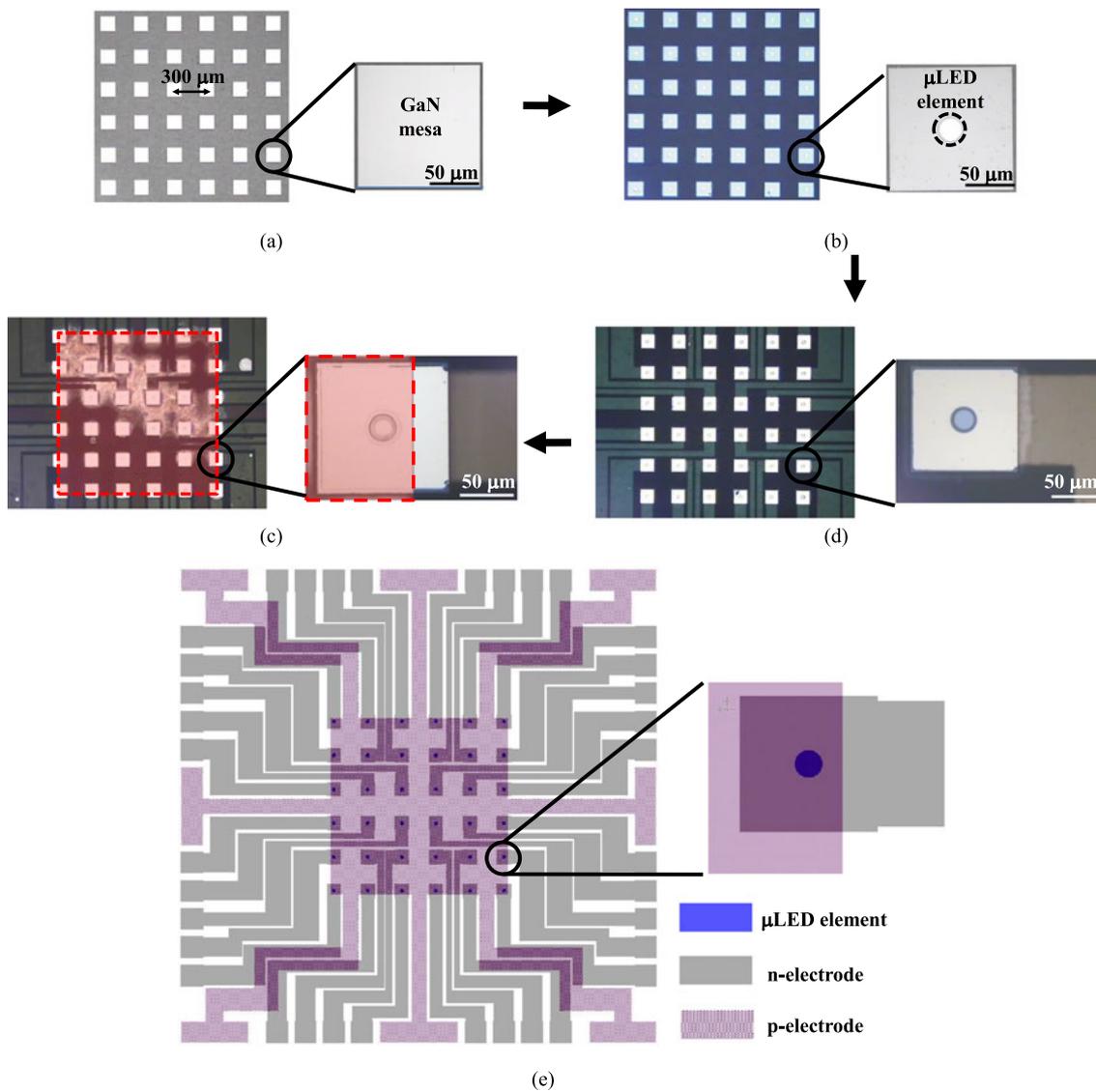


Fig. 2. Plan view optical images of the main steps in the fabrication process of  $\mu$ LED array with individually addressable n-electrodes: (a) GaN mesa etching down to the sapphire substrate; (b)  $\mu$ LED element etching finished at the n-type GaN layer; (c) metal deposition for individually addressable n-electrodes; (d) metal deposition for a shared p-electrode. High-magnification images for a typical  $\mu$ LED element are also shown. Part (e) shows a schematic layout of the whole  $\mu$ LED array.

proximity to the polished sapphire substrate of the  $\mu$ LED array, the current versus voltage (I-V) and optical power versus current (L-I) characteristics were measured at the same time, through scanning each data point under direct-current (DC) conditions. The E-O modulation bandwidth of  $\mu$ LED elements was measured following the same method described in [7] and [15]. A small-signal modulation, of fixed amplitude, from an HP8753ES network analyser was combined with a DC bias using a bias-tee, and applied to a representative  $\mu$ LED element using a high-speed probe. The modulated light output from the  $\mu$ LED element was collected by a 1.4 GHz bandwidth photoreceiver, and a network analyzer used to measure the frequency response.

After the initial characterization outlined, the  $\mu$ LED array was integrated with the CMOS driver to demonstrate its compatibility and application in VLC with integrated control. Arbitrary waveforms were sent to the  $\mu$ LED elements through the CMOS drivers. These waveforms were generated

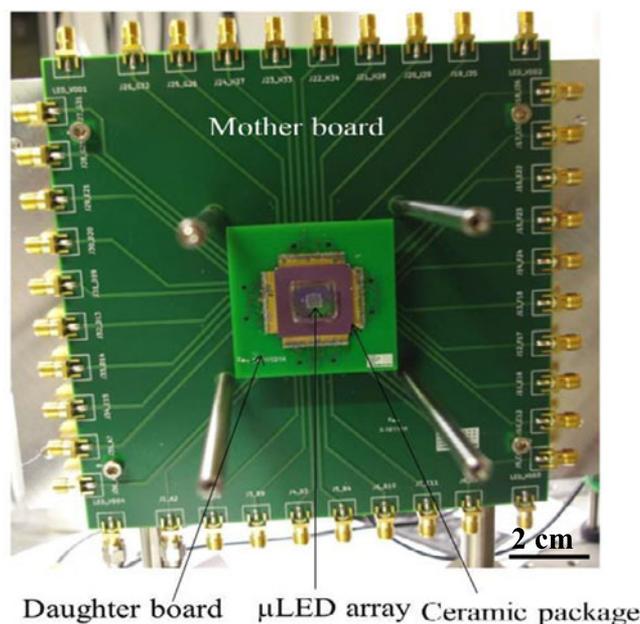


Fig. 3. Photograph of the system integrating the individual-n-addressable  $\mu$ LED array with the NMOS-based CMOS driver.

through a Matlab<sup>TM</sup> interface, and downloaded onto the field-programmable gate array. The signal levels correspond to integers ranging from 0–255 on an 8-bit DAC, and waveforms were created as a  $1 \times X$  array. The corresponding output current of the CMOS drivers was proportional to the received integer value for each sample period. The symbol-rate was determined by modifying the clock speed of the CMOS driver, which was also controllable through the Matlab interface. The LED power supply was set to 9 V and limited to 70 mA per active  $\mu$ LED element. The output responses were collected by a Hamamatsu C5658 avalanche photodiode (APD) with 1 GHz bandwidth. The distance between the  $\mu$ LED array and APD was around 50 cm. All measurements were performed at room temperature.

### 3. Results and Discussion

#### 3.1 Performance of a Single $\mu$ LED Element

Fig. 4(a) illustrates the typical I-V and L-I characteristics of a single  $\mu$ LED element in an array. This  $\mu$ LED element can be operated at a current up to 80 mA, and is able to produce an optical power over 2 mW before thermal rollover, which corresponds to current and optical power densities of 17.7 kA/cm<sup>2</sup> and 442.3 W/cm<sup>2</sup>, respectively. This high operating current density leads to a shorter differential carrier lifetime and, thus, increases the modulation bandwidth of the  $\mu$ LED element [7]. As shown in Fig. 4(b), this  $\mu$ LED element has an E-O modulation bandwidth in excess of 440 MHz, which is over 12 times higher than the corresponding value for typical commercial LEDs [20]. Compared with an individual  $\mu$ LED element from the conventional individually p-addressable array reported in our early work [7], [15], all the performance characteristics show a significant improvement, which is in part attributed to the Pd metal contact to p-type GaN employed here. We have found that Pd metal contacts to p-type GaN have lower specific contact resistivity and higher reflectivity than the metal contact scheme used in our previous work: annealed Ni/Au, capped with Ti/Au as a reflector. These properties reduce the series resistance of a  $\mu$ LED element, and enhance the light extraction efficiency (LEE) resulting in better electrical, optical and modulation performance. Another significant point of comparison with a  $\mu$ LED element in a conventional array

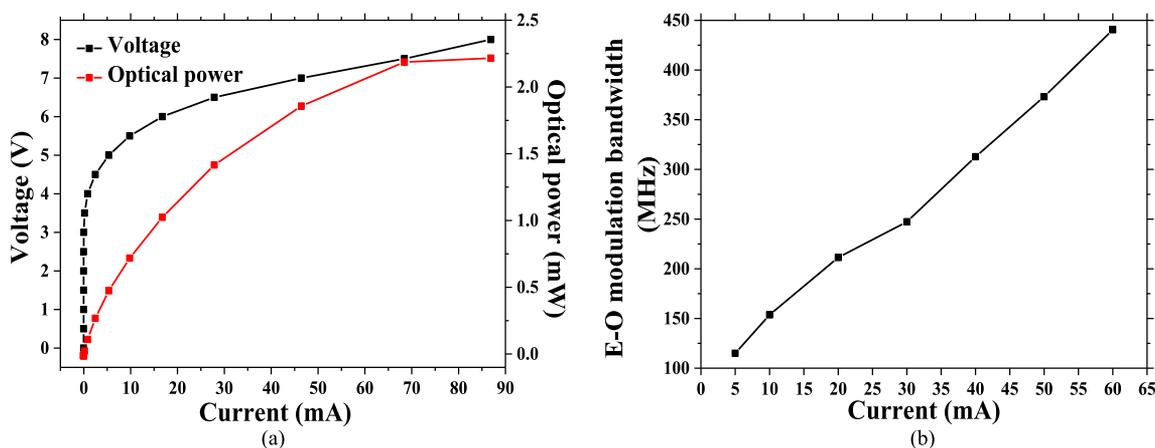


Fig. 4. (a) I-V and L-I characteristics of a single  $\mu$ LED element in the array; (b) E-O modulation bandwidth characteristic of the same  $\mu$ LED element. Lines connecting data points are to guide the eye only.

is that the area of metal contact to n-type GaN for each  $\mu$ LED element is limited by the size of the GaN mesa etched down to the sapphire substrate, as discussed in Section 2. This limited contact area (less than  $1.7 \times 10^{-4} \text{ cm}^2$  per element) leads to the higher series-resistance contributed from the metal contact to n-type GaN, which should degrade the I-V characteristic for the  $\mu$ LED element in this innovative array such as higher turn-on voltage. Nevertheless, we do not observe the remarkable degradation on the I-V characteristic and the low contact resistivity of the Ti/Au metal contact to n-type GaN ( $\sim 3.7 \times 10^{-5} \text{ cm}^2$ ) [21] rationalizes this observation. This observation further indicates that the electrical performance of a GaN-based  $\mu$ LED element is dominated by the series-resistance from the metal-contact to p-type GaN which also motivates our work on Pd metal contact to p-type GaN as discussed in early part.

### 3.2 $\mu$ LED Element Yield and Uniformity of Electrical/Optical Characteristics

In addition to the performance characteristics of single  $\mu$ LED elements, the  $\mu$ LED element yield and the uniformity of electrical/optical characteristics across a full array are important factors for applications. As explained above, a deep etch down to the sapphire substrate is necessary to define separate GaN mesas within which each  $\mu$ LED element is fabricated. This step leads to a relatively deep gap, or trench, between adjacent GaN mesas (around  $6 \mu\text{m}$  in depth for the epitaxial structure employed), which has no counterpart in conventional  $\mu$ LED array process flows. We have found this deep gap has a great influence on the  $\mu$ LED element yield, and reference to Fig. 1(b) will show how dielectric and metal layers must be deposited over the exposed substrate in this region. Initial versions of the  $6 \times 6 \mu$ LED arrays were fabricated using conventional stripping solvents to remove lift-off resists, and the specific materials tried were detailed in Section 2. With  $170 \mu\text{m}$  gaps between mesas, the  $\mu$ LED element yield in the array was around 90%. However, when the gap width decreased to  $6 \mu\text{m}$  in a similar array design, the  $\mu$ LED element yield dropped to around 67%. The cause of low yields was the incomplete removal of photoresist residues, as illustrated by a typical scanning electron microscope (SEM) image shown in Fig. 5. These photoresist residues lead to degradation of the  $\text{SiO}_2$  layer deposited in the following step and, consequently, short-circuiting of  $\mu$ LED elements and low element yield. The extent of contamination was also consistently greater in the small-gap case. Although our survey of different types of lift-off resist and cleaning solvents could not be exhaustive, we consider this issue and the solution now discussed to be of general applicability. The optimized process introduced an  $\text{O}_2$ -based plasma ashing step to replace the solvent-based step for photoresist stripping before the  $\text{SiO}_2$  deposition. Such low-damage oxidizing plasma processing is known to be effective for full removal

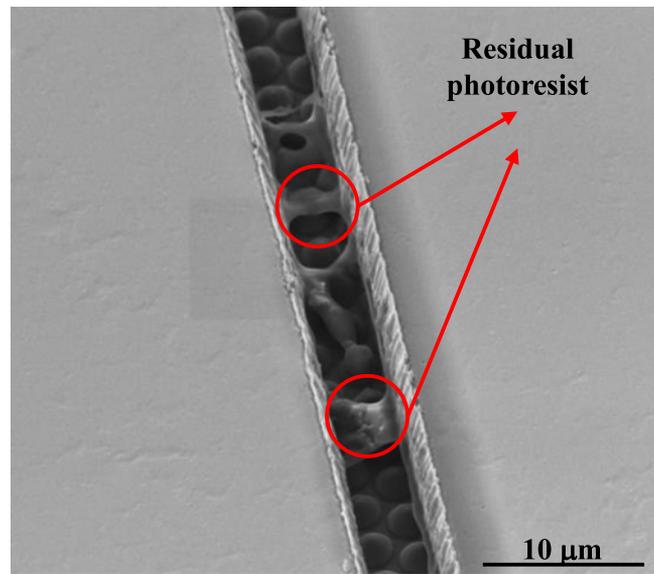


Fig. 5. Oblique-view SEM image of photoresist residues in a deep narrow gap ( $6\ \mu\text{m}$  in both width and depth) between two adjacent GaN mesas. Examples of photoresist residues are highlighted by red circles. The lenticular features visible in the gap are from the periodic surface texturing (patterned sapphire substrate, PSS) applied to the sapphire before the growth of the LED structure. Note also that the GaN etch steps leave near-vertical sidewalls.

of photoresist residues in many other types of semiconductor device processing. We are not aware of a previous application to analogous GaN device process flows, but the chemical stability of GaN and its relative resistance to oxidation [22] are possibly significant for the viability of our optimised process flow [23], [24]. With the introduction of this ashing step, the  $\mu\text{LED}$  element yield in the  $\mu\text{LED}$  array with  $170\text{-}\mu\text{m}$  mesa separation increased to 100% of arrays tested. Furthermore, the yield improvement is more significant for  $\mu\text{LED}$  arrays with a narrower gap between mesas. For example, the  $\mu\text{LED}$  element yield in arrays with a gap width of  $6\ \mu\text{m}$  increased from 67% to over 95%.

As a separate issue to the improvement in  $\mu\text{LED}$  element yield, we find the ashing step can also improve the uniformity of electrical and optical characteristics. Because the custom CMOS drivers are designed for operation with current setpoints, we compared the applied voltage and optical output power of selected  $\mu\text{LED}$  elements when driven at the same operating current within the same array. Fig. 6(a) illustrates the applied voltage and optical power at a fixed current of 60 mA (corresponding to a current density of  $13.3\ \text{kA}/\text{cm}^2$ ) measured for 5 randomly selected  $\mu\text{LED}$  elements in an array fabricated without  $\text{O}_2$  plasma ashing. The applied voltage and output power variations are within 18.1% and 6.4%, respectively [Variation is defined as  $(V_{\text{max}} - V_{\text{min}})/V_{\text{min}} \times 100\%$  for voltage and equivalently for power]. Since the optical power of a  $\mu\text{LED}$  element at a fixed current is proportionate to LEE, which is strongly influenced by the reflectivity of the Pd-based metal contact to p-type GaN, the degree of uniformity confirms consistency in the optical properties of these contacts. The larger variations in applied voltage correlate with the different lengths of Ti/Au interconnection track to different elements. Fig. 6(b) shows comparable results for elements in an array processed with the plasma ashing step. The applied voltage and optical power variations at 60 mA are reduced to 6.8% and 3.5% respectively. To ensure a fair comparison, the positions of the five elements measured for this figure are exactly same as those measured for Fig. 6(a). The same pattern of variation in applied voltage, correlating with the length of interconnect track, can thus be seen. The applied voltage variation could also be further reduced by increasing the thickness of Ti/Au metal bilayer.

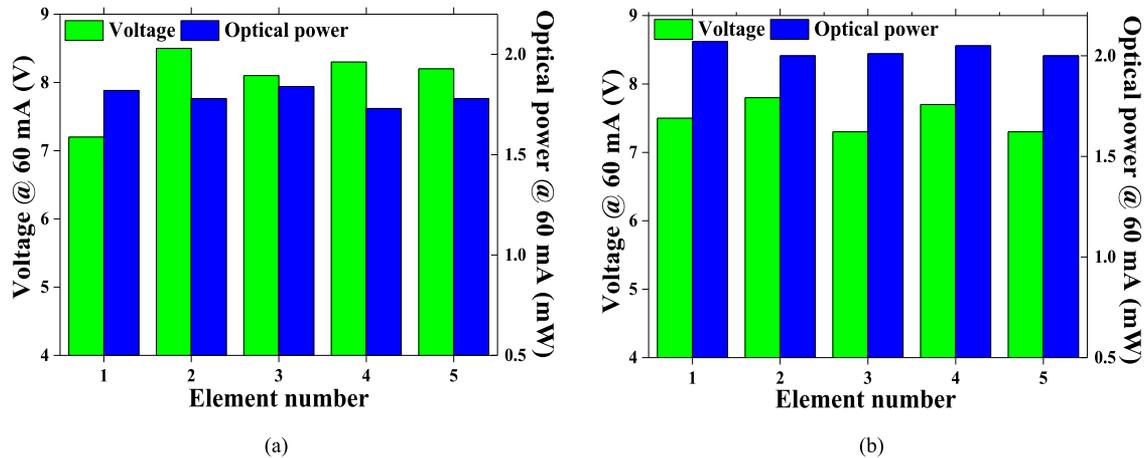


Fig. 6. Electrical and optical uniformities of 5 selected  $\mu$ LED elements of  $\mu$ LED arrays (a) without the ashing step or (b) with the ashing step. The positions of selected elements are exactly the same in both arrays.

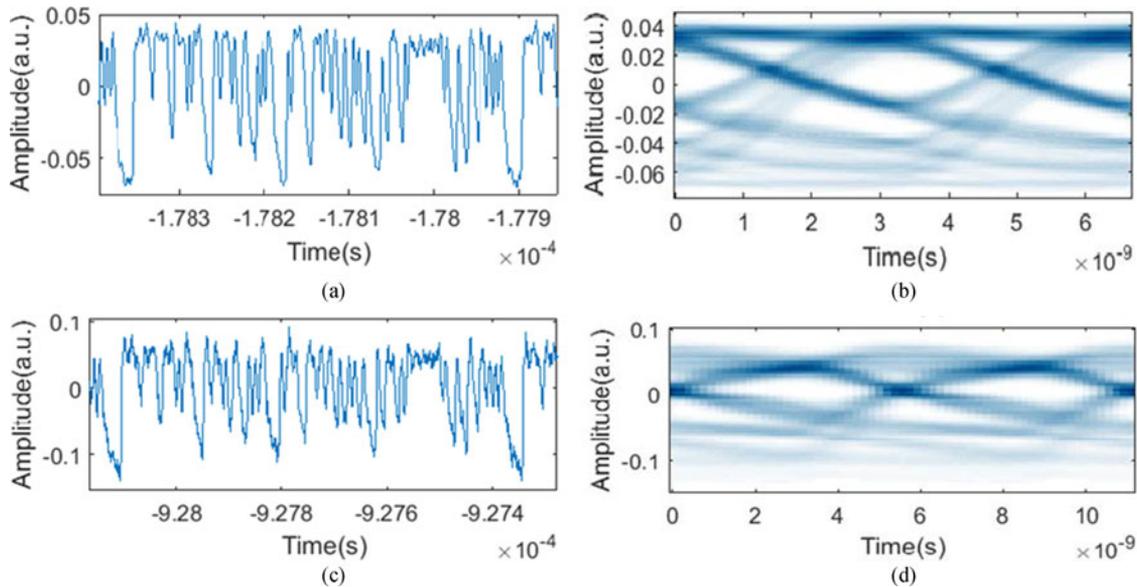


Fig. 7. Received waveforms and resultant eye-diagram for a single  $\mu$ LED element operated at 300 MHz [(a) and (b)] and four  $\mu$ LED elements operated at 180 MHz [(c) and (d)].

### 3.3 VLC Application of the $\mu$ LED Array Integrated With NMOS Transistor-Based CMOS Driver

The  $\mu$ LED array was integrated with the custom NMOS transistor-based CMOS driver following the scheme described in Section 2. For the purpose of illustrating the VLC application, a pseudo-random OOK data stream was generated and sent to the  $\mu$ LED elements through the CMOS driver. This was done for 1 and 4  $\mu$ LED elements each operating synchronously with the same waveform but driven by independent DACs. Pseudo random data sequences were generated and transmitted between 10 and 475 Mbps. The received waveforms and resultant eye-diagrams are shown in Fig. 7. As shown in Fig. 7(a) and (b), a single- $\mu$ LED-element could be operated at 300 Mbps without observable bit error. When four  $\mu$ LED elements were operated together, a similar eye diagram was observed at a lower bitrate of 180 Mbps, as shown in Fig. 7(c) and (d). This drop is

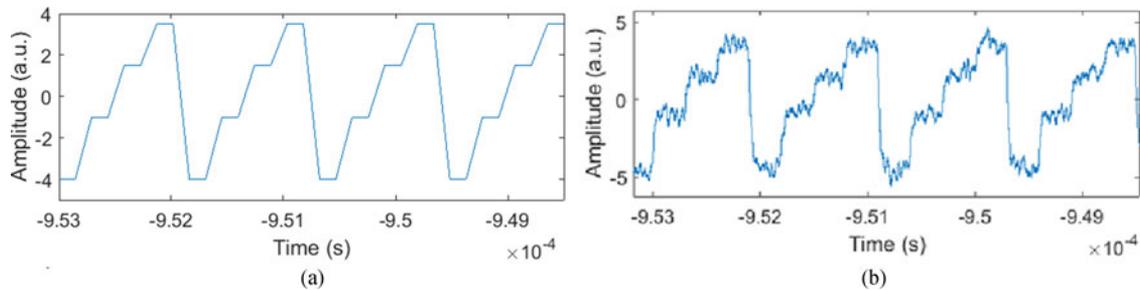


Fig. 8. Programmed stepped sawtooth input waveform with four distinct steps (a) and corresponded optical output waveform from a single  $\mu$ LED element (b). The  $\mu$ LED element was operated at 10 MHz.

likely due to heating effects as the four elements operated in close proximity to each other. It should be noted that the present array has no heat sink, so this effect has the potential to be alleviated. These results demonstrate single- and multi-element operation of the array at high bitrates. The apparent time jitter within the eye-diagram is partially due to the reset time of the DACs after each repetition of the OOK waveform.

As an alternative to simple OOK modulation, the custom CMOS driver is also capable of altering the modulation depth and DC offsets of the generated waveform, allowing greater control over the data encoding. This flexibility in operation allows the CMOS driver to directly modulate each  $\mu$ LED independently with different encoding schemes. The concept was tested with stepped sawtooth, or staircase-like, waveforms, representative of pulse amplitude modulation scheme. The optical output waveforms from a single  $\mu$ LED element in response to such input signal are shown in Fig. 8. The  $\mu$ LED element was operated at 10 MHz at an offset of 240 mA with a modulation depth of 16 mA. Using an input with 4-level input waveform as shown in Fig. 8(a), the corresponding  $\mu$ LED output also showed four distinct intensity levels clearly [see Fig. 8(b)]. The data rates presented here are lower than in our other work, which used multiple parallel channels to increase the aggregate data rate [19]. However, we wish to highlight that, since the modulation bandwidth of  $\mu$ LED elements was shown to be greater than 400 MHz, it does not limit the data rates achievable using this CMOS-driven system. Further optimization work is ongoing on both driver and  $\mu$ LED parts to improve the VLC performance of this integrated system.

#### 4. Conclusion

In summary, we present the design, process flow development, performance characterization and application of an innovative GaN-based  $\mu$ LED array. In this design,  $\mu$ LED elements share a common p-electrode with individually addressable n-electrodes. This is a reversed structure compared with the conventional GaN-based arrays, which makes the array compatible with an NMOS transistor-based CMOS driver for faster modulation. We have optimized the fabrication process to improve the yield and uniformity of individual  $\mu$ LED elements. By integrating an array emitting at 450 nm with a custom NMOS transistor-based CMOS driver, application to VLC, and in particular to multi-level data encoding schemes, is also demonstrated.

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