Multi-Tasking dc-dc and dc-ac Converters for dc Voltage Tapping and Power Control in Highly Meshed Multi-Terminal HVDC Networks

Grain Philip Adam*, Ibrahim Abdelsalam**, Lie Xu*, John Fletcher***, Graeme Burt* and Barry Williams*
*University of Strathclyde; **Arab Academy for Science and Technology and Maritime Transport, Cairo, Egypt; and
***University of New South Wales, Sydney, Australia.
grain.adam@strath.ac.uk; i.abdelsalam@aast.edu, lie.xu@strath.ac.uk; john.fletcher@unsw.ed.au; graeme.burt@strath.ac.uk; and barry.williams@strath.ac.uk

***Abstract*—this paper extends a recently proposed dc auto-transformer to a true multi-port converter that can function simultaneously as dc auto-transformer and a dc/ac converter for dc voltage matching and tapping, and power control in highly meshed multi-terminal dc grids. The presented multi-port converter can generate multiple adjustable dc voltages from a fixed or variable input dc voltage, or from an active ac grid. Theoretical discussions and simulations indicate that when the proposed multi-port converter is used as a hybrid dc and ac hub to manage congestions and resolve loop flow issues in a highly meshed multi-terminal dc network, large dc power can be fed to the lower dc terminal, without exposing the switching devices of the lower sub-converter to excessive current stress. Its increased control flexibility and response to dc faults at high and low dc terminals are validated using simulations and experiments.**

Key words: modular multilevel converter; multi-terminal dc grids; multi-port converter; high-voltage direct current transmission systems.

I. INTRODUCTION

Highly meshed multi-terminal high-voltage direct current (MT-HVDC) networks are seen as an important first step for the generic implementation of smart and super transmission grids where large powers can be exchanged over wide geographical areas, with full control over the power flow at each dc or ac node retained. Such networks or grids are expected to be comprised of several dc voltage levels as in traditional ac grids. The dc voltage level in each segment of such networks will be determined by the power transfer capacity and the thermal limit of the employed dc lines. In such dc networks, dc/dc converters are expected to act as voltage matching and power control devices, including isolation in settings where galvanic isolation or dc fault containment are necessary. This entails that the dc/dc converters in a MT-HVDC network must perform voltage matching plus the functionalities of present flexible ac transmission system (FACTS) devices.

Recently, several isolated and non-isolated modular dc-dc converters suitable for MT-HVDC networks have been proposed [1-10]. Isolated versions of these converters are developed around the front-to-front (F2F) connected ac/dc converters that prevent the impact of a dc fault from propagating beyond the affected side. This feature can be exploited to minimize the number of dc circuit breakers needed and to divide a large MT-HVDC network into several isolated protection zones. The main drawback of a F2F dc/dc converter is that both of its high and low voltage converters and interfacing transformer must be rated to 1.0pu, and their active and passive devices are exposed to full load currents. Thus the power loss of the F2F dc/dc converter is the same as that of the back-to-back HVDC link of similar power rating, which is not insignificant.

In an effort to reduce the capital cost and footprint of the F2F modular dc/dc converter, references [7, 8] operate it in a quasi-two-level (Q2L) mode. In this mode, the MMC cell capacitors are used briefly to facilitate stepped transitions of the output phase pole between the positive and negative dc rails, with a brief time (a few μs) spent at each intermediate voltage level. This allows the cell capacitance, arm inductance and current rating of all switching devices in series with the cell capacitors of the half-bridge cells, to be reduced drastically. This Q2L approach allows the ac link of the F2F modular dc/dc converter to be a quasi-square waveform, with the coupling transformer in the ac link exposed to low and controlled *dv/dt*, and with exploitation of the real powers of the dominant low-order harmonics such as the 3rd, 5th and 7th.

Further reduction in the dc/dc converter capital cost and footprint is achieved when the MMCs in F2F dc/dc converters are replaced by the transition arm converter (TAC) [2]. These gains are achieved, because the TAC is a half-bridge version of an

alternative arm converter [4, 11, 12], but where all half-bridge cells are moved to one arm and the switches that form each director switch are turned on and off individually [2].

The most promising non-isolated modular dc/dc converter (auto dc-transformer, with partial dc fault blocking capability) is presented in [6, 13]. Its main attributes are: the switching devices of the low-voltage stage do not experience the full current associated with power transfer; and the MVA rating of an ac transformer that connects the upper and lower sub-converters from the ac side represents *(n-1)/n* of the dc/dc converter rated power, where $n=V_{dc1}/V_{dc2}$, and V_{dc1} and V_{dc2} are the dc link voltages of the high and low voltage sides. Several variants of this auto dc transformer, including F2F and multi-pole versions, are presented in [6]. However, the vast possibilities hidden in these converters are not explored, including details of their control philosophies.

Another version of a modular auto dc transformer is presented in [3]. The main weakness of the modular dc/dc converter in [3] is that it requires extremely large passive filters to remove the fundamental ac component that is deliberately injected into the modulating signals to facilitate power exchange within the converter from the positive and negative dc pole voltages.

In [1], several non-isolated buck and boost hybrid cascaded dc/dc converters are proposed for HVDC applications. In these dc/dc converters, full-bridge cells in each limb are used as an active power filter to attenuate the deliberately injected ac components in each limb in order to generate any desired dc voltage magnitude from a fixed input dc voltage. Absence of ac transformers in the hybrid cascaded dc/dc converters in [1] is advantageous as this leads to cheaper and lighter dc/dc converters than those presented in [6, 13]. However, the main shortcoming of these converters is that the director switches and full-bridge chain link of each limb must be sized to block the full dc link voltage of the high-voltage side when the dc fault is at the low-voltage side. This leads to higher semiconductor losses.

This paper extends the concept of dc auto-transformer originally presented in [6, 13] to generic multi-port modular dc-dc and dc-ac converters that can generate multiple independent dc outputs relative to dc ground and a number of independent ac outputs from a fixed or variable input dc voltage. The presented converter offers a cost effective solution when creating a hybrid hub that facilitates dc voltage matching and tapping, and power control in highly meshed future dc grids. The theoretical basis of the proposed multi-port converter is explained using basic two-port and three-port converters, and corroborated using simulations and experimentations, considering different operating modes. This paper identifies the main theoretical relationships that govern the power flow within the proposed multi-port converters, beyond that covered in [6, 13]. For example, in the two-port version the current stresses in the switching of the lower sub-converters are linked to their ac powers not the total power being fed to the lower dc terminals as explained in [6, 13]. Also, it has been shown that with an increased number of ports, the total power is shared between several sub-converters, leading to a significant reduction in the rated power of the low-voltage sub-converters and their currents' stresses.

II. MULTI-FUNCTION DC/DC AND DC/AC MODULAR MULTILEVEL CONVERTER

A) Operating principle

Figure 1 presents multi-port modular multilevel converters that can be used as a fully controllable dc/dc and dc/ac hub in highly meshed multi-terminal dc grids to facilitate power control and dc voltage matching and tapping. The proposed multi-port configurations are derived from the auto dc transformers presented in [6, 13]. For a given rated power and high and low dc voltages V_{dc1} to V_{dc5}, the two, three and five port converters in Figure 1 can control active and dc powers in all directions. But the current stresses in the semiconductor switch of the upper and lower sub-converters of the multi-ports in Figure 1 vary with the power flow direction rather than the dc voltage transformation ratio, as suggested in [13], these current stresses can be reduced as the number of ports increases. Considering the power flow directions indicated by the dc current polarities in Figure 1(a) for illustration, the active powers the upper and lower sub-converters exchange with the ac side can be approximated in terms of dc link currents and voltages by:

$$P_{ac1} = \tfrac{3}{2} V_{m1} I_{m1} \cos(\delta_1 + \varphi_1) \approx 3(V_{dc1} - V_{dc2}) I_{d1}$$
$$P_{ac2} = \tfrac{3}{2} V_{m2} I_{m2} \cos(\delta_2 + \varphi_2) \approx 3 V_{dc2} I_{d2} \quad (1)$$

where, I_{d1} and I_{d2} are dc components in the arms of the upper and lower sub-converter ($I_{d1}=⅓I_{dc1}$ and $I_{dc2}=3(I_{d2}-I_{d1})\approx 3I_{d2}-I_{dc1}$, δ_1 and δ_2 are the load angles between the terminal voltages of the upper and lower sub-converters relative to the ac grid voltage; φ_1 and φ_1 are power factor angles between the grid voltages and phase currents; and V_{m1} and V_{m2}, and I_{m1} and I_{m2} are the peaks of the terminal voltages and phase currents of the upper and lower sub-converters. Notice that I_{dc2} represents mismatch between dc link currents of sub-converters 1 and 2. Alternatively, P_{ac1} can be expressed as:

$$P_{ac1} = V_{dc1} I_{dc1} (1 - V_{dc2}/V_{dc1}) = P_{dc1}(n-1)/n \quad (2)$$

where, $n=V_{dc1}/V_{dc2}$ and $P_{dc1}=V_{dc1}I_{dc1}$. The net active power exchange between the upper and lower sub-converters in Figure 1(a) and the ac grid P_g is given by an algebraic sum, viz., $P_g=P_{ac1}+P_{ac2}$. Since the peak phase voltages at the ac terminals of the sub-converters 1 and 2 are:

$$V_{m1}=½m_1(V_{dc1}-V_{dc2}) \quad (3)$$

$$V_{m2}=½m_2V_{dc2} \quad (4)$$

The active current associated with the power exchange between the ac and dc sides of the sub-converters 1 and 2 can be expressed in terms of dc currents by: $\tfrac{3}{4} m_1 I_{m1} \cos(\delta_1 + \varphi_1) \approx |I_{dc1}|$ and $\tfrac{3}{4} m_2 I_{m2} \cos(\delta + \varphi) \approx 3|I_{d2}|$.

When the power flow directions in sub-converters 1 and 2 are from the ac to dc side (or from the dc to ac side), the transformer windings and semiconductor switches of the lower sub-converter experience higher current stresses than the upper sub-converter.

$$I_{d1}=⅓|I_{dc1}| \quad (5)$$

$$I_{d2}=⅓|I_{dc1}|+⅓|I_{dc2}| \quad (6)$$

When the power flow direction in the sub-converter 1 opposes that in the sub-converter 2, the mean dc currents in the arms of the sub-converters 1 and 2 are $I_{d1}=⅓|I_{dc1}|$ and $I_{d2}=⅓|I_{dc1}|-⅓|I_{dc2}|$, and active currents in the transformer windings of the upper and lower sub-converters are:

$$|I_{dc1}| \approx \tfrac{3}{4} m_1 I_{m1} \cos(\delta_1 + \varphi_1) \quad (7)$$

$$\big||I_{dc1}| - |I_{dc2}|\big| \approx \tfrac{3}{4} m_2 I_{m2} \cos(\delta + \varphi). \quad (8)$$

This indicates that the switching devices and transformer windings of the lower sub-converter experience lower current stresses when the power flow direction in the upper sub-converter opposes that in the lower; thus, higher overall system efficiency would be expected. In this case, the power exchange between the upper and lower sub-converters through the ac side can be approximated by:

$$V_{dc2}||I_{dc1}|-|I_{dc2}|| \quad (9)$$

When both ac and dc sides of the multi-port converter in Figure 1 (a) are connected to active ac and dc networks, ac powers P_{ac1} and P_{ac2} can be controlled to optimize the current stresses in sub-converters 1 and 2, independent of n. This is because P_{ac1} can be used to specify the amount of dc power to be exchanged between sub-converter 1 and 2 through their arm, without passing through the ac side:

$$P_{dc12}\approx P_{dc1}/n\approx P_{ac1}/(n-1) \quad (10)$$

Whilst P_{ac2} defines the proportions of P_{dc2} to be sourced from ac side, and current stresses in sub-converter 2. In this manner, the entire dc power required at dc terminal of the sub-converter 2 (P_{dc2}) can be provided through the dc side, with $P_{ac2}=0$ and zero current stresses on its switching devices, provided that the ratio n is sufficiently high to avoid overstressing switches of the sub-converter 1. For an example, when V_{dc1}=1200kV, V_{dc2}=400kV, $n=V_{dc1}/V_{dc2}$=3, and transformer windings connected to sub-converters 1 and 2 rated at 600kV and 200kV, 400MW could be delivered to dc terminal of sub-converter 2 with $P_{ac2}=0$:

$$P_{ac1}=(n-1)P_{dc12}=2\times 400\text{MW}=800\text{MW} \quad (11)$$

Notice that under such operating condition, the dc link currents I_{dc1} and I_{dc2} are: $I_{dc1}=P_{ac1}/(V_{dc1}-V_{dc2})=800\times 10^3/800=1$kA and $I_{dc2}=P_{dc2}/V_{dc2}=400\times 10^3/400=1$kA as anticipated.

Figure 1 (b) and (c) present the cases where the proposed multi-port converter can generate multiple dc voltage levels with positive and negative polarities with respect to ground, while ensuring that current stresses are shared between sub-converters. In the multi-port converter in Figure 1 (b), sub-converters 1 and 2 exchange power between their dc sides using both ac and dc sides as in two-port converter in Figure 1 (a). Whilst sub-converter 3 exchanges power using its ac link only, sharing an ac power (P_{ac1}) sub-converter 1 presents to its ac side with sub-converter 2. Such arrangement offers reduced current stress on the sub-converter 2 when tri-port converter in Figure 1 (b) operates as an auto transformer, with no connection to the ac grid. In this case, when the sub-converter 1 is sourcing ac power (P_{ac1}) and sub-converters 2 and 3 are both sinking ac powers P_{ac2} and P_{ac3}, the amount of ac power will be transferred through sub-converter 2 is:

$$P_{ac2}=P_{ac1}-P_{ac3} \quad (12)$$

Full definition of P_{ac1} is sufficient for determination of the magnitudes and directions of the total dc power (P_{dc1}) at high-voltage dc terminal $P_{dc1}=nP_{ac1}(n-1)$, and the amount of dc power to be exchanged between sub-converters 1 and 2 without passing through ac side (P_{dc1}/n).

When the ac side of the proposed tri-port converter is connected to the ac grid, the magnitude of the dc power (P_{dc2}) at the terminal of sub-converter 2 is determined by P_{ac1} and P_{ac2}, with P_{ac1} determining the amount of power to be transferred from sub-converter 1 to 2 through the dc side without passing by the ac side, and P_{ac2} determines the proportion of power to be transferred from ac side of sub-converter 2 to its dc side:

$$P_{dc2}\approx P_{dc1}/n+P_{ac2}\approx P_{ac1}/(n-1)+P_{ac2} \quad (13)$$

In both of the above cases, the dc power of sub-converter 3 (P_{dc3}) is determined exclusively by its ac power (P_{ac3}). Operating principle of the five-port converter in Figure 1(c) is similar to that of the tri-port in Figure 1, including the power exchange between its sub-converters. Besides the aforementioned attributes, the multi-ports in Figure 1 do not expose the dc cables and converter transformers to excessive dc voltage stresses as with some versions of the tri-pole multi-port dc/dc converter recently presented in [6].

B) DC fault handling

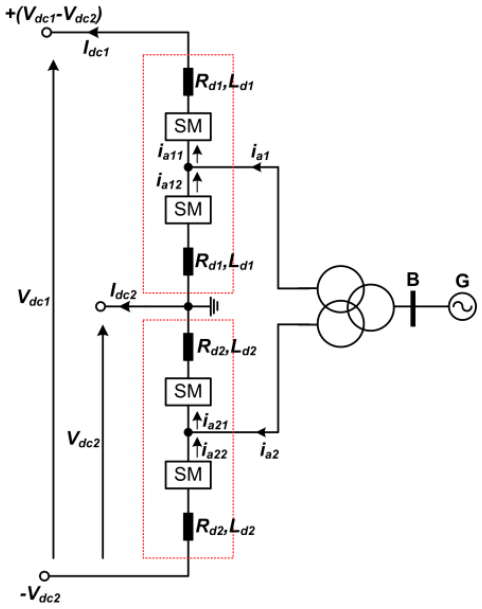
The proposed multi-port converters in Figure 1 can ride through different permanent dc faults, with limited loss of power transfer capacity and with minimum interruption time.

For example, a permanent pole-to-ground dc fault at a positive pole of the tri-port converter in Figure 1 (b) requires that sub-converter 1 to be blocked briefly and the remaining sub-converters '2' and '3' must reduce their active power exchange to zero temporarily until the dc fault is cleared by the dc circuit breaker connected to the positive pole. Then the remaining sub-converters '2' and '3' can resume power transfer, operating as a two-port converter (switching devices of sub-converters '2' and '3' would not experience high surge currents from the ac side as their dc link voltages remain unaffected) . If additional reactive power support is needed, upper sub-converter '1', which is connected to the isolated dc pole, can be unblocked to operate as a static synchronous compensator (STATCOM). Similarly, the implications of a permanent pole-to-ground dc fault at the negative dc pole of sub-converters 2 and 3 (switching devices of affected converter will be exposed to high current stresses, while no substantial ac in-feed current will be observed at the ac terminals of the unaffected sub-converters).

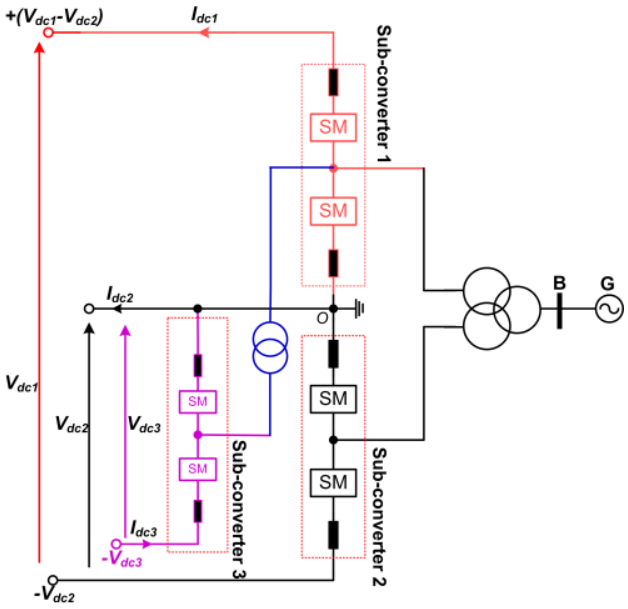
During a pole-to-pole dc short circuit fault at the high-voltage dc terminals, between the two outer dc cables at V_{dc1}-V_{dc2} and $-V_{dc2}$ from the ground level, both sub-converters '1' and '2' must be blocked and the dc power of the sub-converter '3' must be reduced to zero until the dc fault is cleared. Then sub-converter '3' can resume power exchange with the ac side, operating as a typical asymmetrical monopole.

III. CONTROL SYSTEMS

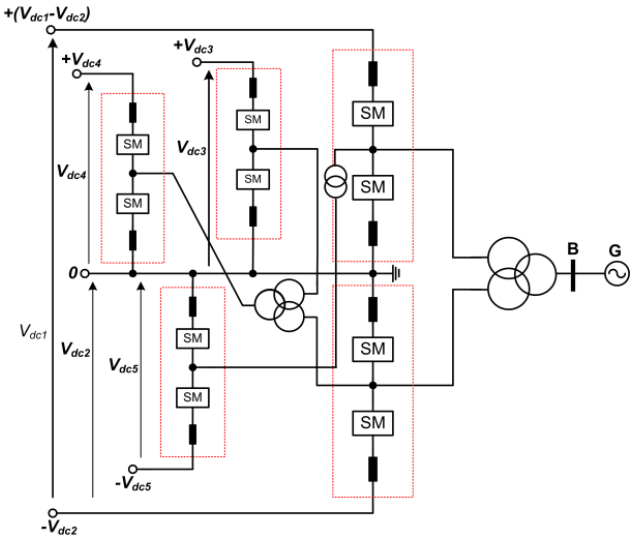
When the ac side of the proposed multi-function dc-dc and dc-ac MMC is fed from an active ac network, as in Figure 1(a), the power exchange between its ac/ac, ac/dc and dc/dc terminals can be controlled by manipulating the phase and magnitude of the voltage vectors at the terminals of the upper and lower sub-converters relative to grid, as illustrated in Figure 1(d).



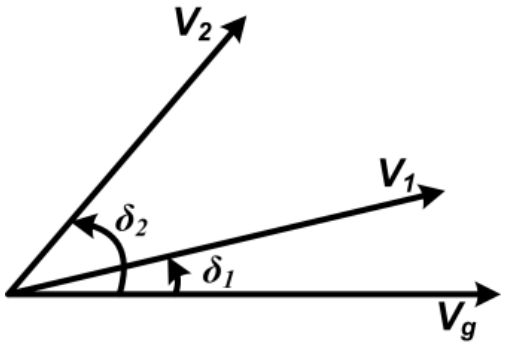
(a) Two-port dc/dc plus dc/ac converter



(b) Tri-port dc/dc plus dc/ac converter



(c) Five-port dc/dc and dc/ac converter



(d) Voltage vectors that represent grid voltage $\boldsymbol{V_g}$ and terminal voltage of the upper and lower sub-converters, $\boldsymbol{V_1}$and $\boldsymbol{V_2}$

Figure 1: Evolution of the proposed multi-port dc/dc and dc/ac converter

The load angle difference δ_1-δ_2 determines the magnitude and direction of active power flow (P_{ac2}) being exchanged between the upper and lower sub-converters through the ac side, and $I_{dc1}V_{dc2}=I_{dc1}V_{dc1}/n=P_{dc1}/n$ determines the dc power being exchanged between the upper and lower sub-converters not passing through the ac side. When $\delta_1+\delta_2=0$, no active power is injected into the ac grid; but the entire ac power of the upper sub-converter is exchanged with the lower sub-converter ($P_{ac2}=-P_{ac1}$, where $P_{ac1}=P_{dc1}(n-1)/n$ and $I_{dc2}=nI_{dc1}$), resembling the dc auto-transformer operation presented in [13]. When $\delta_2-\delta_1=0$, no power is exchanged between the upper and lower sub-converters through the ac side; instead the entire power exchange between the upper and lower sub-converters is through the dc side ($P_{ac2}=0$). This discussion indicates that the upper and lower sub-converters of the multi-function MMC being studied can be controlled independently.

For instance, when the ac side of the two-port system in Figure 1 (a) is connected to a dead ac network (without generation), one of the sub-converters must set a stiff ac bus in the ac link and the other sub-converter must regulate the active power exchange.

Recall that defining the set point for P_{ac1} determines the total input dc power at the high-voltage dc terminal, $P_{dc1}=nP_{ac1}/(n-1)$ and dc link current $I_{dc1}=P_{dc1}/V_{dc1}=n/(n-1)\times P_{ac1}/V_{dc1}$.

When the power flow in the upper sub-converter opposes that in the lower sub-converter and $P_{ac1}>P_{ac2}$, P_{ac2} determines the power exchanged between the upper and lower sub-converters through the ac side and that to be injected into the ac grid, $P_g=P_{ac1}+P_{ac2}$. Considering the case above but with $P_{ac2}>P_{ac1}$, P_{ac1} determines the power exchanged between the upper and lower sub-converters through the ac side and $|P_{ac1}-P_{ac2}|$ determines ac power to be exchanged with the ac grid. When the power flow directions in the upper and lower sub-converters are in the same direction, there is no power exchange between the upper and lower sub-converters through the ac side; instead the entire power exchange is through the dc side, and individual sub-converters and the ac grid.

Considering the duality model of the three-winding transformer in [14], the basic differential equations that describe the upper and lower sub-converters of the system in Figure 1 (a) can be expressed with reference to the secondary and tertiary sides as:

$$\begin{aligned} L_{T1}\frac{di_{abc1}}{dt}+R_{T1}i_{abc1} &= v^{s}_{abcg}-\tfrac{1}{2}(V_{dc1}-V_{dc2})-\tfrac{1}{2}(v_{labc1}-v_{uabc1}) \\ L_{T2}\frac{di_{abc2}}{dt}+R_{T2}i_{abc2} &= v^{t}_{abcg}-\tfrac{1}{2}V_{dc2}-\tfrac{1}{2}(v_{labc2}-v_{uabc2}) \end{aligned} \quad (14)$$

where $R_{T1}=½R_{d1}+R_s+R_{ps}$ and $R_{T2}=½R_{d2}+R_t+R_{pt}$ and $L_{T1}=½L_{d1}+L_s+L_{ps}$ and $L_{T2}=½L_{d2}+L_t+L_{pt}$ are equivalent lumped series resistances and inductances refer to the secondary and tertiary sides; R_{ps} and R_{pt}, and L_{ps} and L_{pt} are transformer primary resistance and inductance referred to secondary and tertiary sides; R_s and R_t, and L_s and L_t are resistances and inductances of the secondary and secondary windings. Because of the asymmetrical nature of the upper and lower sub-converters in Figure 1(a), the dc components $½(V_{dc1}-V_{dc2})$ and $½V_{dc2}$ cancel with those in the converters' terminal voltages v^{s}_{abcg} and v^{t}_{abcg} when seen from secondary and tertiary sides of the upper and lower sub-converters. Thus, $v^{s}_{abcg}-\tfrac{1}{2}(V_{dc1}-V_{dc2})\approx v_{abcs}$ and $v^{t}_{abcg}-\tfrac{1}{2}V_{dc2}\approx v_{abct}$, and since the dc free terminal voltages of the upper and lower sub-converters can be expressed in terms of their corresponding upper lower arm voltages: $\tfrac{1}{2}(v_{labc1}-v_{uabc1})\approx v^{abc}_{c1}$ and $\tfrac{1}{2}(v_{labc2}-v_{uabc2})\approx v^{abc}_{c2}$. With these assumptions, the *d-q* version of equation (14) is:

$$\begin{aligned} di_{dq1}/dt &= -R_{T1}i_{dq1}/L_{T1}+(v_{dqs}-v_{cdq1}-j\omega L_{T1}i_{dq1})/L_{T1} \\ di_{dq2}/dt &= -R_{T2}i_{dq2}/L_{T2}+(v_{dqt}-v_{cdq2}-j\omega L_{T2}i_{dq2})/L_{T2} \end{aligned} \quad (15)$$

Equation (15) indicates that two independent current controllers are needed for the upper and lower sub-converters of the two-port converter in Figure 1(a). These current controllers are:

$$\begin{aligned} \lambda_{dq1} &= k_{pi1}(i^{*}_{dq1}-i_{dq1})+k_{ii1}\int(i^{*}_{dq1}-i_{dq1})dt \\ \lambda_{dq2} &= k_{pi2}(i^{*}_{dq2}-i_{dq2})+k_{ii2}\int(i^{*}_{dq2}-i_{dq3})dt \end{aligned} \quad (16)$$

$$\begin{aligned} v_{cdq1} &= v_{dqs}-j\omega L_{T1}i_{dq1}-\lambda_{dq1} \\ v_{cdq2} &= v_{dqt}-j\omega L_{T2}i_{dq2}-\lambda_{dq2} \end{aligned} \quad (17)$$

Hence, the outer loops that control direct axis voltage, active power or dc voltage set i^{*}_{d1} and i^{*}_{d2}, while i^{*}_{q1} and i^{*}_{q2} are set from the outer loops that regulate reactive power or quadrature axis voltage. The overall control structures employed to control the upper and lower sub-converters of the two-port system in Figure 1(a) are similar to those of the active power or dc voltage regulators of a typical MMC based HVDC link [15, 16]. Generic block diagram that summarizes the implementation of the control system employed in this paper is shown in appendix, see Figure 11.

IV. SIMULATIONS

To illustrate the control flexibility that the proposed multi-function dc-dc and dc-ac MMC can offer to future power systems, the two and three-port converters in Figure 1 are simulated using the average model in [17, 18] and the following parameters: arm reactors ($R_{d1}=R_{d2}=0.5\Omega$, $R_{d3}=0.4\Omega$; $L_{d1}=L_{d2}=45$mH and $L_{d3}=30$mH); cell capacitances ($C_{m1}=C_{m2}=10$mF and $C_{m3}=8$mF); Converter transformer ($R_p=R_s=R_t=0.002$pu, $L_p=L_s=L_t=0.05$pu, 1300 MVA and 400 kV/300 kV/300 kV); and 400 kV ac grid with 15000 MVA three-phase short circuit ratio and $X/R=15$. In this study, the sub-converters in Figure 1(a) employ the following

controllers: DC voltage or active power control; reactive power at B is regulated to zero; fundamental current control in the synchronous reference frame; and a controller for suppressing the circulating current.

A) Two-port multi-function dc-dc plus dc/ac converter

i) Independent control of high and low voltage dc terminals:

Figure 2 shows waveforms when the upper and lower sub-converters of the multi-function dc-dc and dc-ac converter in Figure 1 regulate their dc link voltages V_{dc1}-V_{dc2} and V_{dc2} independently, feeding two passive loads of 1800Ω (800MW) and 900Ω (400MW) connected to the high and low voltage dc terminals, respectively. Initially, V_{dc1}-V_{dc2} and V_{dc2} are regulated at 600 kV and at t=1s, V_{dc1}-V_{dc2} is increased by 20%. Figure 2 (a) and (b) show the dc voltages V_{dc1} and V_{dc2}. These voltages show that the proposed multi-port converter can be used for dc voltage tapping like a conventional ac auto-transformer, with full control over the dc voltages of both dc terminals. However, minimum and maximum limits for the variation of the dc link voltages are constrained by the transformer's voltage (turns) ratios and their insulation levels. Figure 2 (c) shows the dc powers the upper and lower sub-converters exchange with the ac side, and the total dc power consumed by the two dc loads connected to the high and low voltage dc terminals. Figure 2 (d) shows the active powers being exchanged through the upper and lower converters of the multi-port converter, including the total active power exchanged with the ac grid. Figure 3 (a) and (b) are the ac current waveforms at the terminals of the upper and lower sub-converters, and Figure 3 (c) and (d) show the corresponding upper and lower arm currents for phase '*c*'. The lower sub-converter experiences higher current stresses than the upper sub-converter, as explained in section II (when the power flow in the upper and lower sub-converters are in the same direction). Figure 3(e) shows the dc link currents I_{dc1} and I_{dc2} and corresponding dc currents in the arms of the upper and lower MMC sub-converters. The results in Figure 3 (c), (d) and (e) are consistent with the theoretical discussion regarding distribution of the current stresses between the upper and lower converters of the proposed systems when the power flow directions are the same in the dc terminals of sub-converters 1 and 2.

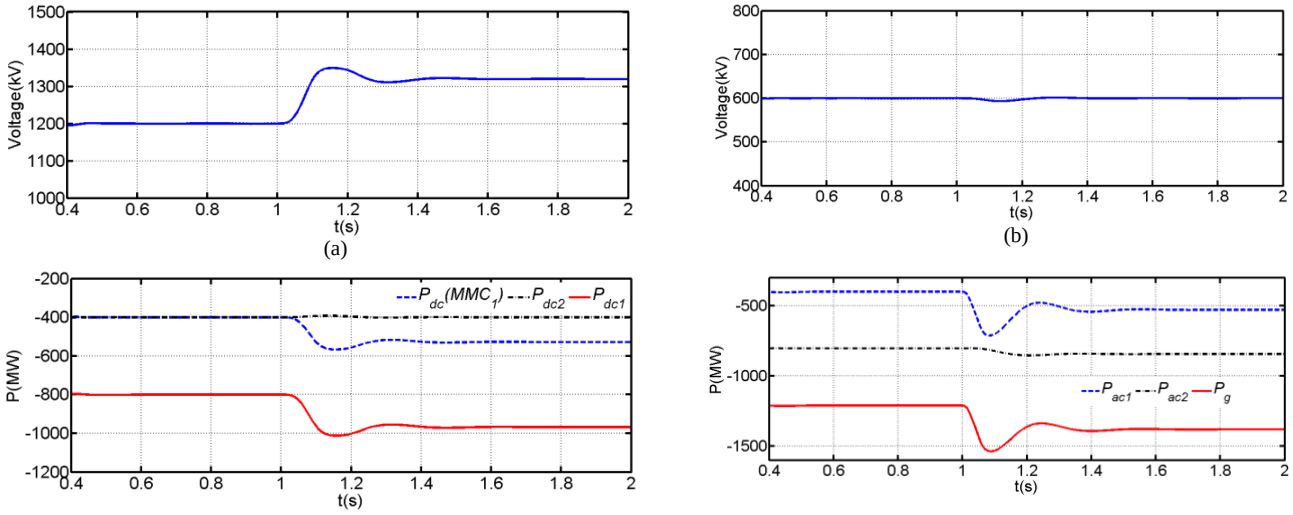
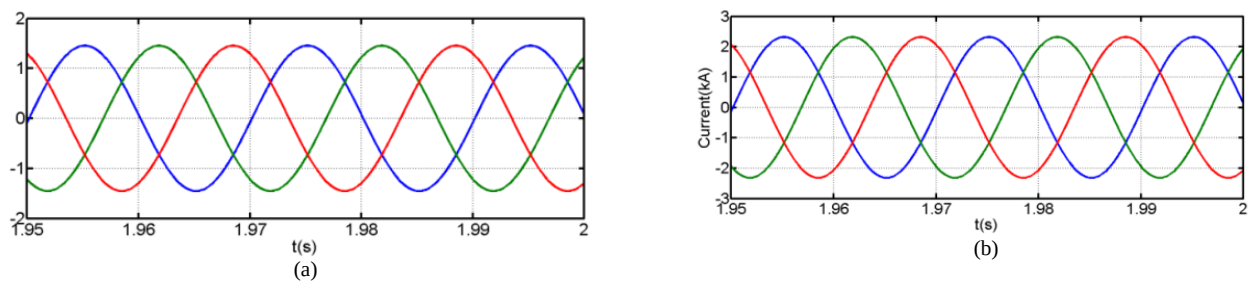
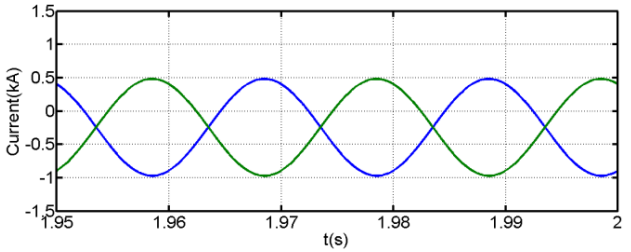
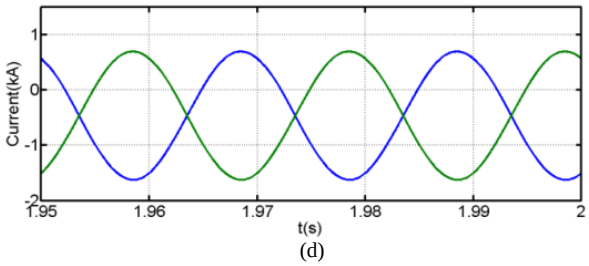


Figure 2: Simulation waveforms for the two-port scheme in Figure 1(a) with V_{dc1} and V_{dc2} initially set to 1200 kV and 600 kV and at t=1s, V_{dc1}-V_{dc2} is increased by 20% (resistive loads connected to the high and low voltage dc terminals are R_{dc1}=1800Ω and R_{dc2}=900Ω): (a) DC voltage of the high-voltage dc terminal, V_{dc1}, (b) DC voltage of the low-voltage dc terminal, V_{dc2}, (c) DC power contributed by the upper converter, P_{dc} MMC_1, dc power at the low and high voltage dc terminals P_{dc2} and P_{dc1} and (d) Active power at input terminals of the upper and lower sub-converters, P_{ac1} and P_{ac2} and total active power drawn from the ac grid, P_g

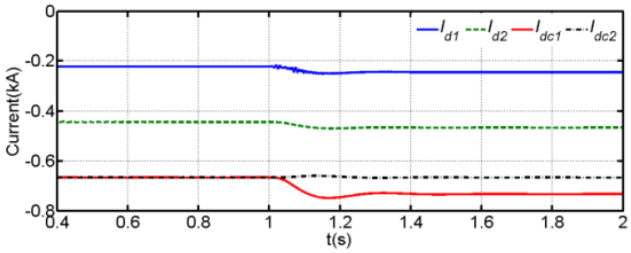




(c)



(d)



(e)

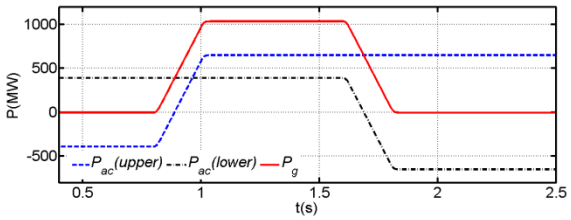
Figure 3. Simulation waveforms for the two-port scheme in Figure 1(a) when V_{dc1} and V_{dc2} initially set to 1200 kV and 600 kV and at t=1s, V_{dc1}-V_{dc2} is increased by 20% (resistive loads connected to the high and low voltage dc terminals are R_{dc1}=1800Ω and R_{dc2}=900Ω): (a) Three-phase currents at the input of the upper sub-converter, (b Three-phase currents at the input of the lower sub-converter) , (c) Phase '*c*' upper and lower arm currents of the upper sub-converter and (d) Phase '*c*' upper and lower arm currents of the lower sub-converter and (e) DC link currents (I_{dc1} and I_{dc2}) and dc components in the arm currents of the upper and lower sub-converters (I_{d1} and I_{d2})

ii) Four quadrant operation of ac and dc terminals:

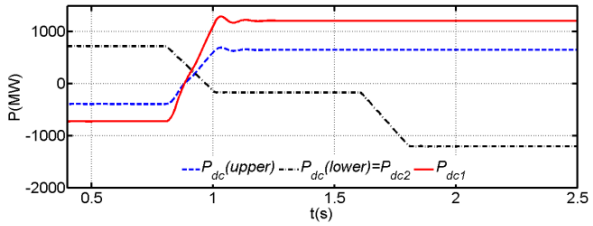
Figure 4 presents waveforms when the upper and lower sub-converters regulate their active power exchange with the ac grid as follows:

- Initially, the upper sub-converter sets its power exchange with the ac side at -390 MW (from ac to dc); and at t=0.8s, it changes the magnitude and direction of the power flow from -390 MW to 650 MW.
- Initially the lower sub-converter sets its power exchange with the ac grid at 390 MW (from dc to ac); and at t=1.6s, it changes the magnitude and direction of the power flow from 390 MW to -650 MW.

Figure 4 (a) shows active powers the upper and lower sub-converters exchange with the ac grid, including the total active power exchanged with the ac grid. When the upper and lower sub-converters have the same power magnitude but opposite direction, zero power is drawn from the ac grid. This indicates that under this operating condition, the proposed multi-function scheme in Figure 1(b) resembles the auto dc transformer proposed in [13]. Figure 4 (b) displays the dc powers at the terminal of the upper and lower sub-converters, including the dc power being exchanged at the high and low voltage dc terminals. Figure 4 (c) and (d) present samples of the arm currents of the upper and lower sub-converters. Figure 4 (e) shows the dc currents in the arms of the upper and lower sub-converters, and in the high and low voltage dc terminals. Although a large dc current is observed in the low voltage dc terminal, no sub-converter is exposed to increased current stress apart from that due to the small difference in the dc voltage across the sub-converters.



(a)



(b)

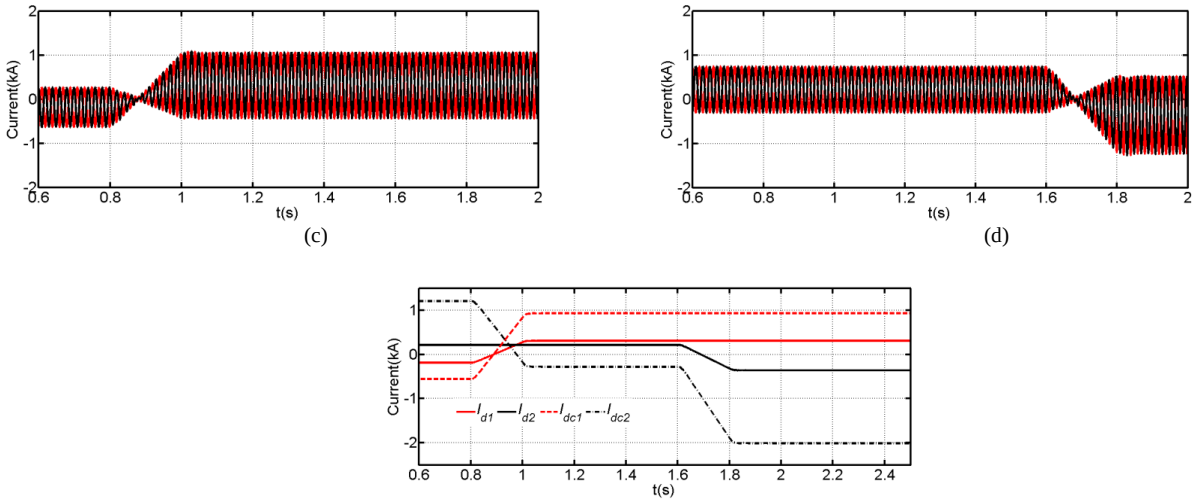
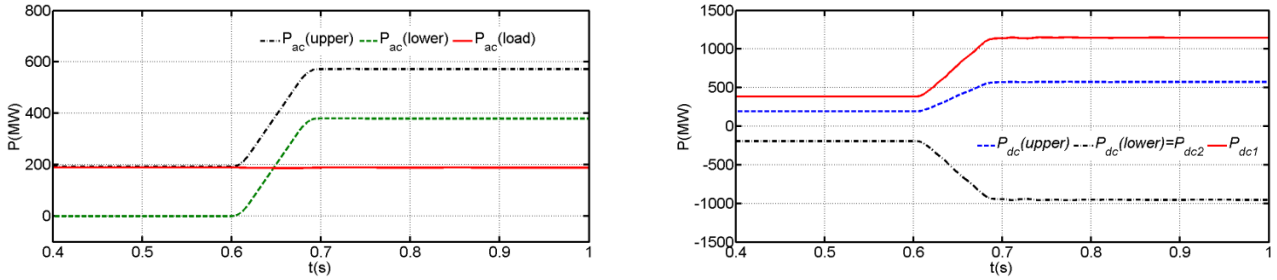


Figure 4. Simulation waveforms when the two-port scheme in Figure 1(b) is operated from two active dc terminals (V_{dc1}=1300 kV and V_{dc2}=600 kV or +700 kV/-600 kV) and an active ac grid, when the upper and lower sub-converters control their active power exchange with the ac grid: (a) Active powers the upper and lower sub-converters exchange with the ac grid, P_{ac}*(upper)* and P_{ac}*(lower)*, including the total ac power exchanged with the ac grid, P_g , (b) DC powers at the terminals of the upper and lower sub-converters, P_{dc}*(upper)* and P_{dc}*(lower)*, including the high and low voltage dc terminals, P_{dc1} and P_{dc2}, (c) Phase '*c*' upper and lower arm currents of the upper sub-converter, (d) Phase '*c*' upper and lower arm currents of the lower sub-converter and (e) DC currents in the arms of the upper and lower sub-converters, I_{d1} and I_{d2}, and in the high and low voltage dc terminals, I_{dc1} and I_{dc2}

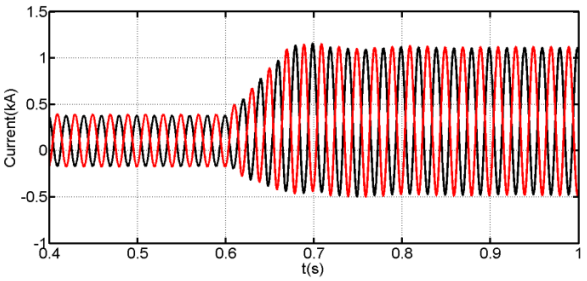
iii) *Power control between dc terminals when ac terminal is connected to a passive load*:

Figure 1(a) is operated from a symmetrical dc link voltage of ±600 kV with its ac side connected to passive load. Fig. 6 shows results when that multi-function scheme is simulated with the transformer primary winding connected to a passive load of 200MW and 50MVAr, and the secondary and tertiary windings are connected to the upper and lower sub-converters. In this illustration, the upper sub-converter is operated in a voltage control mode that sets a stiff ac bus at its terminals, and the lower sub-converter locks to the ac voltage set by the upper sub-converter and controls active power by manipulating its terminal voltage (magnitude and phase) relative to that at the upper sub-converter. Initially, the lower sub-converter regulates its power exchange with the upper sub-converter through the ac side to zero; and at *t*=0.6s, it increases its power exchange through the ac side from 0 to 380 MW. Figure 5(a) shows the active powers the upper and low sub-converters exchange through the ac side, including that consumed by the passive ac load connected to the transformer primary winding. Figure 5 (b) shows the dc powers exchanged by the upper and lower sub-converters, including the low and high voltage dc terminals. Figure 5 (c) and (d) display the arm currents of the upper and lower sub-converters of the proposed multi-port converter, while Figure 5(e) presents dc currents in the upper and lower arms of the upper and lower sub-converters, and in the low and high voltage dc terminals. When the lower sub-converter exchanges zero active power with the ac side, zero currents are observed in its arms, and in this period I_{dc2}=-I_{dc1}; thus I_{d2}=*0*, P_{dc}*(upper)*=P_{dc}*(lower)*, Figure 5 (a) to (e). The results in Figure 5 illustrate the increased control flexibility the multi-function converter offers when its ac side is connected to an ac island with no generation.

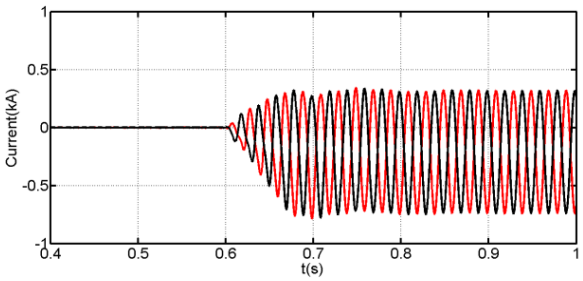


(a) Active powers exchanged between the upper and lower sub-converters, and the ac grid

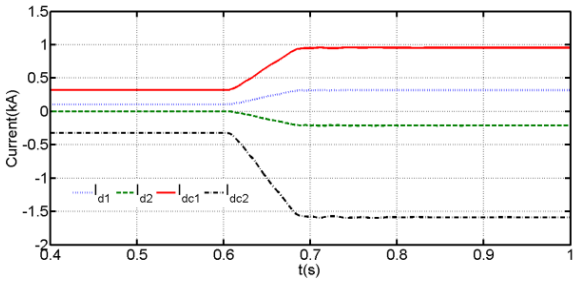
(b) DC powers exchanged between the upper and lower, and in the high and low voltage, dc terminals



(c) Upper and lower arm currents of the upper sub-converter



(d) Upper and lower arm currents of the lower sub-converter

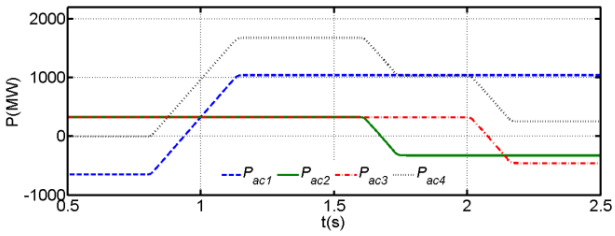


(e) DC currents in the arms of the upper and lower sub-converters, and in the high and low voltage dc terminals

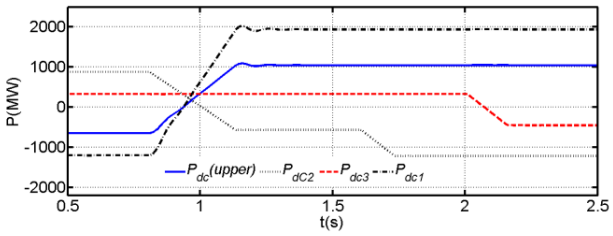
Figure 5: Waveforms when the proposed multi-function dc-dc and dc-ac converter is operated from a symmetrical dc link voltage of ±600kV, with one of the ac terminals connected to an ac island with no generation.

B) Four-quadrant operation of tri-port multi-function dc-dc and dc-ac converter

Figure 6 presents simulation waveforms for the tri-port converter in Figure 1(b), with the initial set-points of sub-converters 1, 2 and 3 set to exchange P_{ac1}=-650 MW, P_{ac2}=325 MW and P_{ac}=325 MW with the ac grid. At times t=0.8s, 1.6s and 2s, sub-converters 1, 2 and 3 are commanded to vary their set-points from -650 MW to +1040 MW, 325 MW to -325 MW and 325 MW to -455 MW respectively. Figure 6 (a) shows that when t<0.8s the proposed tri-port converter in Figure 1(b) operates as a typical auto dc-transformer with multiple dc outputs and zero active power exchange with the ac grid. Figure 6 (b) shows the dc powers at different dc terminals, including at sub-converter 1. From Figure 6 (a) and (b), the power flow distributions in the tri-port converter adhere to the same principles as the two-port converter, as established previously, viz., $P_{ac1}=(n-1)/nP_{dc1}$ and $P_g=P_{ac1}+P_{ac2}+P_{ac3}$. Figure 6 (c) and (d), and Figure 7(a) show sub-converter arm currents as their power set-points vary. Notice that although the dc power at the terminal of sub-converter 2 changes at $t=0.8s$ with P_{ac1} (due to internal dc power transfer from sub-converter 1 to 2 through the dc side), the current stress in the sub-converter 2 arms remain to be defined by P_{ac2}, Figure 6 (a), (b) and (d). Whilst the dc power and current stresses of the sub-converter 3 are merely determined by its ac side power (P_{ac3}). Figure 7(b) displays dc link currents and dc components in the common-mode currents of the different sub-converters, and the dc current distributions in sub-converters 1 and 2 obey the same principles as established for the two-port converter in sections III and IV-A. Results shown in Figure 6 and Figure 7 support the narrative that the current stress in the sub-converter 2 can be reduced independent of n, should its ac power (P_{ac2}) be reduced.



(a)



(b)

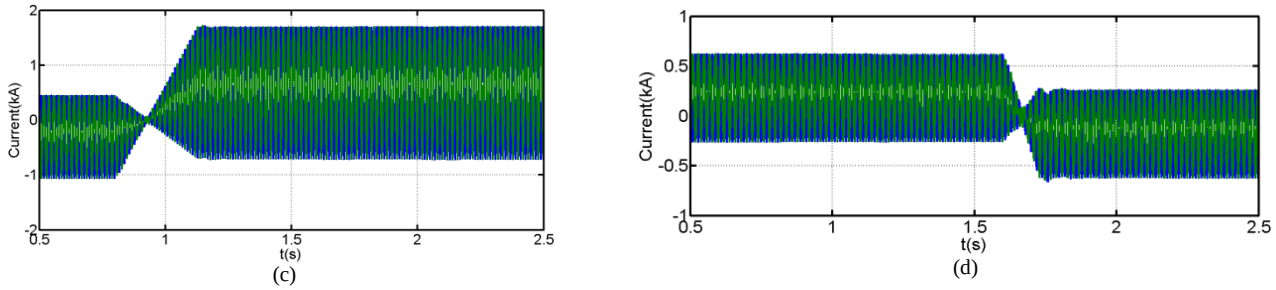
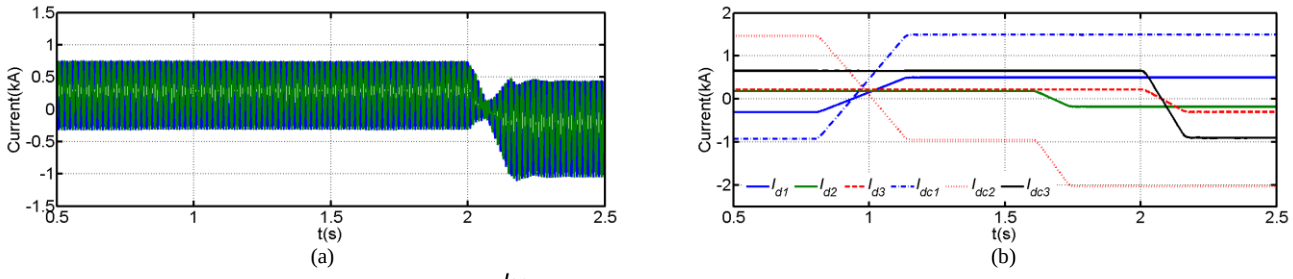
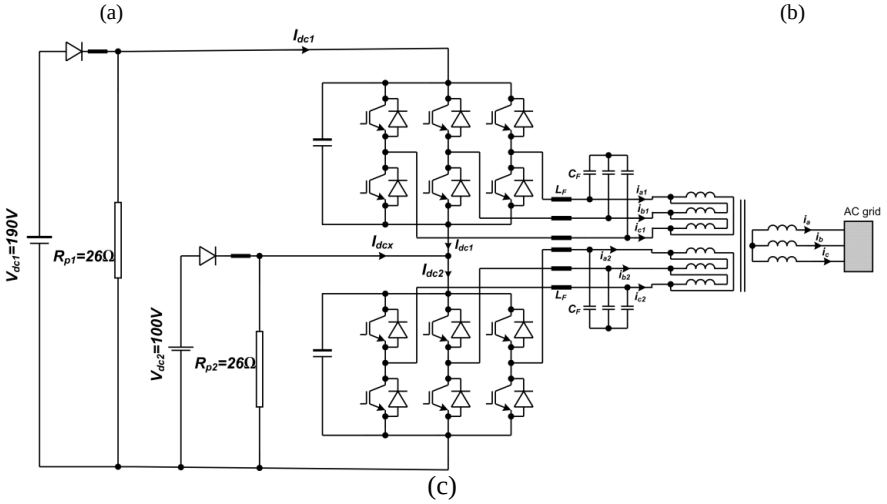


Figure 6. Simulation waveforms for the tri-port modular dc-dc and dc-ac converter in Figure 1 (b) when it is connected to three active dc terminals at V_{dc1}=1300 kV, V_{dc2}=600 kV and V_{dc3}=500 kV, and an active ac grid: (a) Active powers at the terminals of different sub-converters, including that exchanged with the ac grid, (b) DC powers at the sub-converters dc terminals, (c) Phase '*c*' upper and lower arm currents of sub-converter 1and (d) Phase '*c*' upper and lower arm currents of sub-converter 2





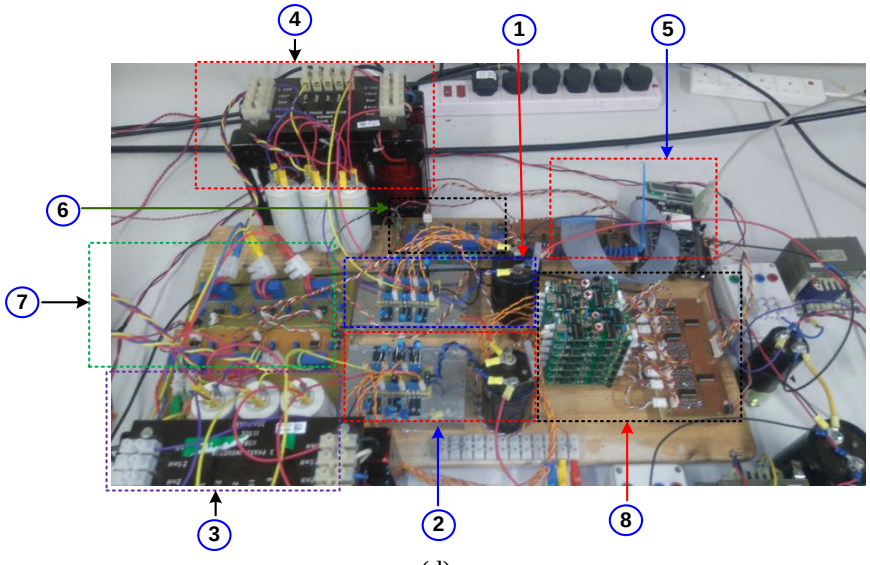


Figure 7. Simulation waveforms for the tri-port modular dc-dc and dc-ac converter in Figure 1 (b) when connected to three active dc terminals at V_{dc1}=1300 kV, V_{dc2}=600 kV and V_{dc3}=500 kV, and an active ac grid: (a) Phase '*c*' upper and lower arm currents of sub-converter 3 and (b) DC components of the common-mode currents of sub-converters 1, 2 and 3 and their corresponding dc link currents. (c) Schematic diagram of the experimental test where the MMCs of the upper and lower sub-converters are replaced by two-level converters, and (d) picture of experimental test rig, where 1 and 2 are upper and lower sub-converters, 3 and 4 are ac filters for upper and lower sub-converters, 5 is the PSoC microcontroller, 6 and 7 are voltage and current transducers, and 8 represent gate drives and complementary board to halve the number of gating signals being generated from PSoC,

V. EXPERIMENTAL VALIDATION

This section uses experimental results obtained from a scaled-down prototype of the two-port dc-dc and dc-ac multi-function converter in Figure 7 (c) and (d) to confirm the validity of the theoretical discussions and simulation results presented in sections II and IV, in particular with regard to the increased control flexibility and dc fault handling. Although all the previous discussions represent the upper and lower sub-converters of the multi-tasking dc-dc and dc/ac converter being studied by MMCs, in the experimental test-rig, these sub-converters are implemented using conventional three-phase two-level voltage source converters as shown in Figure 7 (a) and (b) for simplicity. To mimic bidirectional dc power flow of the active source using single-quadrant dc power supplies (ability to source and sink dc power), a diode and small inductor are connected in series with each of the dc sources and all in parallel with resistors (R_{p1} and R_{p2}, which are selected such that $I_{dc1}R_{p1}<V_{dc1}$ and $I_{dcx}R_{p2}<V_{dc2}$ over the entire operating range; thus, the dc voltages applied of the high and low dc terminals remained fixed by the single-quadrant supplies as $V_{dc1}=(I_{s1}+I_{dc1})R_{p1}$ and $V_{dc2}=(I_{s2}+I_{dcx})R_{p2}$, I_{s1} and I_{s2} are current contribution of the dc supplies connected to the high and low dc terminals respectively). With these resistors, the dc voltages V_{dc1} and V_{dc2} will remain at 190V and 100V as the upper and lower sub-converters vary their reference currents. Table I lists test rig schematic parameters.

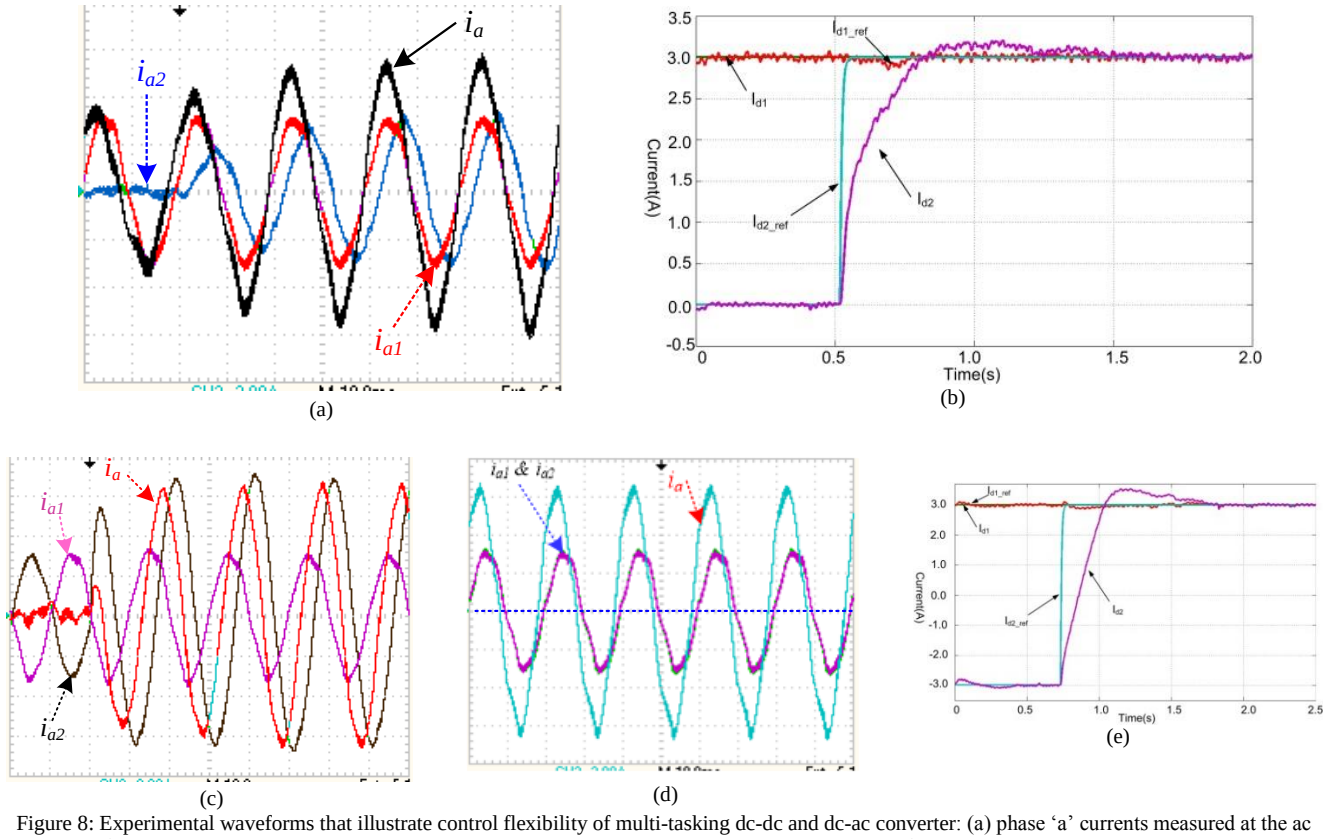


Figure 8: Experimental waveforms that illustrate control flexibility of multi-tasking dc-dc and dc-ac converter: (a) phase 'a' currents measured at the ac terminals of the upper and lower sub-converters and grid side (i_{a1}, i_{a2} and i_a) and (b) direct axis currents of the upper and lower sub-converters (i_{d1} and i_{d2}) when i_{d1_ref} is fixed at 3A and step change is applied to i_{d2_ref} from 0 and 3A and quadrature reference currents of the upper and lower sub-converters are held at zero ($i_{q1}=i_{q2}=0$); when i_{d1}=3A and step change is applied to i_{d2} from -3A to -3A, the experimental waveforms as summarised as follows: (c) represents snapshot of the (i_{a1}, i_{a2} and i_a) zoomed around the time of application of step change to i_{d2} and (d) is the snapshot of the (i_{a1}, i_{a2} and i_a) when the system has reached the steady-state condition, (e) represents the direct axis currents of the upper and lower sub-converters for the latter case. In both cases, the scale is maintained at (10ms/div and 2A/div)

Table I: Test rig parameters

Parameter	Value
Grid voltage	45Vrms at 50Hz
DC link voltage of the high-voltage side (V_{dc1})	190V
DC link voltage of the low-voltage side (V_{dc2})	100V
Phase interfacing inductance (L_F)	2.6mH
AC filter capacitance (C_F)	30μF
Interfacing transformer (Y/Δ/Δ)	400/415/415
Switching frequency	2.4kHz
Sub-converters' dc link capacitors	2.2mF

A)-Demonstration of control flexibility

Figure 8 shows experimental waveforms obtained from the prototype of the multi-tasking dc-dc and dc-ac converter in Figure 8 when it is operated with the following set-points:

- Upper sub-converter maintains its direct and quadrature axis direct currents constant at $i_{d1}=3A$ and $i_{q1}=0$.
- Lower sub-converter changes its direct axis current i_{d2} from 0 to 3A, while its quadrature current is maintained at zero ($i_{q2}=0$).

Figure 8 (a) shows phase '*a*' currents of the upper and lower sub-converters (red and blue) and total current being injected into ac grid (in black). Figure 8 (b) depicts the direct axis currents of the upper and lower converters superimposed on their references. Observe that the phase currents and their d-q versions follow the current commands given to the upper and lower sub-converters. Figure 8 presents additional experimental waveforms obtained under the following operating conditions:

- Upper sub-converter maintains its direct and quadrature axis direct currents constant at $i_{d1}=3A$ and $i_{q1}=0$.
- Lower sub-converter changes its direct axis current i_{d2} from -3 to 3A, while its quadrature current is maintained at zero ($i_{q2}=0$).

Figure 8 (c) and (d) show phase 'a' currents of the upper and lower sub-converters (black and purple) and total current being injected into ac grid (in red) zoomed around the point when step in i_{d2} is applied, and their corresponding steady-state when all transients have died out. Figure 8 (e) depicts the direct axis currents of the upper and lower sub-converters overlaid on their reference currents. Observe that the phase currents and their d-q versions follow the current commands given to the upper and lower sub-converters, with zero grid current when $i_{d2}=-i_{d1}$. This indicates that under this condition the multi-tasking converter in Figure 7 operates as an auto dc-transformer presented in [6, 13].

B) DC faults

i) DC short circuit fault at the high-voltage dc terminal

For illustration of the dc fault response of the multi-port dc-dc and dc-ac converter being studied in this paper, a temporary dc fault is applied at the high-voltage dc terminals (between positive and negative poles) of the prototype in Figure 7, and selected experimental waveforms are summarised in Figure 9. In pre-fault and post-fault conditions, $V_{dc1}=200V$, $V_{dc2}=110V$, $i_{d1}=i_{d2}=2A$ and $i_{q1}=i_{q2}=0$; and during fault period both upper and lower sub-converters are blocked, with their reference direct axis currents reduced to zero. Figure 9(a) and (b) present the dc link voltages of the high and low voltage dc terminals and voltages across the dc link capacitors of the upper and lower sub-converters. Figure 9(c) and (d) show phase '*a*' output currents of the upper and lower sub-converters in red and blue, and the total current being injected into ac grid in black (scope and plotted from scope CSV data that aim to show the peak ac currents during fault). Observe that the dc voltages across the dc link capacitors of both sub-converters collapse and high ac in-feed currents occur at their ac terminals as illustrated in section II-B. Figure 9(e) and (f) display the dc link currents I_{dc1}, I_{dc2} and I_{dcx} in pre-fault, post-fault and during dc short circuit fault (scope and plotted from data to show the peak dc fault currents). These results show that both upper and lower sub-converters of the multi-tasking converter studied are both affected by occurrence of the dc fault at the high-voltage dc terminal even though the lower sub-converter is being supplied from the separate dc source. This is because the upper and lower sub-converters share the same common-mode

current and dc voltage, which causes substantial drop of its dc link voltage, and rapid rise of I_{dcx} and I_{dc2}. But the switching devices of the lower sub-converters are exposed to relatively low current stresses compared to that of the upper sub-converter, and its dc link current (I_{dc2}) exhibits a brief period of rapid current rise followed by extended period of oscillatory and decaying dc fault current (started even before the fault is cleared). From the results in Figure 9 it can be concluded that a permanent dc short circuit fault at the high-voltage dc terminal will lead to loss of power transfer from the upper converter, while the sub-converter could resume power transfer after the fault is cleared.

ii) Pole-to-ground dc fault

Figure 10 shows additional experimental waveforms that illustrate the response of the multi-tasking converter being studied to a dc short circuit fault at the low-voltage dc terminal (negative pole to ground). Figure 10(a), (b), (d) and (e) display the dc link voltages (V_{dc1} and V_{dc2}), ac currents (i_a, i_{a1} and i_{a2}), and dc link currents (I_{dc1},I_{dc2} and I_{dcx}). Observe that the apparent impact of the dc short circuit fault at the low-voltage dc terminal appears to be limited to the lower sub-converter as illustrated in section II-B and confirmed by the ac current and dc link current of the upper sub-converter (no significant increase in their magnitudes).

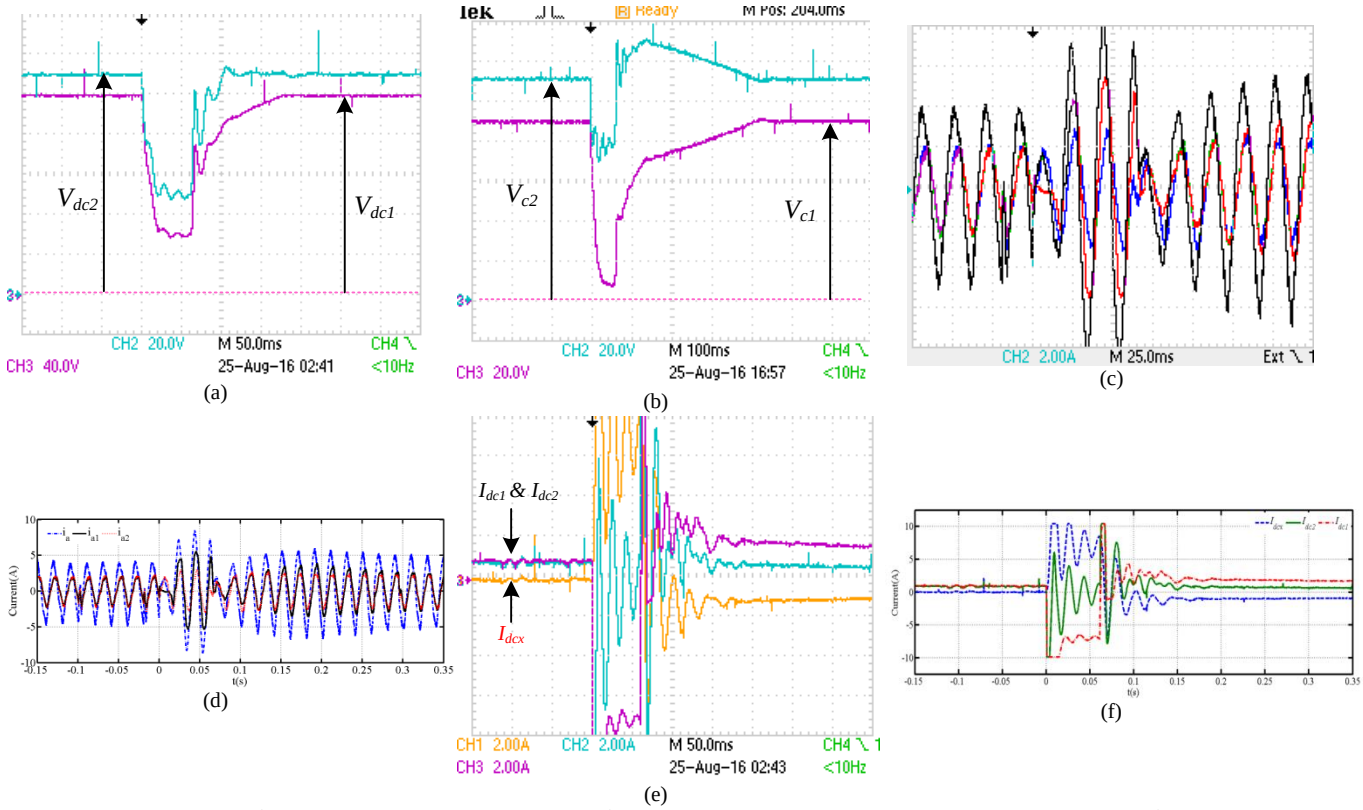
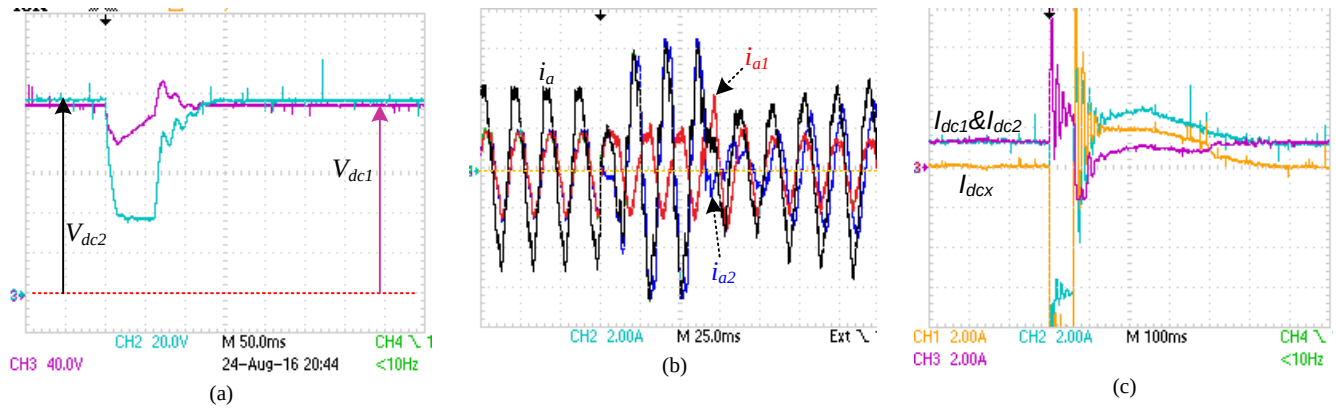
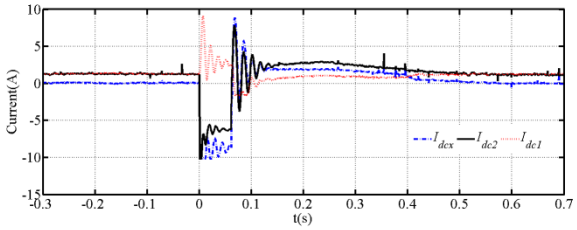


Figure 9. Experimental waveforms when a temporary dc short circuit fault is applied to the high-voltage dc terminal: (a) dc voltages of the high and low dc terminals, (b) dc voltages across the dc link capacitors of the upper and lower sub-converters, (c) line currents i_a, i_{a1} and i_{a2} measured at the primary, secondary and tertiary windings of the interfacing transformer, (d) are dc link currents I_{dc1}, I_{dc2} and I_{dcx} and (e) are the same dc link currents which are plotted from scope csv data to show the missing parts from the scope version in (d) due to scale used





(d)

Figure 10. Experimental waveforms that illustrate the behaviour of multi-tasking dc-dc and dc-ac converter being investigated during a temporary dc short circuit fault at low-voltage dc terminal: (a) dc voltages of the high and low dc terminals, (b) Phase 'a' line currents i_a, i_{a1} and i_{a2} measured at the ac terminals of the upper and lower sub-converters and in the grid side (primary, secondary and tertiary windings of the interfacing transformer), (c) dc link currents I_{dc1}, I_{dc2} and I_{dcx} as captured from scope screen and (d) dc link currents I_{dc1}, I_{dc2} and I_{dcx} plotted from CSV data stored in the scope in attempt to show the missing parts in (d)

VI. CONCLUSIONS

This paper presented multi-port dc-dc and dc-ac converters with multiple dc and ac terminals suitable for dc voltage matching and tapping and power conversion in a highly meshed multi-terminal dc grid, including resolution of loop flows and congestion management. Their basic operation and control were explained using two and three port examples. The presented simulation and experimental results showed that the increased control flexibility of the proposed multi-port converter could be attractive for resolving several control issues in highly complex dc grids. Experimental validation of the dc fault handing show that although the multi-port converter being studied compromises dc fault ride-through compared to isolated F2F dc/dc converters, it offers the possibilities of riding through dc faults with minimum interruption time and limited loss of power transfer.

VII. ACKNOWLEDGMENT:

This work was supported by the Australian Research Council through Discovery Projects funding scheme under Project DP150102368

VIII. APPENDIX A

Figure 11 summarises a generic block diagram of the multi-tasking dc-dc and dc-ac converter being studied in this paper. Notice that the inner controllers remains the same, while implementation of the outer controllers varies significantly according the control objective of the upper and lower sub-converters. For an example, when the high-voltage dc terminal is connected to active dc link and the low-voltage dc terminal is connected to passive dc load and ac side is connected to passive load or left unconnected, the upper sub-converter must be operated in voltage control mode to define the magnitude and frequency of the ac voltage in the ac side. Whilst the lower sub-converter must lock to ac voltage set by the upper sub-converter and set the dc voltage for the passive load connected at its dc terminal. The symbols in Figure 11 are described as follows: Vd and Vq represent d-q component of the ac voltage in the ac side; V_{dc1} and V_{dc2} are dc voltages of the high-voltage and low-voltage dc terminals; and ($i^*_{d1,2}$ and $i^*_{q1,2}$) and ($i_{d1,2}$ and $i_{q1,2}$) are reference and actual d and q currents in the ac sides of the upper and lower sub-converters. When the ac side is connected to live ac grid, one of the sub-converter could set the power exchange between the upper and lower sub-converters, and other remaining sub-converter can set the power exchange between the dc side and ac grid.

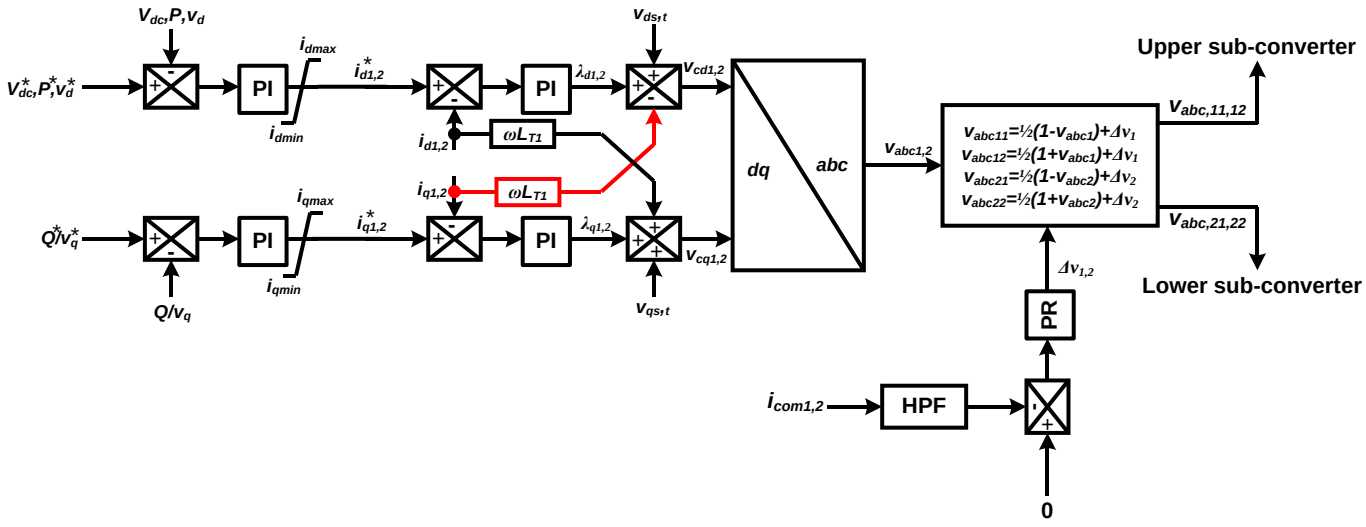


Figure 11: Block diagram summarizes control system of the multi-tasking dc-dc and dc/ac converter

IX. REFERENCES

[1]Y. Jie, H. Zhiyuan, P. Hui, and T. Guangfu, "The Hybrid-Cascaded DC–DC Converters Suitable for HVdc Applications," *Power Electronics, IEEE Transactions on*, vol. 30, pp. 5358-5363, 2015.

[2]I. A. Gowaid, G. P. Adam, B. W. Williams, A. M. Massoud, and S. Ahmed, "The transition arm multilevel converter — A concept for medium and high voltage DC-DC transformers," in *Industrial Technology (ICIT), 2015 IEEE International Conference on*, 2015, pp. 3099-3104.

[3]G. J. Kish, C. Holmes, and P. W. Lehn, "Dynamic modeling of modular multilevel DC/DC converters for HVDC systems," in *Control and Modeling for Power Electronics (COMPEL), 2014 IEEE 15th Workshop on*, 2014, pp. 1-7.

[4]T. Luth, M. M. C. Merlin, T. C. Green, F. Hassan, and C. D. Barker, "High-Frequency Operation of a DC/AC/DC System for HVDC Applications," *Power Electronics, IEEE Transactions on*, vol. 29, pp. 4107-4115, 2014.

[5]A. Schon and M. M. Bakran, "Average loss calculation and efficiency of the new HVDC auto transformer," in *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on*, 2014, pp. 1-10.

[6]A. Schon and M. M. Bakran, "High power HVDC-DC converters for the interconnection of HVDC lines with different line topologies," in *Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE-ASIA), 2014 International*, 2014, pp. 3255-3262.

[7]I. A. Gowaid, G. P. Adam, A. M. Massoud, S. Ahmed, D. Holliday, and B. W. Williams, "Quasi Two-Level Operation of Modular Multilevel Converter for Use in a High-Power DC Transformer With DC Fault Isolation Capability," *Power Electronics, IEEE Transactions on*, vol. 30, pp. 108-123, 2015.

[8]I. Gowaid, G. Adam, S. Ahmed, D. Holliday, and B. Williams, "Analysis and Design of the Modular Quasi Two-Level Converter for Medium and High Voltage Dual Active Bridge DC-DC Transformer Applications," *Power Electronics, IEEE Transactions on*, vol. PP, pp. 1-1, 2014.

[9]S. Kenzelmann, D. Dujic, F. Canales, Y. R. De Novaes, and A. Rufer, "Modular DC/DC converter: Comparison of modulation methods," in *Power Electronics and Motion Control Conference (EPE/PEMC), 2012 15th International*, 2012, pp. LS2a.1-1-LS2a.1-7.

[10] Lu, x, T. th, M. M. C. Merlin, T. C. Green, C. D. Barker, *et al.*, "Performance of a DC/AC/DC VSC system to interconnect HVDC systems," in *AC and DC Power Transmission (ACDC 2012), 10th IET International Conference on*, 2012, pp. 1-6.

[11] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer†, D. R. Critchley†, and R. W. Crookes†, "A New Hybrid Multi-Level Voltage-Source Converter with DC Fault Blocking Capability," in *IET ACDC2010*, London,UK, 2010.

[12] G. P. Adam, S. J. Finney, and B. W. Williams, "Hybrid converter with ac side cascaded H-bridge cells against H-bridge alternative arm modular multilevel converter: steady-state and dynamic performance," *Generation, Transmission & Distribution, IET,* vol. 7, 2013.

[13] A. Schon and M. M. Bakran, "A new HVDC-DC converter with inherent fault clearing capability," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, 2013, pp. 1-10.

[14] F. de Leon and J. A. Martinez, "Dual Three-Winding Transformer Equivalent Circuit Matching Leakage Measurements," *Power Delivery, IEEE Transactions on,* vol. 24, pp. 160-168, 2009.

[15] G. P. Adam and B. W. Williams, "Half and Full-Bridge Modular Multilevel Converter Models forSimulations of Full-Scale HVDC Links and Multi-terminal DC grids," *Emerging and Selected Topics in Power Electronics, IEEE Journal of,* vol. PP, pp. 1-1, 2014.

[16] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 4-17, 2015.

[17] F. B. Ajaei and R. Iravani, "Enhanced Equivalent Model of the Modular Multilevel Converter," *Power Delivery, IEEE Transactions on,* vol. PP, pp. 1-1, 2014.

[18] N. Ahmed, L. Angquist, S. Norrga, A. Antonopoulos, L. Harnefors, and H. P. Nee, "A Computationally Efficient Continuous Model for the Modular Multilevel Converter," *Emerging and Selected Topics in Power Electronics, IEEE Journal of,* vol. 2, pp. 1139-1148, 2014.