Improved Two-level Voltage Source Converter for High-Voltage Direct Current Transmission Systems

Grain Philip Adam, Ibrahim Abdelsalam, John Edward Fletcher, Lie Xu, Graeme M. Burt, Derrick Holliday and Stephen Jon Finney

***Abstract*—this paper presents an improved two-level voltage source converter for dc transmission systems with relatively low rated power and dc operating voltage. Unlike conventional two-level converter, the presented converter employs two distributed cell capacitors per three-phase; thus, do not contribute any current when converter is blocked during dc short circuit fault as in modular multilevel converter case. The use of three-phase cells is proven to be beneficial because the arm currents do not contain 2nd order harmonic currents, and cell capacitors tend to be small as they only experience high-order harmonic current associated with the switching frequency. For the same rated dc link voltage and switching devices, the rated power of the improved two-level converter will be twice that of the conventional two-level converter. Average, switching function and electromagnetic transient simulation models of the improved two-level converter are discussed and validated against detailed switch model. The viability of the improved two-level converter for HVDC applications is examined, considering dc and ac short circuit faults. Besides, reduced complexity of the control and power circuit of the improved two-level converter, it has been found that its transient responses to ac and dc faults are similar to that of the modular multilevel converter.**

***Key words*— ac and dc fault ride-through capability, high-voltage dc transmission systems, modular multilevel converter, and two-level voltage source converter.**

I. INTRODUCTION

In the last two decades, applications of voltage source converters in high-voltage dc (HVDC) transmission systems have increased significantly, particularly, for grid reinforcement of weak ac networks, and connections of offshore wind farms and oil platforms. Significant number of dc transmission systems currently operational are based on two-level and neutral-point-clamped converters, which have robust and simple power circuits, reduced complexity of the control systems, and small footprint[1, 2]. The main drawbacks of the two-level and neutral-point-clamped converters in HVDC transmission systems are [1-4]: high semiconductor losses; expose interfacing transformers to high *dv/dt*; require substantial ac filtering; and input dc link capacitors contribute large transient fault current during pole-to-pole dc short circuit fault (this makes the design of dc circuit breakers increasingly challenging).

Despite the increased power circuit and control complexity of the modular multilevel converter, its introduction to the HVDC transmission applications in the last decade has proven to be attractive for utilities for the following reasons[1-4]: reduced semiconductor losses; no ac filters should the approach that uses large number of cells per arm is adopted; the use of distributed cell capacitors instead of concentrated dc link capacitors as in two-level converter is extremely useful because it leads to substantial

reduction in the magnitude of the fault current to be interrupted by dc circuit breakers; and its low *dv/dt* due to successive switching of small voltage steps in orderly manner, allow scalability of single pole to much higher dc operating voltage such as 640kV and 800kV.

The main drawbacks of the approach that adopts large number of distribute cell capacitors in modular multilevel converter are[1-4]: large footprint; slow dynamic response due to high energy content per converter (nearly ten times that of the two-level converter)[3, 5-12]; and exponential increase in the number of measurable quantities and in the complexity of the power circuit and control systems to level never seen before in power systems, and this makes MMC susceptible to malfunctions and less attractive for HVDC links with relatively lower rated power and dc voltage (less than 300MW and ±150kV per pole). On the other hand, the complex circuit structure of the MMC has improved the availability and facilitated continued operation during internal faults (submodule failures).

Besides the MMC, there are a number of hybrid multilevel converters have been proposed that retain most of the attributes of modular multilevel converter, while reducing footprint and complexity of the power circuit. But most of these hybrid converters tend to achieve the above attributes at increased semiconductor losses, with some suffer from difficulties of current or voltage commutations[2, 13].

This paper presents an improved two-level voltage source converter (I2L-VSC) for HVDC transmission systems, with relatively low dc operating voltage and rated power (less than ±150kV and 300MW), which aimed to:

- Reduce the complexity of the control and power circuit and converter footprint compared to MMC, thanks to the use of one three-phase cell with common capacitor per three arms.
- Reduce the current stresses on dc circuit breakers as the cell capacitors do not contribute to transient component of the fault current when converter is blocked during dc short circuit faults; thus, MMC like transient response to dc short circuit fault is achieved with minimum circuit complexity[14, 15]. This means, incorporation of the proposed converter into parts of dc grid with compatible dc voltage will not significantly alter the fault level.
- Large reduction in the cell capacitance which is achieved by the adoption of the three-phase cells could result in substantial saving in converter cost and improved dynamic response.

Moreover, this paper briefly discusses the operating principle of the improved two-level converter, including the derivations of its averaged, switching function and electromagnetic transient models, and their validations against detailed switched models. Additionally, the performances of the I2L-VSC in HVDC transmission systems have been examined, considering open loop with passive loads at 50Hz and 1Hz, closed loop grid connection at different power factors and modulation indices, and ac and dc network faults using simulations and scaled-down experimentations. Results obtained from these examinations have shown that the transient responses of the proposed converter during ac and dc faults are similar to that of the conventional MMC[14, 15], which are in line with mainstream thinking that aims to reduce design requirements for dc circuit breakers and protection of dc grids. The proposed I2L-VSC should not be seen as an alternative or competitor to MMC; instead, it represents a practical compromise between the MMC and conventional two-level converter. Therefore, the I2L-VSC are expected to be applied in dc

voltage and power levels, where the circuit and control complexity of the MMC cannot be justified, but MMC like dc fault response is paramount. Some of the potential applications of the I2L-VSC are: connection of offshore oil platforms that operate with rated dc voltage and power below 200kV and 200MW, where the offshore converter is required to operate at variable ac voltage and frequency over the full operating range; and medium-voltage dc-dc converters and dc grids.

II. IMPROVED TWO-LEVEL CONVERTER AND ITS MODELLING

A) Operating Principle

Fig. 1 shows a three-phase I2L-VSC that employs only two cell capacitors instead of six capacitors proposed in [2, 15-19] or a large number of capacitors in conventional HB-MMCs[5, 20-22]. Because of the three-phase cell in upper and lower arms, the cell capacitors of the proposed converter will not be exposed to fundamental or any low-harmonic currents as in the traditional MMC with one or '*n*' half-bridge cells per arm. This allows the I2L-VSC cell capacitances to be reduced significantly. Arm inductors are needed to suppress the high frequency harmonics associated with the switching of the upper and lower cells; limit the dc inrush current due to the mismatch between the cell capacitor voltages and the input dc link voltage; limit ac current in-feed from the ac grid during dc short circuit fault; and restrain *di/dt* on the freewheeling diodes of the main switches being used to bypass the cell capacitors when the converter is blocked during dc short circuit fault. Besides its inherent natural cell capacitor voltage balance, the common-mode currents between the upper and lower arms of the same phase leg do not contain parasitic components such as 2nd order harmonic current, because the common-mode voltages of the individual phases do not contain a 2nd harmonic component to drive circulating current as in the conventional HB-MMC (assuming the converter passive parameters are properly selected). Since no modulation index is reserved for suppression of the 2nd harmonic current, the P-Q chart of the proposed converter is expected to be larger than that of the equivalent conventional MMC that actively suppresses the circulating (2nd harmonic) current[23, 24]. Because the connection points of the upper and lower arm cells are opposite (positive rail and ac poles for upper cells and ac poles and negative rail for lower cells), both upper and lower arms receive the same modulating signals and carriers to ensure that the Kirchhoff voltage law is satisfied by all three phases:

$$v_{abc1}(t) + v_{abc2}(t) \approx \psi V_{dc} \tag{1}$$

The column vectors for the switched output voltages of the upper and lower cells $v_{abc1}=[v_{a1},v_{b1},v_{c1}]^T$ and $v_{abc2}=[v_{a2},v_{b2},v_{c2}]^T$ are expressed in terms of the states of the upper switches of the six-pulse bridge converter being employed in each arm and cells capacitors as:

$$v_{abc1}(t) = \left[(1-s_{a1}(t))V_{c1} \quad (1-s_{b1}(t))V_{c1} \quad (1-s_{c1}(t))V_{c1}\right]^T \tag{2}$$

$$v_{abc2}(t) = \left[s_{a2}(t)V_{c2} \quad s_{b2}(t)V_{c2} \quad s_{c2}(t)V_{c2}\right]^T \tag{3}$$

where $\Psi=[1\ 1\ 1]^T$; $s_{abc}=[s_{a1}(t), s_{b1}(t), s_{c1}(t)]$ and $s_{abc}=[s_{a2}(t), s_{b2}(t), s_{c2}(t)]$ are switching functions of the upper switches of the upper and lower cells of the I2L-VSC in Fig. 1(a). The switching function $s_{xj}(t)$ varies between 1 and 0 (where $x=a$, b and c, and $j=1$ and 2), with '1' and '0' stand for on and off states of the switching devices S_{a1}, S_{b1} and S_{c1} and S_{a2}, S_{b2} and S_{c2}. As stated in (1), correct operation of the I2L-VSC requires upper and lower arms of the same phase-leg must be operated in complementary manner (this

means, insertion of the upper cell capacitor into power path requires the lower cell capacitor of the same phase-leg to be bypassed and vice versa). Therefore, this necessitates each cell capacitor and composite switching devices to be rated at the full dc link voltage (V_{dc}). The I2L-VSC generates only two output voltage levels per phase as in the conventional two-level converter. The three-phase output voltages of the I2L-VSC represent the differential mode voltages as in the conventional MMC:

$$v_{abco}(t) = v_{abc1}(t) - v_{abc2}(t) \tag{4}$$

Similarly, the common-mode voltages are:

$$v_{com}(t) = \tfrac{1}{2}(v_{abc1}(t) + v_{abc2}(t)) \tag{5}$$

Each cell of the I2L-VSC adheres to the same operational restrictions of the conventional two-level converter such as:

- Complementary operation of the switching devices of the same leg in order to prevent shoot-through at the cell level ($s_{a1,2}(t) + \bar{s}_{a1,2}(t) = 1$, $s_{b1,2}(t) + \bar{s}_{b1,2}(t) = 1$ and $s_{c1,2}(t) + \bar{s}_{c1,2}(t) = 1$).
- Each switching device and cell capacitor must be rated to block the full dc link voltage (V_{dc}). Therefore, for HVDC applications, series connection of switching devices is necessary to enable operation at dc operating voltage suitable for distribution and transmission systems.

Although the output voltage quality remains the same as in conventional two-level converter, the proposed structure provides a viable method for increasing the capacity of HVDC converters without the need to increase the rated dc link voltage. With the three-phase modulating signals being defined as $m_{abc}(t) = \left[M\sin\omega t \quad M\sin(\omega t + \tfrac{4}{3}\pi) \quad M\sin(\omega t + \tfrac{2}{3}\pi)\right]^T$, the switched output voltages in (2) and (3) could be replaced by their average values as:

$$\tilde{v}_{abc1}(t) = \left[\tfrac{1}{2}V_{c1}(t)(1 - m_a(t)) \quad \tfrac{1}{2}V_{c1}(t)(1 - m_b(t)) \quad \tfrac{1}{2}V_{c1}(t)(1 - m_c(t))\right]^T \tag{6}$$

$$\tilde{v}_{abc2}(t) = \left[\tfrac{1}{2}V_{c2}(t)(1 + m_a(t)) \quad \tfrac{1}{2}V_{c2}(t)(1 + m_b(t)) \quad \tfrac{1}{2}V_{c2}(t)(1 + m_c(t))\right]^T \tag{7}$$

Besides sinusoidal pulse width modulation (SPWM), I2L-VSC could be control using space vector modulation (SVM) or selective harmonic elimination (SHE), with SHE reducing the switching frequency per devices considerably as demonstrated in [25]; hence, a substantial reduction in switching losses.

B) ***Converter Modelling***

Considering the upper and lower cells in Fig. 1, the dynamics of the upper and lower cell capacitor voltages in switched forms are:

$$dV_{c1}(t)/dt = \bar{s}^T_{abc1}(t) i_{abc1}(t)/C \tag{8}$$

$$dV_{c2}(t)/dt = s^T_{abc2}(t) i_{abc2}(t)/C \tag{9}$$

The average effect of the cell capacitor voltage dynamics could be expressed as:

$$dV_{c1}(t)/dt = \bar{d}^T_{abc1}(t) i_{abc1}(t))/C \tag{10}$$

$$dV_{c2}(t)/dt = d^T_{abc2}(t) i_{abc2}(t)/C \tag{11}$$

where $i_{abc1}(t) \approx I_d + \frac{1}{2} I_m \sin(\omega t + \gamma_{abc} + \varphi)$, $i_{abc2}(t) \approx I_d - \frac{1}{2} I_m \sin(\omega t + \gamma_{abc} + \varphi)$, $I_d \approx \frac{1}{3} I_{dc}$, $\gamma_{abc} = \begin{bmatrix} 0 & \frac{4}{3}\pi & \frac{2}{3}\pi \end{bmatrix}$

$\bar{d}_{abc1}(t) = \begin{bmatrix} \frac{1}{2}(1-m_a(t)) & \frac{1}{2}(1-m_b(t)) & \frac{1}{2}(1-m_c(t)) \end{bmatrix}$ and $d_{abc2}(t) = \begin{bmatrix} \frac{1}{2}(1+m_a(t)) & \frac{1}{2}(1+m_b(t)) & \frac{1}{2}(1+m_c(t)) \end{bmatrix}$.

From the above equations, the terms $d^T_{abc1}(t) i_{abc1}(t) = 0$ and $d^T_{abc2}(t) i_{abc2}(t) = 0$, which indicate the natural balancing of the cell capacitors, with no low frequency oscillations in the cell capacitor voltages as in conventional one cell or n-cell MMC cases. Considering the two loops between upper and lower arms and imaginary supply mid-point, the MMC arm dynamics are:

$$\tfrac{1}{2}\psi V_{dc} - v_{abc1}(t) - R_s i_{abc1}(t) - L_s \, di_{abc1}(t)/dt - v_{abco}(t) = 0 \tag{12}$$

$$\tfrac{1}{2}\psi V_{dc} - v_{abc2}(t) - R_s i_{abc2}(t) - L_s \, di_{abc2}(t)/dt - v_{abco}(t) = 0 \tag{13}$$

Fig. 1(b) and (c) show an averaged and switching function models of the proposed converter, constructed from the equations that describe the dynamics of the cell capacitor voltages and arm currents. Combining the equations $v_{abco}(t) = R_T i_{abc}(t) - L_T \, di_{abc}(t)/dt - v_{abc}(t)$, and $i_{abco}(t) = i_{abc1}(t) - i_{abc2}(t)$ with that of the upper and lower arms, the following equations are obtained:

$$L_x \, di_{abco}(t)/dt + R_x i_{abco}(t) = \tfrac{1}{2} m_{abc}(t) \bar{V}_c - v_{abc}(t) \tag{14}$$

$$L_s \, di_d(t)/dt + R_s i_d(t) = \tfrac{1}{2}(V_{dc} - \bar{V}_c) \tag{15}$$

where $L_x = \frac{1}{2} L_s + L_T$, $R_x = \frac{1}{2} R_s + R_T$ and assuming that the cell capacitor voltage ripples are ignored ($V_{c1}(t) \approx V_{c2}(t) \approx \bar{V}_c$).

Fig. 2 depicts electromagnetic transient models of the upper and lower arms of the improved two-level converter and their interfacing to the power circuit. In this mode, all IGBTs are replaced by switched resistors and upper and lower arm cell capacitors described by their Thevenin equivalent based on backward Euler:

$$V_{c1}(t) = V_{c1}(t - \Delta t) + \frac{\Delta t}{C_m} I_{c1}(t) \tag{16}$$

$$V_{c2}(t) = V_{c2}(t - \Delta t) + \frac{\Delta t}{C_m} I_{c2}(t) \tag{17}$$

where, $R_{c1} = R_{c2} = \Delta t / C_m$ represent Dommel equivalent resistors [2, 26-35]. From Fig. 2(a) and (b), the capacitor currents of the upper and lower cell capacitors at present time step are calculated from the arm currents and capacitor voltages at previous time step (history terms) as:

$$I_{c1}(t) = \left[\alpha_{a1} i_{a1}(t - \Delta t) + \alpha_{b1} i_{b1}(t - \Delta t) + \alpha_{c1} i_{c1}(t - \Delta t) - G_1 V_{c1}(t - \Delta t)\right] / (1 + R_{c1} G_1) \tag{18}$$

$$I_{c2}(t) = \left[\alpha_{a2} i_{a2}(t - \Delta t) + \alpha_{b2} i_{b2}(t - \Delta t) + \alpha_{c2} i_{c2}(t - \Delta t) - G_2 V_{c2}(t - \Delta t)\right] / (1 + R_{c2} G_2) \tag{19}$$

Where, $\alpha_{a1} = R_{A11}/(R_{A11} + R_{A12})$, $\alpha_{b1} = R_{B11}/(R_{B11} + R_{B12})$, $\alpha_{c1} = R_{C11}/(R_{C11} + R_{C12})$, $\alpha_{a2} = R_{A21}/(R_{A22} + R_{A22})$, $\alpha_{b2} = R_{B21}/(R_{B21} + R_{B22})$, $\alpha_{c1} = R_{C11}/(R_{C11} + R_{C12})$, $G_1 = 1/(R_{A11} + R_{A12}) + 1/(R_{B11} + R_{B12}) + 1/(R_{C11} + R_{C12})$ and $G_2 = 1/(R_{A21} + R_{A22}) + 1/(R_{B21} + R_{B22}) + 1/(R_{C21} + R_{C22})$.

Similarly, the terminal voltages of the upper and lower cells relative to positive and negative dc link nodes are:

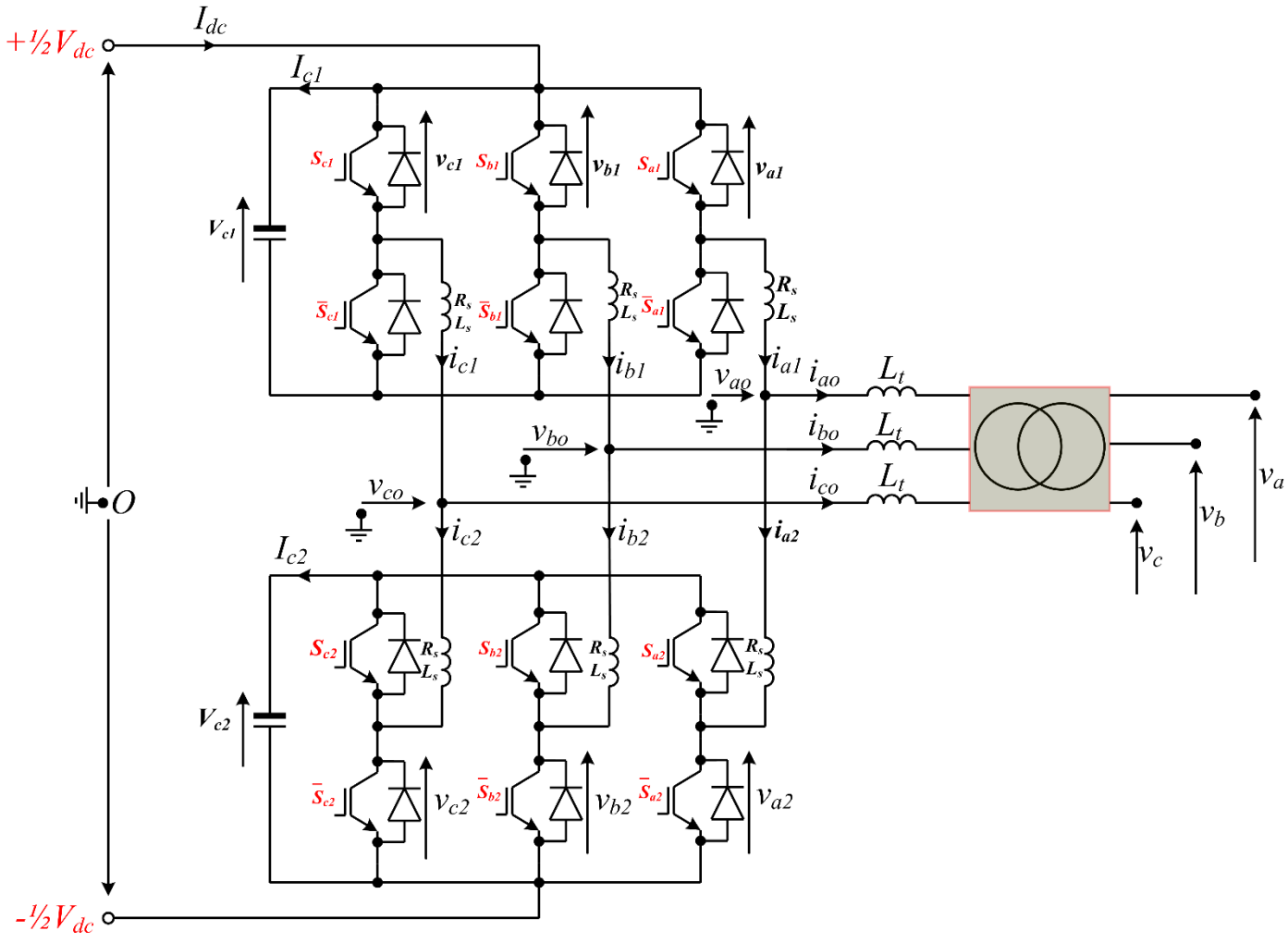
$$
\begin{aligned}
v_{a1}(t) &= V_{c1}(t) \times R_{A11} / (R_{A11} + R_{A12}) \\
v_{b1}(t) &= V_{c1}(t) \times R_{B11} / (R_{B11} + R_{B12}) \\
v_{c1}(t) &= V_{c1}(t) \times R_{C11} / (R_{C11} + R_{C12})
\end{aligned} \tag{20}
$$

$$
\begin{aligned}
v_{a2}(t) &= V_{c2}(t) \times R_{A22} / (R_{A21} + R_{A22}) \\
v_{b2}(t) &= V_{c2}(t) \times R_{B22} / (R_{B21} + R_{B22}) \\
v_{c2}(t) &= V_{c2}(t) \times R_{C22} / (R_{C21} + R_{C22})
\end{aligned} \tag{21}
$$

The terminal voltages calculated from (20) and (21) at each time step are fed to the controlled voltage sources of the power circuit in Fig. 2.

III. VALIDATION OF THE OF THE IMPROVED TWO-LEVEL CONVERTER MODELS AGAINST SWITCH MODEL

Fig. 3 presents simulation waveforms that validate the averaged, switching function and electromagnetic transient simulation models of the I2L-VSC presented in section II, considering open loop case with parameters depicted in Fig. 3. The plots for the output phase currents, upper and lower arm currents, cell capacitor voltages from the averaged, switching function and electromagnetic transient simulation models in Fig. 3 (a), (b), (c) and (d) indicate that these models are able to reproduce identical results as the detailed switch model (including during steady-state and transient due to change of modulation index from 0.5 to 0.95), even though the average model neglects the high frequency switching transients. Detailed switch model refers to the model that employs universal bridge from Matlab-SimPower system library, where each switching device is mimicking the conduction pattern of typical IGBT plus anti-parallel diode. Fig. 3 (e) shows the switched output phase voltage obtained from the switching function and electromagnetic transient simulation models superimposed on that of the detailed switch model. Observe that the three models produce practically identical results to microscopic level. From the plots in Fig. 3, it can be concluded that the presented average, switching function, and electromagnetic transient simulation models are good representation of the I2L-VSC. These models in their present forms could be applied to simulation detailed behaviour of the I2L-VSC during normal and abnormal operation, including symmetrical and asymmetrical ac fault of grid connected inverters and HVDC links. However, minor software overhead or modification of the power circuit (inclusion of additional IGBT and diode to each arm) are necessary to make the presented models applicable to dc fault studies.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Sa1
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vao
iao
Lt
vbo
ibo
vco
ico
O
ic2
ib2
ia2
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vc
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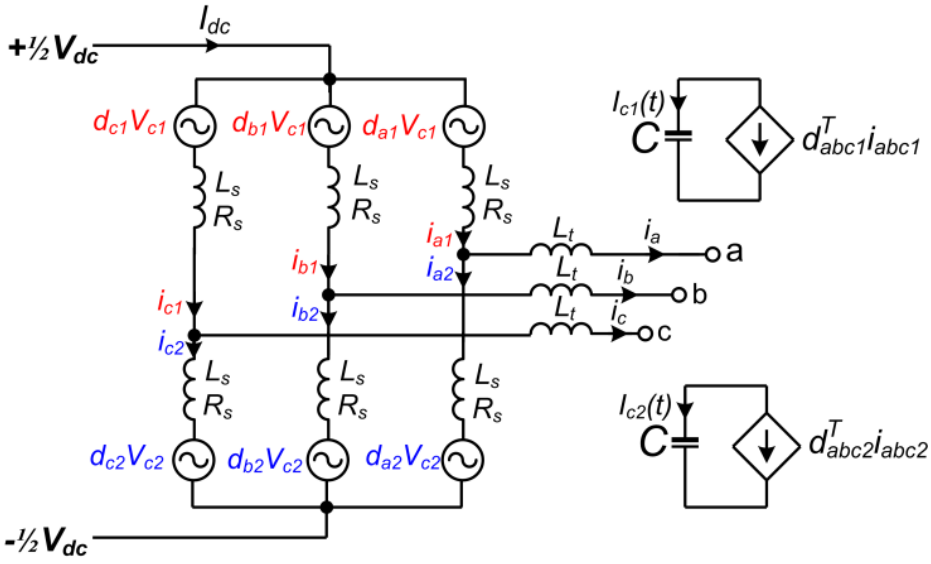
Sb2
Sa2
Vc2
vc2
vb2
va2
-½Vdc

(a)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Rs
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ib1
ic1
ic2
Lt
ia
ib
ic
a
b
c
Ic1(t)
C
dTabc1iabc1
dc2Vc2
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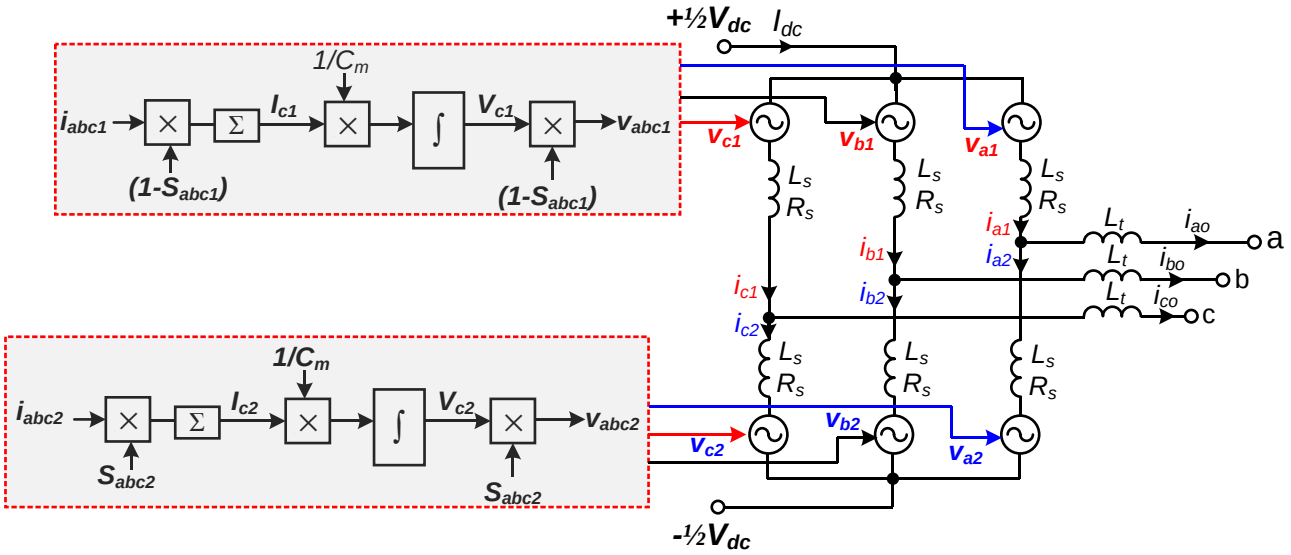
Ic2(t)
dTabc2iabc2
-½Vdc

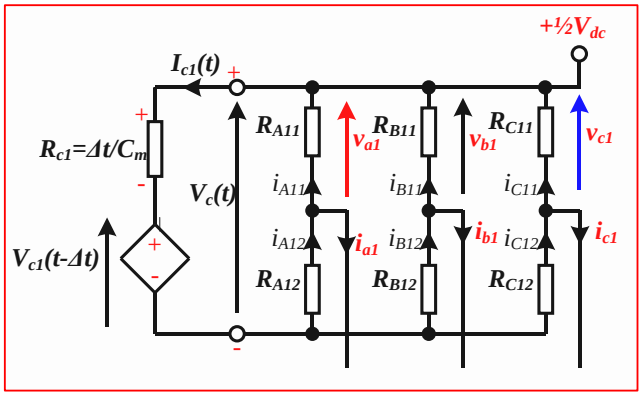
(b) [LX1]

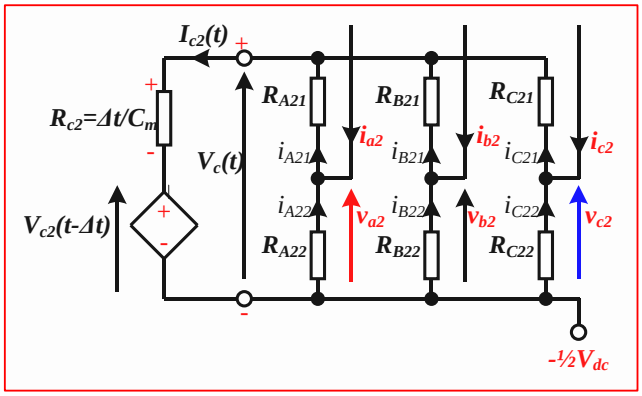


(c)

Fig. 1: (a) The proposed modular level converter with common cell capacitor for three-phases, (b) its averaged model and (c) its switching function model

Electromagnetic transient representation of the upper cell





Electromagnetic transient representation of the lower cell

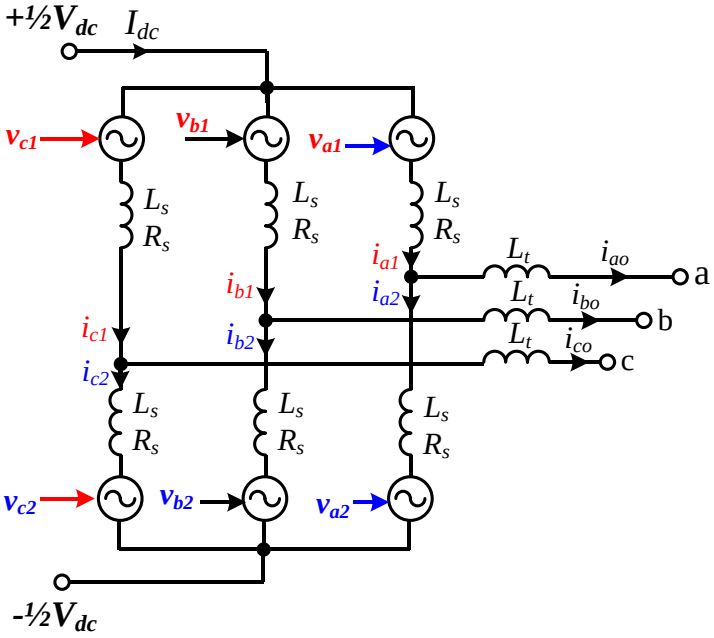
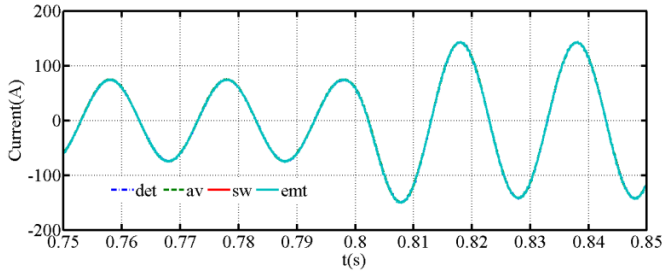
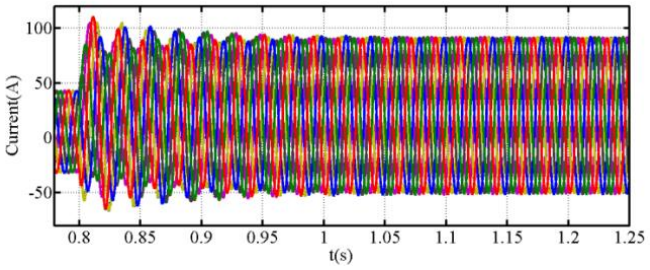


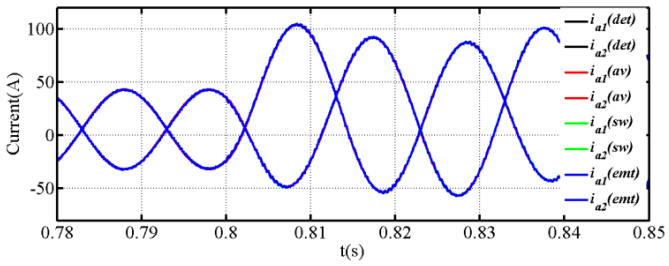
Fig. 2: Electromagnetic transient simulation equivalent of the upper and lower cells, including illustration of their interfacing to the power circuit using controlled voltage source



(a)-



(b)-



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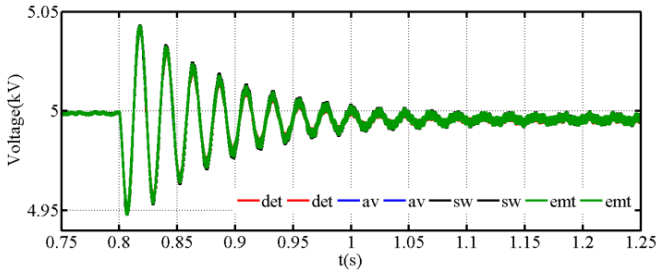
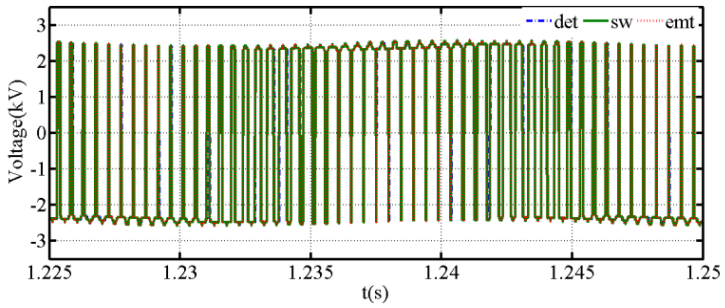


(d)-



(e)-

Fig. 3: Open loop validation of the averaged, switching function and electromagnetic transient simulation models of the improved two-level converter against detailed switch model (V_{dc}=5kV, 2.1kHz carrier frequency, 2mF cell capacitance, 5mH arm inductance, load resistance and inductance are 10Ω and 40mH, and step change in modulation index from 0.5 to 0.95): (a) Phase 'a' load currents of the four models (detailed, average, switch and EMTP models),(b) Upper and lower arm currents (detailed, average, switch and EMTP models), (c) Phase 'a' upper and lower arm currents (detailed, average, switch and EMTP models superimposed on each other), (d) Upper and lower cell capacitors (detailed, average, switch and EMTP models) and (e) Pre-filter output phase voltage (v_{ao}) measured relative to ground (detailed, switching function and EMTP models).

IV. TEST SYSTEMS

Fig. 4 shows a two-terminal symmetrical monopole HVDC link that employs the proposed I2L-VSC. System parameters are displayed in Fig. 4 and listed in Table I. Converter terminals VSC_1 and VSC_2 regulate active power and dc link voltage respectively, and ac voltage at B_1 and B_2. Both converter terminals use two double tuned ac filters, targeted at 1st carrier frequency and dominant sidebands around the 1st and 2nd carrier frequencies, with the total filtering per converter is about 30% of the converter rating.

Table I: system parameters

Rated dc voltage	200kV (±100kV)
VSC_1 and VSC_2 rated apparent power	200MVA
VSC_1 and VSC_2 rated active power	180MW
VSC_1 and VSC_2 rated reactive power	±90MVAr
VSC_1 and VSC_2 rated ac voltage	100kV
Arm inductor (L_s)	10mH
Cell capacitance	100μF
Inductance of interfacing reactor	0.15pu

Transformer leakage inductance	0.1pu
Transformer rated power	200MVA
Transformer nominal voltage ratio	100kV/400kV
DC cable resistance	9mΩ/km
DC cable inductance	1.4mH/km
DC cable capacitance	0.26μF/km

V. SIMULATIONS

Fig. 5 shows simulations waveforms when the active power regulator (VSC_1) of the HVDC link in Fig. 4 is commanded at *t=0.4s* to ramp its active power output from 0 to 160MW, and at *t=1s*, the system is subjected to a permanent pole-to-pole dc short circuit fault at the middle of the link. Fig. 5 (a), (b), (c) and (d) display three-phase ac currents VSC_1 and VSC_2 inject into B_1 and B_2, and respective arm currents. Observe that during normal operation and dc fault, the upper and lower arm currents are similar to that of the conventional modular[LX2], but the common-mode components of the arm currents do not contain any circulating currents (see Fig. 5 (e)). Moreover, during dc short circuit fault the routes of the in-feed current in the blocked converter are similar to that of the conventional MMC (freewheeling diodes of the upper switches in the upper arms, and the opposite in the lower arms). Fig. 5 (e) and (f) show that the common-mode current of each phase-leg of the improved two-level converter is practically pure dc and represents one third of the dc link current during normal operation and dc fault. Additionally, the plots for the arms and common-mode currents, and dc link current displayed in Fig. 5 (c) to (f) indicate that these currents are dominated by the ac grid contribution (steady-state component of the dc fault current), thanks to the concept of distributed capacitors. Unlike the conventional MMC, the cell capacitor voltages of the improved two-level converter do not exhibit any low frequency oscillations, thanks to the use of single capacitor per three phases in each arm (see Fig. 5 (g) and (h)). Also, the magnitudes of high-frequency oscillations seen on the cell capacitors are much smaller, and could allow the use of much smaller arm inductances in other application; however, in HVDC applications being considered here, the arm inductance is selected, taking into account its contribution to dc fault current limiting and di/dt on the freewheeling diodes. Fig. 5(i) shows positive and negative pole to-ground dc voltages measured at the terminals of VSC_1. Despite the high loss concern of the two-level converter, the above discussions show that the improved two-level converter can be used as in point-to-point where the two-level converter offers the best overall trade-off compared to MMC, and in parts of the multi-terminal HVDC network that would be operated at relatively low dc operation voltage and power.

Fig. 6 presents selected simulation waveforms for the improved two-level converter when it is subjected to a temporary symmetrical three-phase ac fault at B_1 for period of 200ms, and VSC_1 reduces its active power injection into B_1 to zero when fault is detected at t=1s. Fig. 6 (a), (b), (c) and (d) show ac voltage at B_1, VSC_1 output current measured at the interfacing inductor, VSC_1 upper and lower arm currents, and VSC_1 common-mode currents of the three phases. Fig. 6 (e) and (f) show VSC1 cell capacitor voltages and its positive and negative pole dc link voltages. Observe that the response of the improved two-level converter to three-phase ac fault is similar to that of the conventional MMC with large number of cells[36]. With 100μF cell capacitance (10ms), the cell capacitor voltages and positive and negative pole dc voltages exhibit limited overshoots around 17.5% during ac fault. This shows

that the substantial reduction achieved in the cell capacitance or energy content of the improved two-level converter compared to MMC did not significantly compromise converter operation.

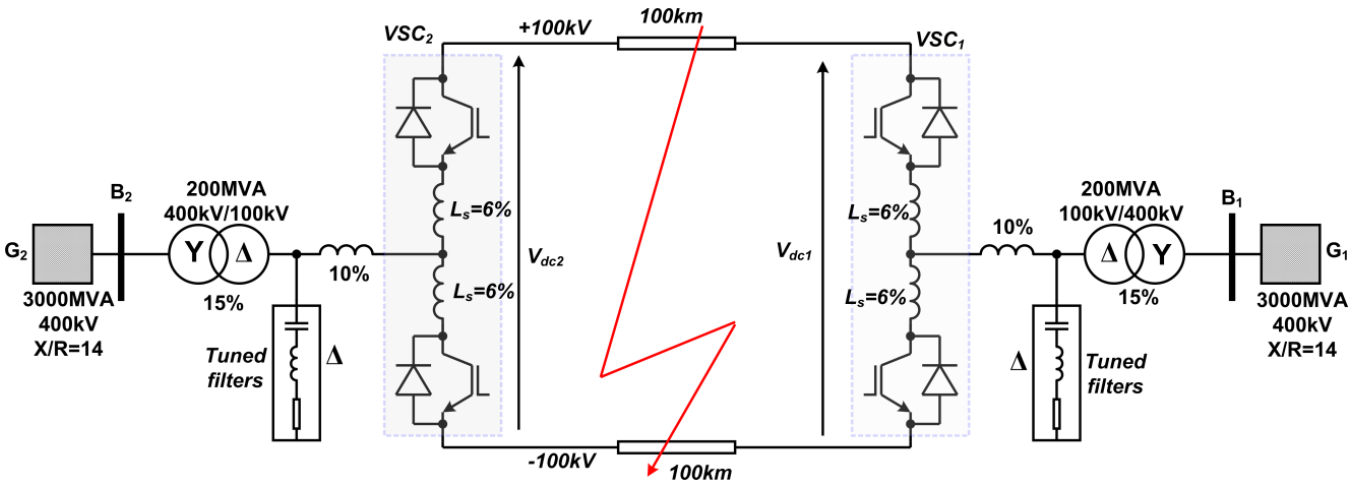
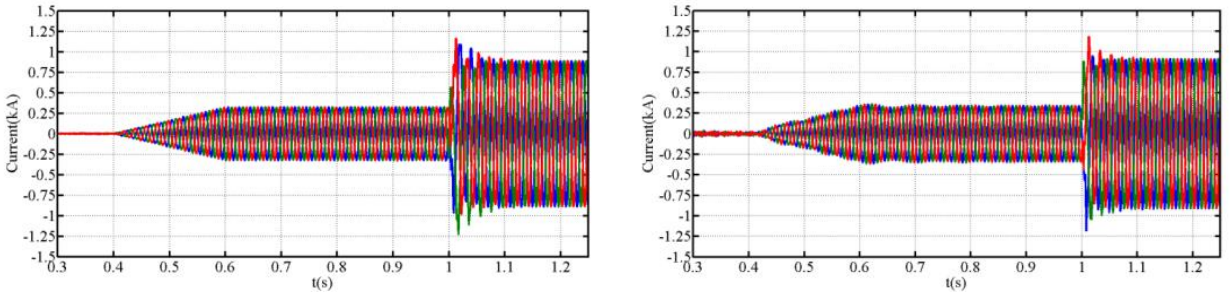
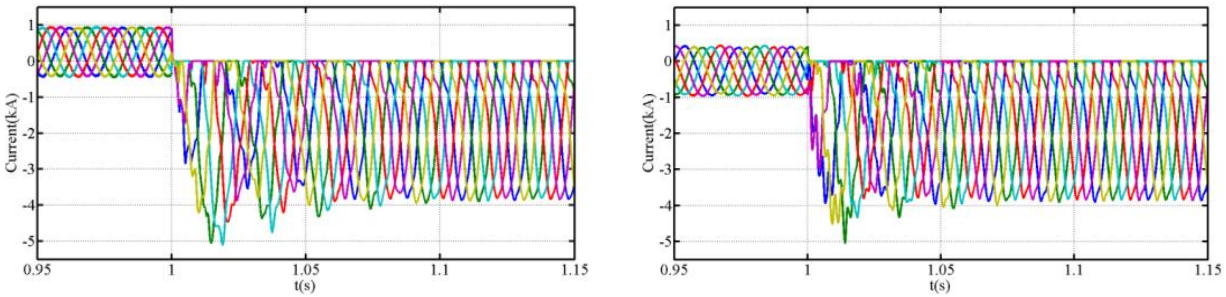


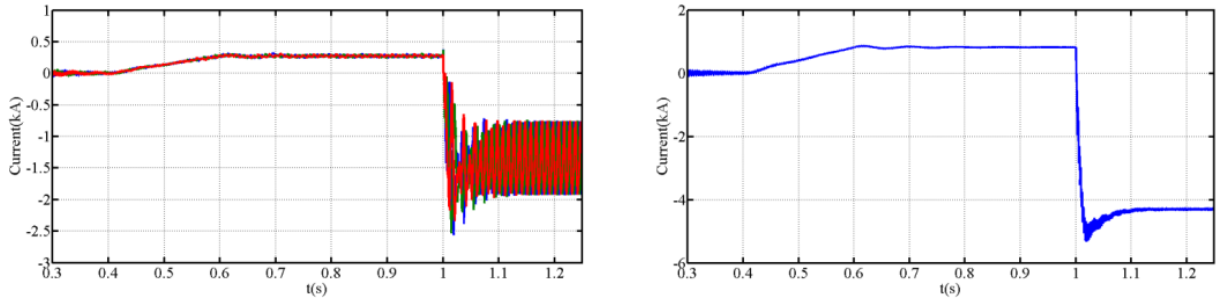
Fig. 4: Two-terminal symmetrical monopolar HVDC link that employs improved two-level converters at VSC_1 and VSC_2



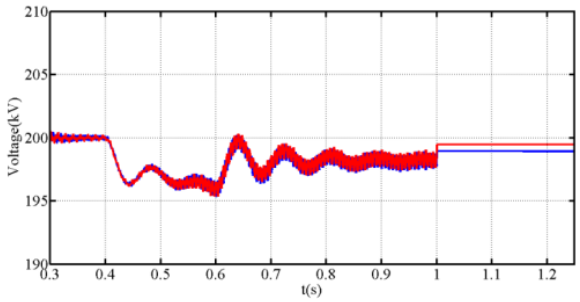
(a) (b)



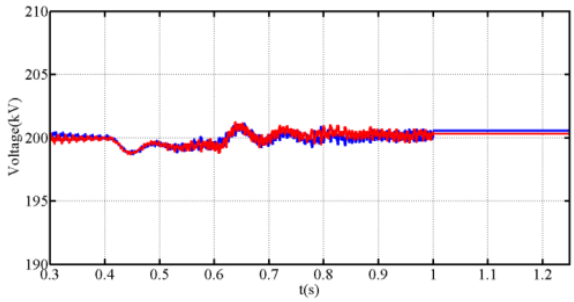
(c) (d)



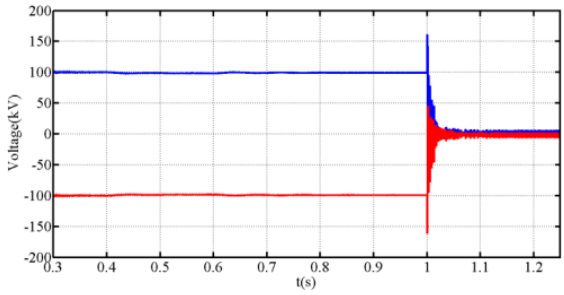
(e) (f)



(g)

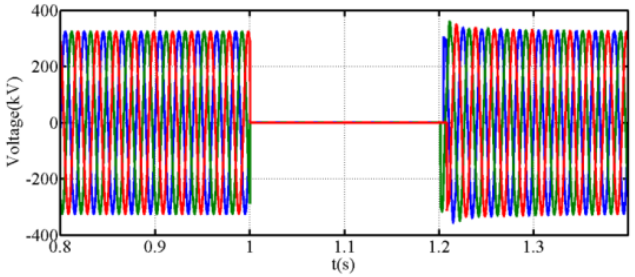


(h)

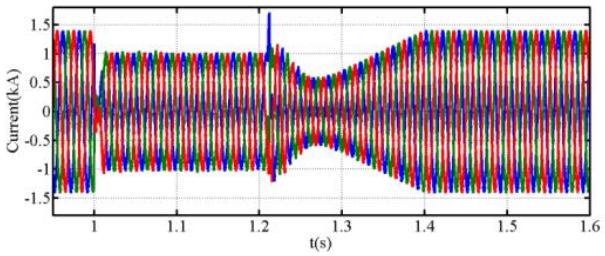


(i)

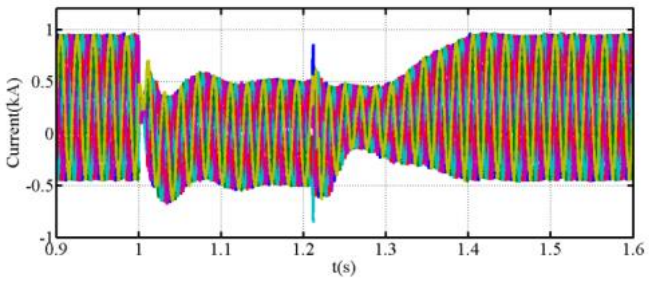
Fig. 5: Waveforms illustrate the response of the improved two-level converter during dc short circuit fault: (a) three-phase currents at B_1, (b) Three-phase currents at B_2, (c) VSC_1 upper and lower arm currents, (d) VSC_2 upper and lower arm currents, (e) Sample of the common-mode current measured at VSC_1, $i_{com}^{abc} = \frac{1}{2}(i_{abc1} + i_{abc2})$, (f) DC link current measure at the terminal of VSC_1, (g) VSC_1 upper and lower capacitor voltages, (h) VSC_2 upper and lower capacitor voltages and (i) Sample of the converter dc link voltage measured at the terminals of VSC_1



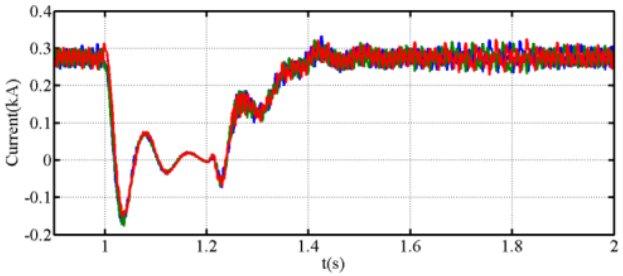
(a)



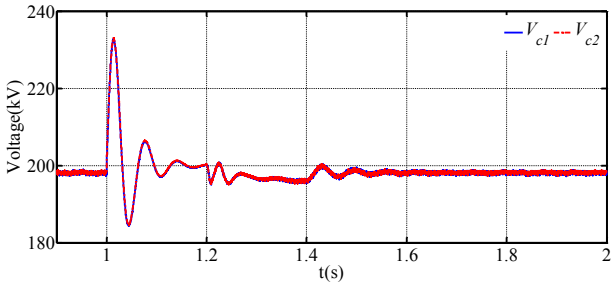
(b)

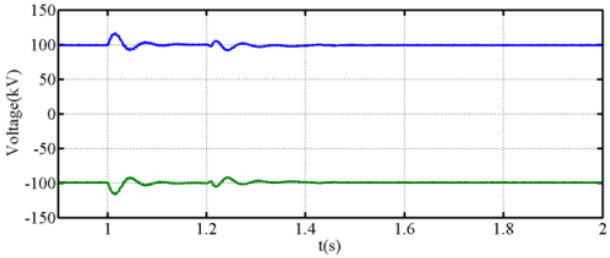


(c)



(d)





(f)

(e)

Fig. 6: Simulation waveforms that illustrate the response of the improved two-level converter to symmetrical ac fault: (a) Three-phase ac voltages measured at B_1, (b) Pre-filter three-phase ac currents measured in the interfacing inductor of VSC_1, (c) VSC_1 upper and lower arm currents, (d) VSC_1 common-mode currents, (e) VSC_1 upper and lower cell capacitor voltages and (f) VSC_1 positive and negative dc link voltages

VI. COMPARISON BETWEEN THE CONVENTIONAL AND IMPROVED TWO-LEVEL CONVERTERS

Fig. 7 presents a comparison between the improved and conventional two-level converters when both are simulated as point-to-point HVDC link in Fig. 4, using parameters in Table I and exposed to the same pole-to-pole dc short circuit studied in Fig. 5. To ensure that both converters have the same inertia (stored capacitor energy) and dc current ripples, the dc link capacitance of the conventional two-level converter is set to be twice of the improved two-level converter shown in Table I.

Fig. 7(a) displays three-phase currents of the I2L-VSC (continuous lines) superimposed on that of the conventional two-level converter (doted lines), all measured at the interfacing reactors which are connected between converter terminals and low-voltage windings of the interfacing transformer. The plots in Fig. 7(a) indicate that the conventional two-level converter draws larger currents than its improved version, which is in line with the above discussions. The plots for the dc link current measured at the dc terminal of the active power regulator (VSC_1) in Fig. 7(b) show the conventional two-level converter contributes larger transient current to dc fault than the I2L-VSC, and this is due to discharge of its dc link capacitor. But due to the small residual dc voltage across the dc link capacitors of the conventional two-level converter, it has slightly lower steady-state dc fault current than the I2L-VSC (recall the latter does not use dc link capacitor across the dc link). Fig. 7(c) displays the current in the switch S_{a1} of the upper cell of the I2L-VSC. Notice that the steady-state peak current of the switch S_{a1} is equal to that of the arm currents ($\frac{1}{3}I_{dc}+\frac{1}{2}I_m$), where I_{dc} and I_m are the dc link current and peak of the output current. Fig. 7(d) shows the current in the switch S_{a1} (phase '*a*' upper arm of the conventional two-level converter). Observe that the switch S_{a1} in the conventional two-level converter is exposed to the peak of the converter output current (I_m) during steady-state which is higher than that of the I2L-VSC, and its diodes are exposed to higher transient currents during a dc fault compared to that of the I2L-VSC. When I2L-VSC is blocked during pole-to-pole dc short circuit faults, the ac in-feed currents from ac to dc side flow through the diodes of the upper switches (S_{a1}, S_{b1} and S_{c1}) in the upper arms, and diodes of lower switches in the lower arms, Fig. 7(e) and (f).

From the above discussions and results in Fig. 7, the following conclusions are drawn:

- The I2L-VSC has better transient response to pole-to-pole dc short circuit faults than the conventional two-level converter, see Fig. 7(a) and (b).
- For the same rated power, dc link voltage and ac side voltage, the I2L-VSC can use switching devices with lower rated current than the conventional two-level converter, see Fig. 7(c) and (d).
- The dc fault currents in the freewheeling diodes of the conventional two-level converter rise at slower rate than that of the I2L-VSC (as the residual dc voltages across its dc link capacitors do not fall instantly to nearly zero), see Fig. 7(e).

To illustrate the power density of the I2L-VSC compared to the conventional two-level converter when both converters employ switching devices of similar current and voltage ratings, it assumes that the output phase current of phase '*a*' is $i_{a0}=I_m sin(\omega t+\varphi)$. Therefore, the upper and lower arm currents of the I2L-VSC will be $i_{a1}=I_d+\frac{1}{2}I_m sin(\omega t+\varphi)$ and $i_{a2}=I_d-\frac{1}{2}I_m sin(\omega t+\varphi)$; where, $I_d=\frac{1}{3}I_{dc}$, and I_m and I_{dc} represent the peak of the output phase currents and magnitude of the dc link current. Also, recall that the I_d could be expressed as $I_d=\frac{1}{4}mI_m cos\varphi$[37], where, m and φ are modulation index and power factor angle. On the other hand, the peak arm current for the conventional two-level converter is the same as that of the output phase currents. However, the peak arm currents of the I2L-VSC vary significantly with power factor. For example, the arm currents at zero and unity power factor boundary conditions are:

- At zero power factor, $I_d=0$, thus, $i_{a1}=+\frac{1}{2}I_m sin(\omega t+\varphi)$ and $i_{a2}=-\frac{1}{2}I_m sin(\omega t+\varphi)$. This feature could be exploited to expand the P-Q envelope of the I2L-VSC, particularly, in the current limit parts of the under excitation region, where converter reactive power output is limited by the current rating of the switching devices. In this region, reactive power capability of the I2L-VSC can be extended to up to double the rated apparent power of the conventional two-level converter, without overstressing the switching devices.
- At unity power factor and unity modulation index, the arm currents of the I2L-VSC are $i_{a1}=\frac{1}{2}I_m(\frac{1}{2}+sin(\omega t+\varphi))$ and $i_{a2}=\frac{1}{2}I_m(\frac{1}{2}-sin(\omega t+\varphi))$. These arm currents' expressions indicate that the I2L-VSC are capable of generating more active power compared to the conventional two-level converter, without overstressing its switching devices).

To substantiate the above discussions, selected waveforms that illustrate the case of zero power factor with I2L-VSC exchanges twice the rated apparent power of the two-level converter are presented in Fig. 8 and Fig. 9. The plots in Fig. 8 (a), (b) and (c) and Fig. 9 (a), (b) and (c) confirm the above discussions, with arm currents of both converters being compared have similar peak currents even though I2L-VSC exchanges twice reactive power of the conventional two-level converter.

Additional waveforms that compare the response of the conventional and improved two-level converters during power reversal are shown in Fig. 10. These waveforms show both converters being compared have similarly responses.

Table II presents semiconductor loss comparison between the conventional and improved two-level converters, using system parameters summarised in Table I, and 1200A, 2.5kV IGBT(T1200TD25A) from West-code, assuming that the voltage stress per switch is 1.250kV. On-state and switching losses of the conventional and improved two-level converter are calculated based on the approach presented in [38-42], with some modification introduced to accommodate the asymmetry of the arm currents in the improved two-level converter as suggested in [15]. The accuracy of the analytical on-state losses in Table II is confirmed using MATLAB simulation, where the average and RMS currents are calculated directly from the simulation. It has been found that the margin of error between the two results is less than 1%. The switching losses are calculated assuming that the turn-on and turn-off energy losses are linear combination of device current at the turn on and turn off instances [43]. Table II shows that the improved two-level converter has lower on-state and switching losses compared to the conventional two-level converter, benefiting from even split of the fundamental output ac current between the upper and lower arms of each phase-leg. Notice that the semiconductor losses in Table II are obtained when switching frequency is 2.1kHz, and since these losses are predominantly switching losses, the

overall semiconductor loss for the improved two-level converter could be reduced drastically by adopting selective harmonic elimination with lower equivalent switching frequency of 1.15kHz as employed in the conventional two-level converter of the Estlink HVDC link[44].

Table III presents global comparison of the attributes and limitations of the improved two-level converter with respect to the conventional two-level converter and modular multilevel converter.

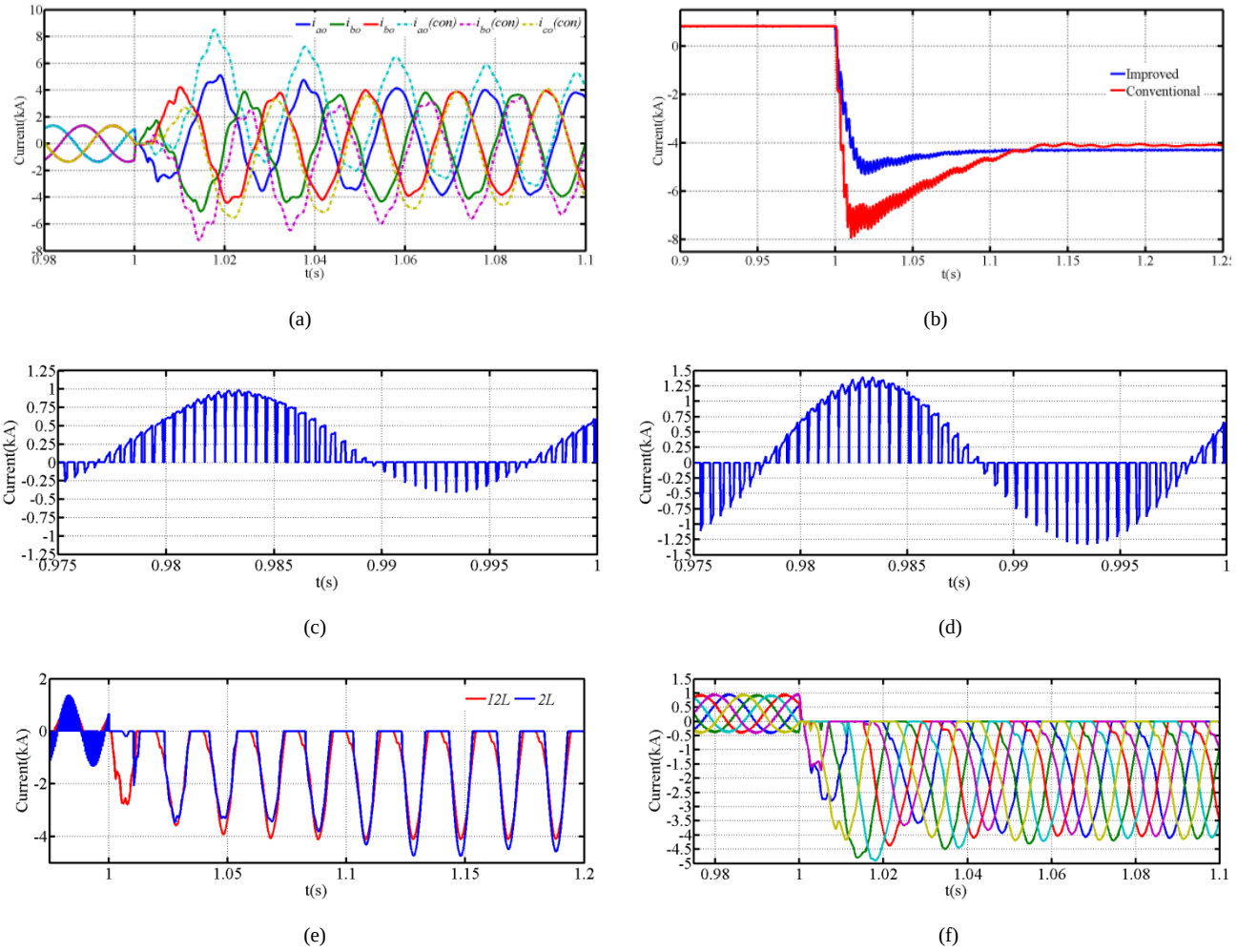
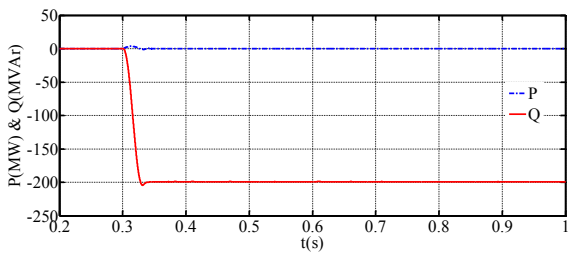
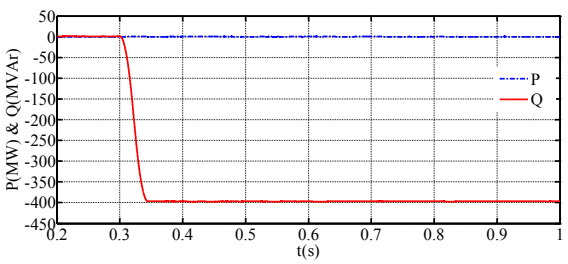


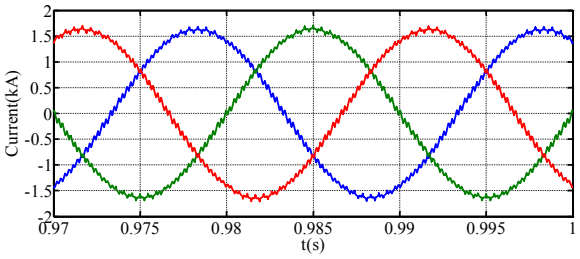
Fig. 7: Selected waveforms illustrate one-to-one comparison of the responses of the proposed I2L-VSC against that of the conventional two-level converter during pole-to-pole dc short circuit fault: (a) three-phase currents measured at the interfacing reactors of the I2L-VSC superimposed on that of the conventional two-level converter; (b) dc link current measured at the terminal of the VSC_1 which is modelled as an I2L-VSC superimposed on that of the conventional two-level converter; (c) current waveform in the switch S_{a1} of the I2L-VSC, measured during steady-state; (d) current waveform in the switch S_{a1} of the conventional two-level VSC, measured during steady-state (which represents phase 'a' upper arm current); (e) current waveform in the switch S_{a1} of the I2L converter superimposed on that of the conventional two-level converter; and (f) six arm currents of the I2L-VSC



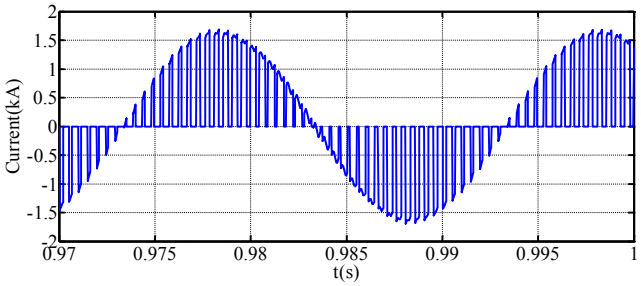
(a) VSC_1 active and reactive powers



(a) VSC1 active and reactive powers

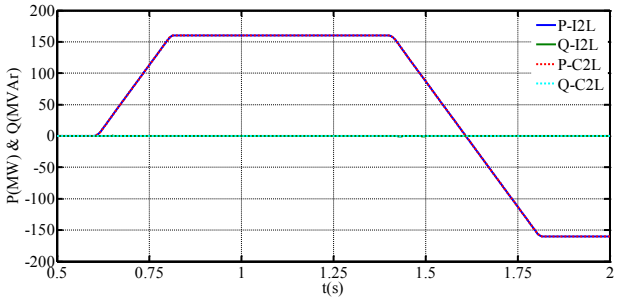


(b) VSC_1 three-phase output currents measured at converter side (low-voltage side of the interfacing transformer)

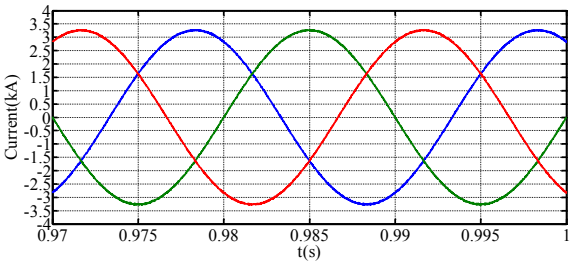


(c) Sample of the current in the upper arm of the phase a

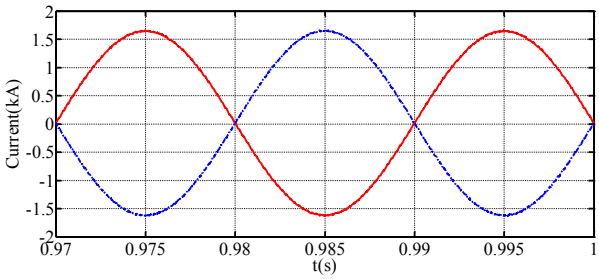
Fig. 8: Waveforms of the conventional two-level converter when it exchanges -200MVAr with the ac grid



(a)

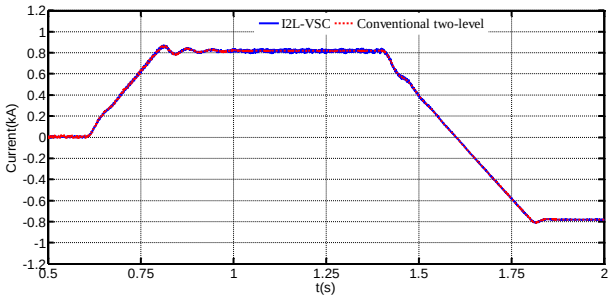


(b) VSC_1 three-phase output currents measured at converter side (low-voltage side of the interfacing transformer)



(c) Samples of the upper and lower arm' currents of the phase a

Fig. 9: Waveforms of the improved two-level converter when it exchanges -400MVAr with the ac grid



(b)

Fig. 10: Selected waveforms illustrate the response both the conventional and improved two-level converter during power reversal (initially, both active and reactive powers are held at zero, at t=0.5s, VSC_1 ramps its active power from zero to import 160MW from G_2 to G_1; at t=1.4s, VSC_1 reverses the power flow from 160MW to -160MW, exporting power from G1 to G2; and reactive power of VSC_1 is held at zero throughout this illustration).

Table II: Semiconductor power loss comparison between conventional and improved two-level converters

	Conventional two-level converter	**Improved two-level converter**
Operating condition	P=180MW & Q=0	
On-state loss	1.4734 MW	1.1996MW
Switching loss	3.5016MW	3.0690MW
Total semiconductor losses	4.9750MW (2.76%)	4.2686MW (2.37%)
Operating condition	P=180MW & Q=90MVAr	
On-state loss	1.74MW	1.36MW
Switching loss	4.06MW	3.35MW
Total semiconductor losses	5.80MW (3.22%)	4.71MW (2.62%)
Operating condition	P=0 & Q=180MVAr	
On-state loss	1.38MW	1.03MW
Switching loss	3.50MW	2.71MW
Total semiconductor losses	4.88MW (2.71%)	3.74MW (2.08%)

Table III: Global comparison between improved and conventional two-level converters and half-bridge modular multilevel converter for HVDC transmission systems applications (Voltage per single IGBT (V_d) is assumed to be equal to that of single MMC submodule capacitor (V_{cell}), therefore, the number cell capacitors (N) is equal to the number of IGBTs in each composite switch of the conventional and improved two-level converters, i.e., $N=V_{dc}/V_d$, where V_{dc} is the dc link voltage)

	Improved two-level converter	Conventional two-level converter	Half-bridge modular multilevel converter
Suitability for dc transmission systems	• HVDC links with rated dc power and dc operating voltage below 200MW and 200kV • Possible to operate in offshore oil platforms that requires variable frequencies from 0 to 63Hz as demonstrated using the conventional two-level converter in [43, 45, 46]. Notice that continuous operation of the I2L-VSC at low frequencies such as 1Hz has been demonstrated in Fig. 12. The I2L-VSC footprint is expected to be similar to or slightly large than that of the two-level converter; therefore attractive in offshore applications.	• HVDC links with rated dc power and dc operating voltage below 200MW and 200kV • Offshore oil platforms that operate at variable frequency such as from 0 to 63Hz as demonstrated in[1, 46]. It small footprint is attractive in offshore applications.	• HVDC links with rated dc power and dc operating voltage above 400MW and 400kV • Unviable at low frequencies[46]; therefore, unsuitable for connection of offshore oil platforms that operate with variable frequency. Also, its large footprint is less attractive in applications with confined space such as offshore oil platforms.
Response to pole-to-pole dc short circuit fault	• Its cell capacitors do not discharge during dc short circuit; thus, it exposes dc circuit breakers connected to its positive and negative pole to similar level of let-through current as the modular multi-level converter of similar rating (lower than the conventional two-level converter, see Fig. 7). • Its freewheeling diodes are exposed to similar current stresses as the modular multilevel converter of similar rating (lower than the conventional two-level converter, see Fig. 7).	• Its dc link capacitor contributes large transient component to dc fault current; thus, making design of dc circuit breakers increasingly challenging [46]. • Exposes its freewheeling diodes to high current stress as it draws extra current from the ac grid as its dc link voltage collapses [47-49].	• Its cell capacitors do not discharge during dc short circuit[2, 3, 50-52]; thus, it exposes dc circuit breakers connected to its positive and negative pole to let-through current, which is predominantly ac grid contribution (its magnitude is determined by the ac grid strength and amount of inductance in the fault loop such as arm and transformer leakage inductances). • Its freewheeling diodes are exposed to lower current stresses than the conventional two-level converter (the same improved two-level converter) [2, 3, 50-52].
Number of semiconductor switches per three-phase converter	6×2N insulated gate bipolar transistors (IGBTs), each rated for V_{dc}/N.	$6\times N$ insulated gate bipolar transistors (IGBTs), each rated for V_{dc}/N	6×2N insulated gate bipolar transistors (IGBTs), each rated for V_{dc}/N
Number of switches in the conduction path	$2N$	N	$2N$
Peak current in the switching devices	$⅓I_{dc}+½I_m$, (I_{dc} and I_m are the dc link current and peak of the output phase current)	I_m	$⅓I_{dc}+½I_m$
Voltage stress per arm	V_{dc}, this means each cell capacitor and composite switch of each arm must be capable of blocking full dc link voltage (V_{dc}) as in the conventional two-level converter.	V_{dc}, this means the dc link capacitor and composite switch of each arm must be capable of blocking full dc link voltage (V_{dc})..	V_{dc}, this means each arm must have sufficient cells to support full dc link voltage (V_{dc}), with share of voltage stress per cell capacitors and switching device is limited to V_{dc}/N.
Semiconductor losses	High, but slightly lower than that of the conventional two-level converter, see Table II	High, see Table II	Low, see reference [15, 53-58]
dv/dt imposed on the interfacing reactors and transformer	High, but remain tolerable as long as the improved two-level converter is applied to system with relatively low dc operating voltage such as 200kV and 300kV	High, but remain tolerable as long as the conventional two-level converter is stretched beyond its dc operating voltage limits which are less 300kV	Low
Voltage stress per device and cell or dc link capacitor	V_{dc} (therefore, series connected devices are used)	V_{dc} (therefore, series connected devices are used)	V_{dc}/N (where N is the number of cells per arm). When N is low as in cascaded two-level converter, series device connection is used within the cells
Power circuit and control complexity	Low complexity, therefore offers the best design trade-off for HVDC links	Low	Very high complexity, but offers the best design trade-off for HVDC links

	with relatively low rated power and dc voltage.		with higher rated power and dc operating voltage.
Arm currents	Continuous, with no 2nd order harmonic currents in its arms; therefore, full modulation index linear range is available for power transfer.	Discontinuous, but full modulation index line range is available for power transfer.	Continuous, but require a dedicated controller with at least 5% of the modulation to be sacrificed for suppression of the 2nd order harmonic currents in its arms. Therefore, its P-Q capability cureb is expected to be smaller the conventional and improved two-level converters with similar ratings. Alternatively, a number of tuned filters to be incorporated into MMC phase legs as being employed in ABB cascaded two-level converter to suppress the circulating currents[59].
Application to Multi-terminal HVDC network	Can be used in parts of multi-terminal dc network that operate with dc voltage, without increasing the fault level beyond that will be contributed by the cable stray capacitors	Not desirable because it will increase fault level	Desirable for use in parts of multi-terminal dc network that operate at high-voltage, without increasing the fault level beyond that will be contributed by the cable stray capacitors

VII. EXPERIMENTAL VALIDATION

This section presents experimental validation of the I2L-VSC, considering open and closed loop operation, with the open loop results aim to illustrate the performance of the I2L-VSC during operation with 50Hz and 1Hz. Whilst the presented closed loop cases illustrate the performance of the I2L-VSC when it is connected to grid, operating at unity and zero power factors. The carrier frequency is fixed at 2.4kHz in all experimental tests presented in this paper.

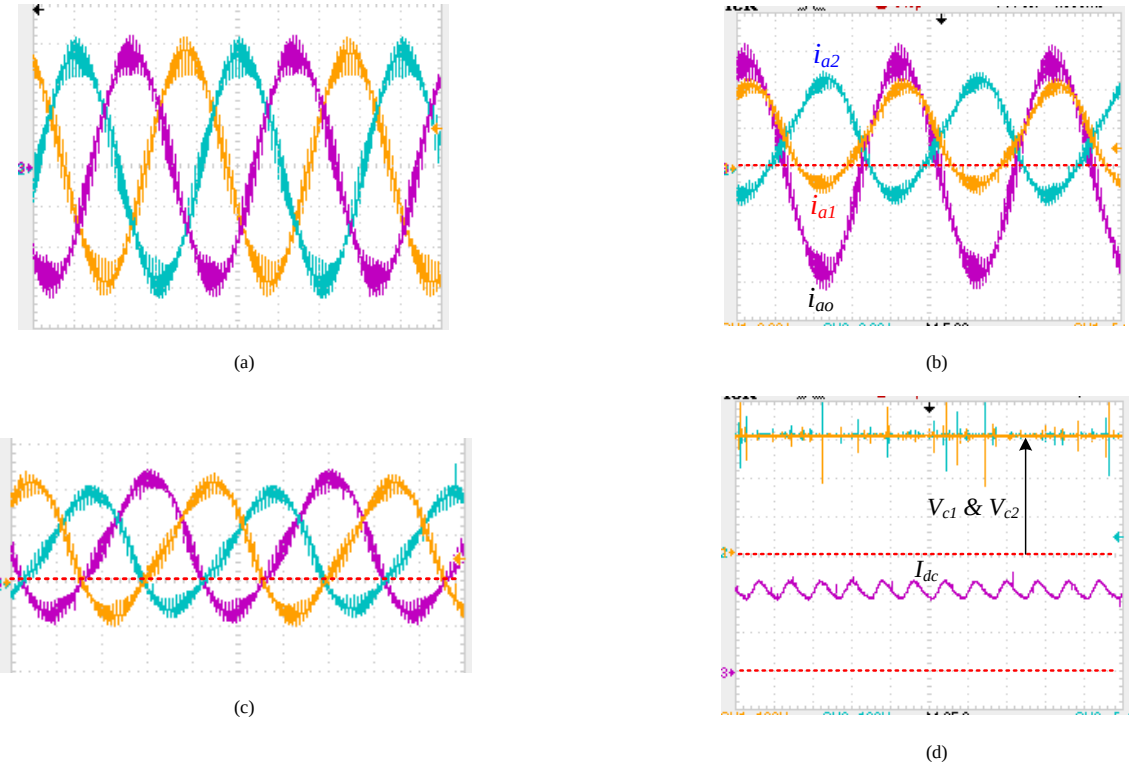
A) Open loop: Fig. 11 shows open loop operation of the I2L-VSC when it supplies a passive load of 26Ω and 5mH at 50Hz and unity modulation index, with detailed of the test rig parameters are given in the caption of Fig. 11. Experimental waveforms for the three-phase load currents, phase '*a*' upper and lower arm currents, 'i_{a1} and i_{a2}', superimposed on its corresponding output phase current 'i_{ao}' indicate that the I2L-VSC adheres to the same principles as the MMC, including continuous arm currents, $½i_{ao}$ superimposed on $⅓I_{dc}$, and no 2nd harmonic currents are observed in the arm currents as predicated in the simulation section, see Fig. 11(a) and (b). Samples of the three-phase lower arms (i_{a2}, i_{b2} and i_{c2}) in Fig. 11 (c) exhibit limited unbalanced due to inherent mismatch in the arm inductances, but this does not affect the three-phase output phase currents i_{ao}, i_{bo} and i_{co}. Fig. 11(d) shows upper and lower arm cell capacitor voltages and dc link currents, and observe the cell capacitor voltages (V_{c1} and V_{c2}) show no low frequency oscillations as predicated by the above simulation cases, but the dc link current (I_{dc}) display small low frequency ripple due to unbalanced in the ac components of the three-phase arm currents, see Fig. 11 (c).

Fig. 12 presents an additional case when the I2L-VSC imposes 1Hz on the passive load connected to its ac side; with the rest of the operating parameters remain the same as in case presented in Fig. 11. Observe that as the ac effect of the arm reactors disappears at 1Hz, the three-phase output load currents remain sinusoidal, despite the arm currents tend to drop to zero for majority of the half cycle in arm with small duty cycle (provided the upper and lower arms of the same phase-leg operate in complementary manner), see Fig. 12(a), (b) and (c). The lower arm three-phase currents appeared to be balanced as the effect of unequal arm inductors diminishes at low frequency. Fig. 12 (d) shows that both the upper and lower cell capacitors and dc link currents are pure dc and

free of low frequency oscillation as indicated earlier in simulation section, and this is because of perfect balance of the ac components of the three arm currents.

B) Closed loop: Fig. 13 presents experimental waveforms of the I2L-VSC when it injects $i_d^*=5.5A$ and $i_q^*=0$ (unity power factor) into 50Hz ac grid at 150Vrms line-to-line voltage, with control systems depicted in Fig. A 1 in appendix A is employed in this demonstration. Fig. 13 (a), (b) and (c) show the three-phase currents converter injects into ac grid superimposed on phase '*a*' voltage, phase '*a*' upper and lower arm and output currents, and upper and lower cell capacitor voltages and dc link current. Additional scenario that considers the case of zero power factor ($i_d^*=0$ and $i_q^*=5.5A$) is presented in Fig. 14. Observe that these results indicate that the I2L-VSC is able to operate satisfactory in all scenarios, including the scenario in Fig. 14 with zero dc link current and dc bias in the arm currents. These results support the accuracy of the theoretical discussions and analysis presented in previous sections.

C) Simulated dc short circuit fault: Fig. 15 displays experimental waveforms of the improved two-level converter when it is subjected to a permanent pole-to-pole dc short circuit fault. The dc fault is initiated by connecting 26Ω resistance across the dc link and 26Ω in series with the dc supply to limit its current. Fig. 15 (a) and (b) shows that when converter is blocked, the cell capacitor voltage remain flat at its pre-fault condition when the dc link voltage collapses to 50%, dc link current reverses direction and the upper and lower arms only conduct through their respective freewheeling diodes as expected, and illustrated in the simulation section. These results support claim with regard to similarity of the transient response of the I2L-VSC is similar to that of the conventional MMC.



(a) (b) (c) (d)

Fig. 11: Waveforms that illustrate the open loop operation of the improved two-level converter at 50Hz, unity modulation index, V_{dc}=300V, passive load of 13Ω and 5mH, 3.3mH arm inductance and 470μF cell capacitance: (a) Three-phase load currents i_{ao}, i_{bo} and i_{co} (5ms/div and 2A/div), (b) Phase '*a*' output and upper and lower arm currents i_{ao}, i_{a1} and i_{a2} (5ms/div and 2A/div), (c) Lower arm currents i_{a2}, i_{b2} and i_{c2} (5ms/div and 2A/div) and (d) Cell capacitor voltages V_{c1} and V_{c2} and dc link current I_{dc}(25ms/dv, 2A/div and 100V/div)

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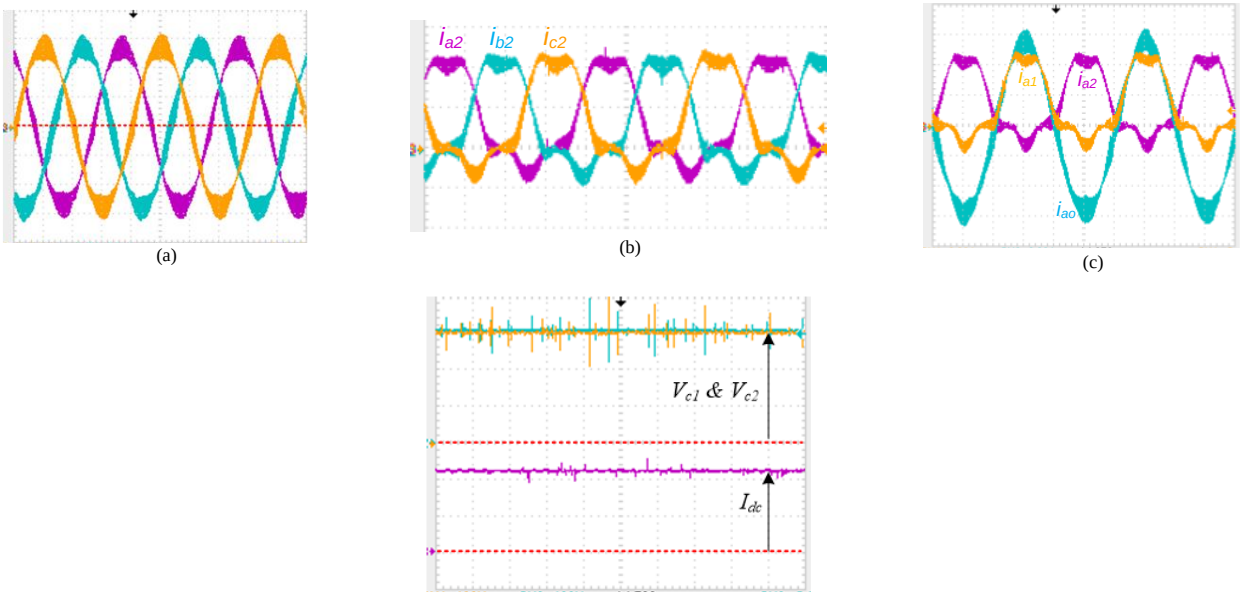
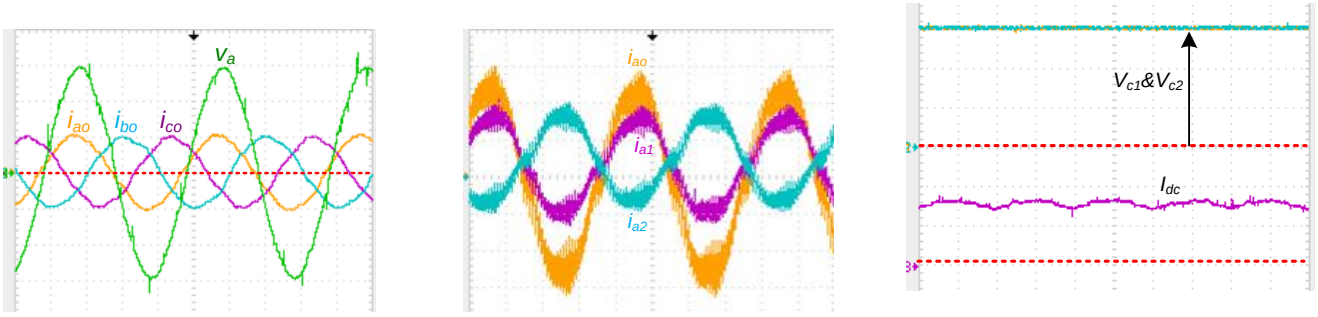


(a) (b) (c) (d)

Fig. 12: Waveforms that illustrate the open loop operation of the improved two-level converter at 1Hz, unity modulation index, V_{dc}=300V, passive load of 13Ω and 5mH, 3.3mH arm inductance and 470μF cell capacitance: (a) Three-phase output currents i_{ao}, i_{bo} and i_{co} (250ms/div, 2A/div), (b) Lower arm currents i_{a2}, i_{b2} and i_{c2} (250ms/div, 2A/div), (c) Phase 'a' output and upper and lower arm currents (250ms/div and 2A/div) and (d) Cell capacitor voltages V_{c1} and V_{c2} and dc link current I_{dc}(500ms/div, 2A/div and 100V/div)

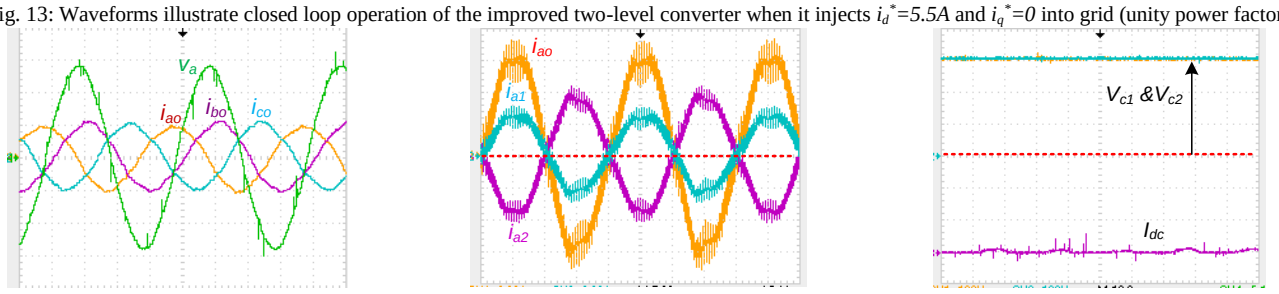


(a) Three-phase currents converter injects into ac grid superimposed on phase 'a' of the grid voltage (5ms/div, 5A/div and 40V/div)

(b) Phase '*a*' upper and lower arm currents superimposed on phase 'a' output current(5ms/div, 2A/div)

(c) Upper and lower cell capacitor voltages, V_{c1} and V_{c2}, and dc link current, I_{dc}(10ms/div, 2A/div and 100V/div)

Fig. 13: Waveforms illustrate closed loop operation of the improved two-level converter when it injects i_d^*=*5.5A* and i_q^*=*0* into grid (unity power factor)

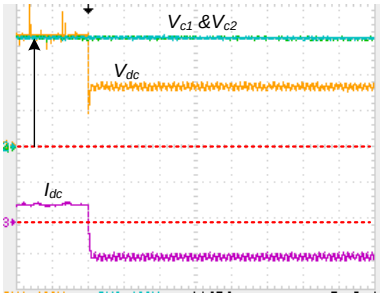


(a) Three-phase currents converter injects into ac grid superimposed on phase 'a' of the grid voltage (5ms/div, 5A/div and 40V/div)

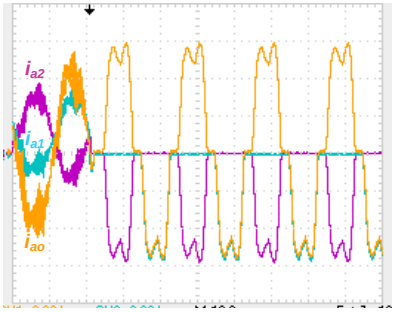
(b) Phase '*a*' upper and lower arm currents superimposed on its corresponding output phase current(5ms/div, 2A/div)

(c) Upper and lower cell capacitor voltages, V_{c1} and V_{c2}, and dc link current, I_{dc}(10ms/div, 2A/div and 100V/div)

Fig. 14: Waveforms illustrate closed loop operation of the improved two-level converter when it injects i_d^*=*0* and i_q^*=*5.5* into grid (zero power factor)



(a) DC link current and voltage, and cell capacitor voltages (25ms, 5A/div and 100V/div)



(b) Upper and lower arm and output phase currents (i_{a1}, i_{a2} and i_{ao})

Fig. 15: Experimental waveforms that illustrate response of the improved two-level converter to dc short circuit

VIII. CONCLUSIONS

This paper presented an improved two-level converter as potential alternative for conventional two-level converter in HVDC transmission systems, with relatively low rated dc voltage and power. The theoretical discussions, simulations and experimentations indicate that the improved two-level converter offers the best compromise between semiconductor losses, waveforms quality, system complexity and transient response to ac and dc network faults. The latter aspects are critical when considering integration of the proposed converter into dc grids, which are expected to be dominated by MMCs . Moreover, this paper presented average, switching function and electromagnetic transient simulation models of the I2L-VSC, including their validations against detailed switch model. It is worth emphasizing that the proposed converter retains ability to operate continuously with full load current at low frequencies such as 1Hz, which is not possible with conventional MMC.

IX. APPENDIX

Fig. A 1 shows generic control system employed with the HVDC link in Fig. 4. Only inner current controller implemented with the test rig in Fig. A.2 to produce experimental waveforms in Fig. 13, Fig. 14 and Fig. 15.

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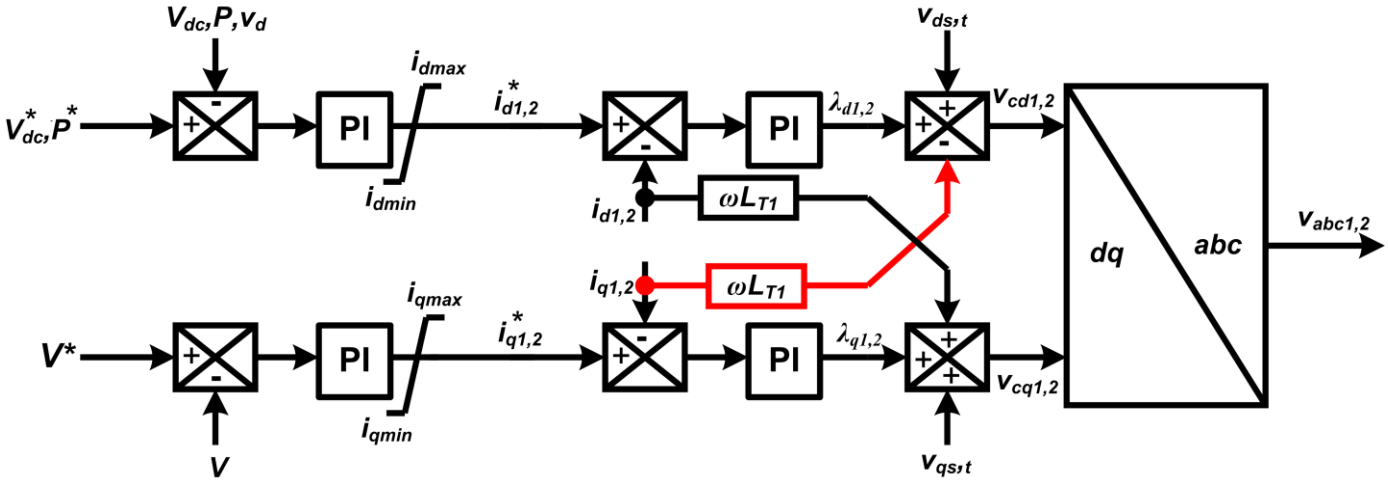
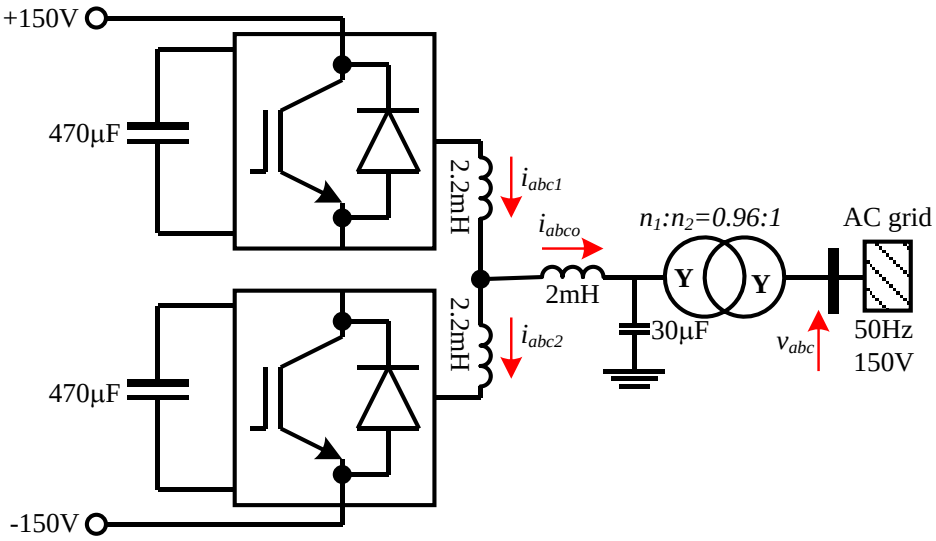
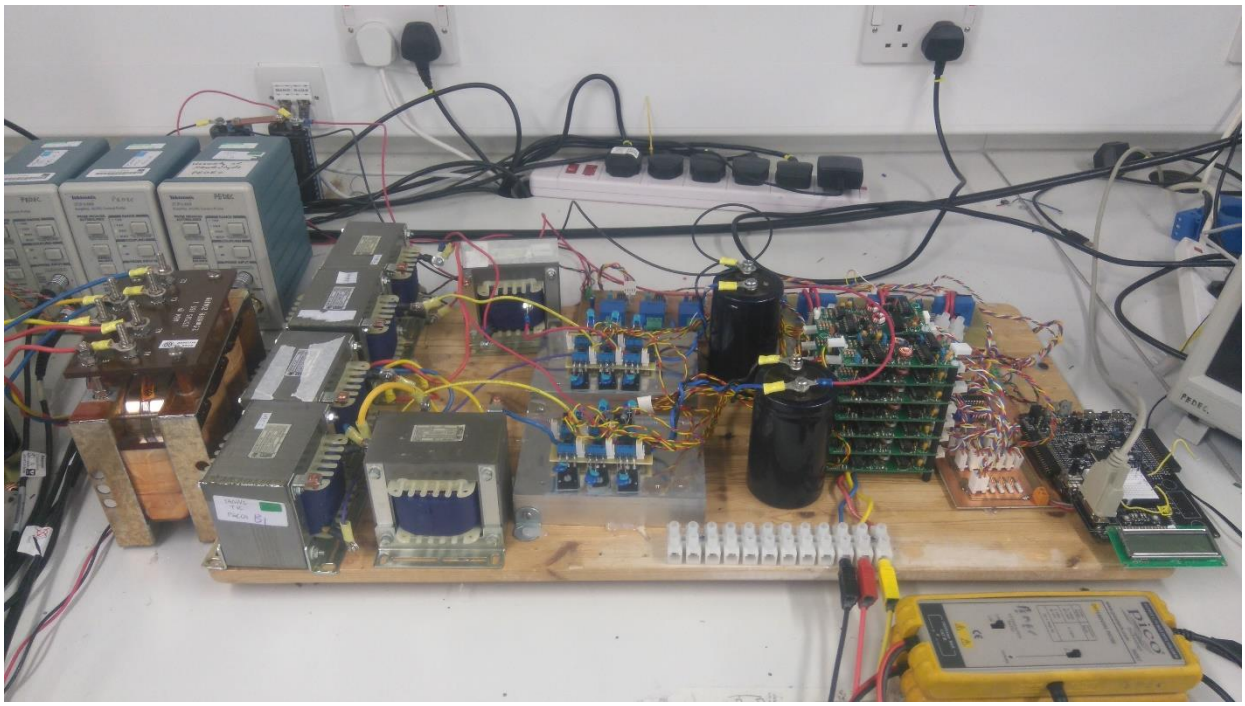


Fig. A 1: Simplified block diagram of the control system employed with test system in Fig. 4, while the inner controller is the only part implemented in the experimental demonstration



(a)



(b)

Fig. A.2: (a) Experimental test rig and (b) picture of the test rig

X. ACKNOWLEDGEMENT

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XI. BIOGRAPHIES

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Ibrahim Abdelsalam: received a first class B.Sc. and M.Sc. degrees in electrical engineering from the Arab Academy for Science and Technology and Maritime Transport, Egypt, in 2006(Alexandria campus) and 2009(Cairo campus). He received the Ph.D. degree in power electronics From University of Strathclyde, Glasgow, UK, 2016. Currently he is Lecture in electrical department at Academy for Science and Technology and Maritime Transport. His research interests are power electronic converters and their applications in wind energy conversion systems, and advanced control strategies of the multilevel voltage and current source converters.

John E. Fletcher (M' 11 – SM'13), He received the B.Eng. (with first class honors) and Ph.D. degrees in electrical and electronic engineering from Heriot-Watt University, Edinburgh, U.K., in 1991 and 1995, respectively. Until 2007, he was a Lecturer at Heriot-Watt University. From 2007 to 2010, he was a Senior Lecturer with the University of Strathclyde, Glasgow, U.K. He is currently a Professor with the University of New South Wales, Sydney, Australia. His research interests include distributed and renewable integration, silicon carbide electronics, pulsed-power applications of power electronics, and the design and control of electrical machines. Prof. Fletcher is a Charted Engineer in the U.K. and a Fellow of the Institution of Engineering and Technology.

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Derrick Holliday has research interests in the areas of power electronics, electrical machines and drives. In 1995 he obtained the degree of PhD from Heriot Watt University and, since then, has held full-time academic posts at the Universities of Bristol and Strathclyde. He has authored or co-authored over 70 academic journal and conference publications. He is currently leading industrially funded research in the field of power electronics for HVDC applications, and is co-investigator on research programmes in the fields of photovoltaic systems and the interface of renewable energy to HVDC systems.

S.J. Finney obtained an MEng degree in Electrical and Electronic Engineering from Loughborough University of Technology in 1988. He worked for the Electricity Council Research Centre before joining the power electronics research group at Heriot-Watt University in 1990, receiving the award of PhD in 1994. From 1994 to 2005 he was a member of academic staff at Heriot-Watt University. In 2005 he joined the University of Strathclyde as a senior lecturer, where he has been promoted to reader then a Professor of Electrical Engineering with the Institute of Energy and Environment, specialising in power electronic systems. He joined University of Edinburgh as professor of electrical engineering in mid-2017. His research interests include power electronics for high power applications and the management of distributed energy resources.

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