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An Active Power Filter Based on a Three-Level Inverter and 3D-SVPWM for Selective Harmonic and Reactive Compensation

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Abstract: Active Power Filters (APFs) have been used for reducing waveform distortion and improving power quality. However, this function can be improved by means of a selective harmonic compensation. Since an APF has rating restrictions, it is convenient to have the option of selecting an individual or a set of particular harmonics in order to compensate and apply the total APF capabilities to eliminate these harmonics, in particular those with a greater impact on the Total Harmonic Distortion (THD). This paper presents the development of a new APF prototype based on a three-phase three-level Neutral Point Clamped (NPC) inverter with selective harmonic compensation capabilities and reactive power compensation. The selective harmonic compensation approach uses several Synchronous Rotating Frames (SRF), to detect and control individual or a set of harmonics using *d* and *q* variables. The APF includes a Three-Dimensional Space Vector Modulator (3D-SVPWM) in order to generate the compensation currents. Because of its multilevel topology, the proposed active power filter can be used in diverse power quality applications at sub-transmission and distribution voltage levels. Simulation and experimental results are shown to validate the proposed solution and assess the prototype performance in different scenarios.

Keywords: active power filters; neutral point clamped; selective harmonic compensation; synchronous rotatory frames

1. Introduction

Harmonic currents produced by power electronic devices and nonlinear loads reduce power quality, leading to diverse problems like increases in power losses, excessive heating in rotating machinery, electromagnetic interference in communication systems, low power factor and failures in electronic equipment [1–5]. There are several alternatives in the industry to improve power quality, each one with their own advantages, disadvantages and field of application, e.g., transient suppressors, line voltage regulators, uninterruptible power supply and active and hybrid power filters [6], among others. APFs are used extensively in three-phase systems to reduce harmonic pollution and improve power quality. These devices can be considered as controlled current sources, which inject harmonic currents opposite to the harmonic currents generated by power electronic devices and non-linear loads, reducing effectively distortion in the current and voltage waveforms [7]. A general description of the APFs' design can be found in [8,9].

APFs have been also proposed to compensate the zero sequence through the neutral conductor in four-wire systems [10], where a Flying Capacitor Converter (FCC) operates as a Shunt Active Power Filter (SAPF) [11]. In general, the controller design of APFs is based on two stages that are clearly defined. In the first stage, the APFs' controller determines the fundamental and the harmonic reference current to be compensated. Several harmonic current detection methods described in the literature have been used at this stage, e.g., instantaneous reactive power theory [12], synchronous reference frame method [13] and supplying current regulation [14], among others. Each one of these techniques has been used in diverse application, and the synchronous reference frame method offers some advantages for dealing with selective harmonic separation.

The second stage in the APF is normally designed to generate the harmonic reference currents to be injected into the AC mains. Initially, for harmonics current cancellation, some well-known modulation techniques, like the Pulse Width Modulation (PWM) technique described in [15], were used. Thus, in [16], an APF for a three-phase, two-level inverter was proposed, where the controller design is oriented to supervise both the line current and the DC-link voltage regulators. Later, the introduction of Space Vector Pulse Width Modulation (SVPWM) techniques and the use of modern high speed micro-processors became one of the more important developments in three-phase inverters [17]. This is due to its undoubted operational advantages over carrier-based techniques, e.g., lower Total Harmonic Distortion (THD), higher efficiency and higher voltage available in the DC-link, as shown in the comparative study presented in [18].

More recently, the 3D-SVPWM modulation technique was proposed in [19]. This technique was applied successfully to two level inverters in [20], minimizing the number of commutations in the switching sequence and duty cycles. The excellent performance of 3D-SVPWM has motivated the development of new applications in motor drives, rectifiers, Static Synchronous Compensator (STATCOM), High Voltage Direct Current (HVDC), APFs and diverse renewable energy applications [21,22]. Some other applications of 3D-SVPWM include a three-phase split-capacitor voltage source inverter, which employs a hybrid voltage control algorithm [23], a three-phase four-leg voltage source converter with a microcontroller [24] and a prototype to reduce common-mode voltage (CMV) at the output of multilevel inverters [25]. It should be mentioned that the Neutral Point Clamped (NPC) three-level inverter is actually the most extensively-applied multilevel topology [26–30]. Another important feature of the 3D-SVPWM technique is the fact that it improves the performance of three-level inverters compared with a two-level device [31]. Consequently, when applied to multilevel inverters, its performance also improves significantly.

Multilevel inverters are used in high-power and medium-voltage applications due to their competitive advantages over their two-level counterparts. Some of their advantages are, e.g., reduced switching-voltage ratings, smaller switching stresses dv/dt and an improved output voltage at lower switching frequencies. These characteristics have led to the development of many applications, including dynamic battery systems, where the multilevel topology allows one to generate a wide range of output voltage levels [32], flexible alternating current transmission system (FACTS) for medium voltage applications [33] and diverse applications in renewable energy, in particular wind energy systems [34].

The developments presented above briefly describe the evolution of modulation techniques for APFs. Actually, 3D-SVPWM is the most efficient and widely-used technique for current harmonic compensation due to its versatility and efficiency. On the other hand, the use of NPC multilevel inverters has become a clear trend, which has the purpose of attending to the potential demand for new applications at power distribution and sub-transmission voltage levels under the smart grid concept. However, the combined application of the above developments (3D-SVPWM and NPC multilevel inverter) for selective harmonic current compensation in APFs has been scarce and limited only to four-wire system applications in order to compensate the zero sequence component [35]. As far as the authors know, the 3D-SVPWM technique never before has been used in NPC multilevel inverters for selective harmonic current and reactive compensation in APFs.

This paper address the design and testing of a novel APF with selective harmonic current compensation capabilities, based on a three-phase multilevel NPC inverter, as shown in Figure 1. The proposed design has the advantage of reducing an individual harmonic current or a particular group of harmonic currents, improving power quality in the grid, which is reflected in the THD. The APF uses the 3D-SVPWM to generate the pulses that the converter needs to produce the compensation currents. The APF multilevel topology facilitates its use in power quality applications at sub-transmission and distribution voltage levels. The advantage of multiple or selective harmonic compensation is evident, since the APF can be used in diverse applications for reducing an individual or a set of harmonic currents, in addition to reactive power compensation. This feature allows one to use all of the power available in the APF for reducing those harmonics with a greater impact on the THD. In the next sections, the salient steps in the APF design are described. Finally, the experimental works for the assessment of the proposed design in an APF prototype are presented.

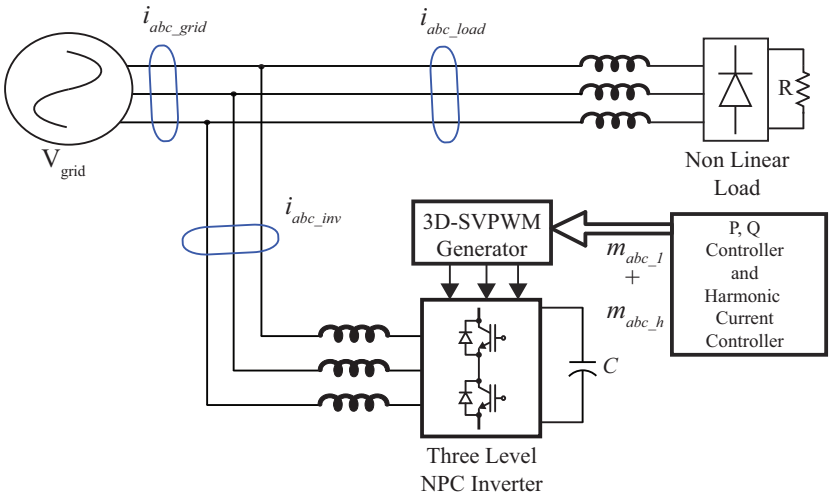


Figure 1. Active power filter with multilevel inverter topology.

2. Results and Discussion

2.1. Three-Level Inverter

An advantage of the multilevel NPC inverter topology is that voltage stresses across the switches are reduced due to a greater number of switching devices and voltage levels. An appropriate selection of switching vectors also reduces harmonic currents generated by the inverter [36,37].

A three-phase three-level NPC inverter is shown in Figure 2. Each phase shares a common DC bus, subdivided by two capacitors in three levels. The voltage across each capacitor is $V_{DC}/2$; and the voltage stresses across each switching device and clamping diodes are limited to $V_{DC}/2$. A three-level NPC is capable of providing five levels of line to line voltage and three levels of phase voltage. The NPC inverter reduces harmonics in both current and voltage output.

Table 1 shows the switch states for phase a, and similar switching sequences can be derived for the remaining phases considering a displacement of 120°. Here, S_{1a} and S_{3a} are complementary between them and, so, for S_{2a} and S_{4a}. State condition 1/0 means switch ON/OFF conditions.

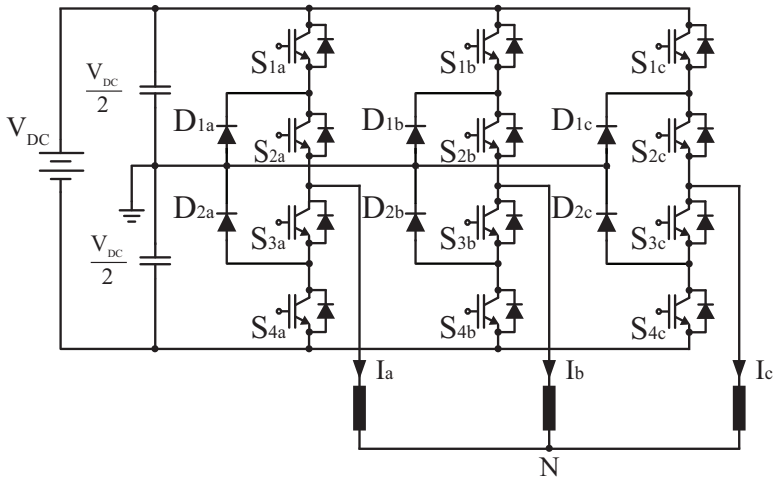


Figure 2. Three-level Neutral Point Clamped (NPC) inverter topology.

Table 1. Switching states for a three-level NPC inverter.

States of Switches				Voltage
S_{1a}	S_{2a}	S_{3a}	S_{4a}	Level V_{aN}
1	1	0	0	$+V_{DC}/2$
0	1	1	0	0
0	0	1	1	$-V_{DC}/2$

From Figure 2, a (m)-level diode clamped inverter includes ($m-1$) capacitors on the DC bus. Furthermore, there are m-level phase voltage outputs and ($2m-1$)-level line voltage outputs. Each active switching device has to withstand a blocking voltage of $V_{DC}/(m-1)$; however, the clamping diode must have different voltage ratings for reverse voltage blocking. The number of diodes required is $2(m-2)$, and the number of switches is $2(m-1)$ for each phase, where m is the number of inverter levels.

2.2. Harmonic Detection Using the d-q Synchronous Reference Frame

The harmonics in the load current are detected using the Synchronous Reference Frame (SRF) technique and a Low Pass Filter (LPF); see Figure 3. Hence, in the *d-q* harmonic frame, only the selected harmonic is a DC-signal, and all other frequencies, including the fundamental, are AC signals. The LPF is used for removing all of these AC signals, filtering only the DC signal representative of the harmonic current of interest [38]. The filtered *d-q* harmonic current from the load and the inverter is then fed to the PI controller. The controller generates harmonic currents of equal magnitude to those produced by the non-linear load, for example, but of opposite polarity. Therefore, the harmonic currents due to the non-linear load will be compensated by the inverter harmonic currents, at the point of common coupling.

The proposed arrangement includes a saturation limit on every PI controller in order to ensure that harmonic currents never increase beyond an allowed range. Otherwise, the inverter voltage reference reaches magnitudes greater than the maximum allowed voltage by the DC capacitor. This may lead to saturation in the modulator signal, which in turn produces unwanted harmonic signals. The main advantages of this approach are that it allows one to compensate a single or a set of harmonic currents, according to system requirements. For example, only those harmonic currents with a greater impact on the THD can be selected for compensation. This is quite useful because APFs do not have infinite power available to compensate harmonic currents.

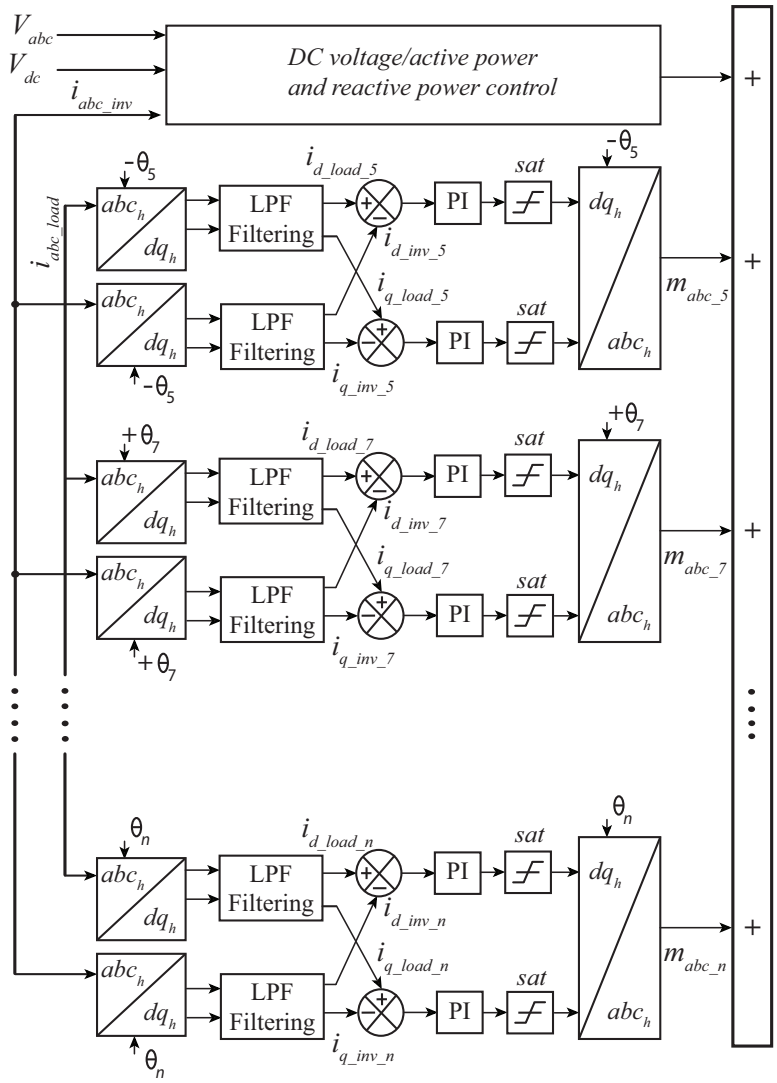


Figure 3. Selective harmonic compensation based on the synchronous reference frame.

2.3. Active Power Filter Controller

The vector control approach used has the advantage of a decoupled control for active and reactive power, combined with a fast dynamic current response. The block diagram for the proposed APF controller is shown in Figure 4. The design uses the three phase currents and voltages, which are vectors in the complex α-β reference frame. A rotating reference frame synchronized with the AC-grid is also introduced, the d-q frame, where voltages and currents remain constant. The angle between both reference frames, θ, is computed by using a Phase Locked Loop (PLL). The information from the PLL is used to synchronize the grid voltage phase angle with the phase voltages generated by the inverter. Therefore, from the above, it is convenient to use the cascade connection of two controllers with independent PI control loops in an outer and inner array.

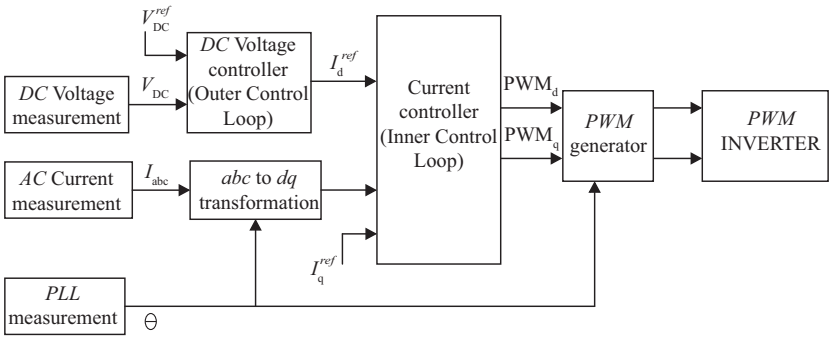


Figure 4. Vectorial control scheme.

2.4. Inner and Outer Controller

The control system is mainly based on a fast inner loop controlling the AC current. The inner current control loop can be implemented in the *d*-*q* frame using the basic relationship for the system model. The inner current control block is presented in Figure 5. Inside the PI controller block, there are two PI regulators, for the d and q axis current, respectively. After comparison, these PI controllers transform the error between the d and q current components into voltage magnitudes. The representative equation for the PI controller is:

$$R(s) = K_p + \frac{K_i}{s} = K_p \left(\frac{1 + T_i \cdot s}{T_i \cdot s} \right), \tag{1}$$

applying the Laplace transform to $I \rightarrow I(s)$. Considering $I(s)$, $I_{ref}(s)$ and the PI controller block:

$$\left\{ I_{ref}(s) - I(s) \right\} \left(K_p + \frac{K_i}{s} \right) = V'_{inv}(s). \tag{2}$$

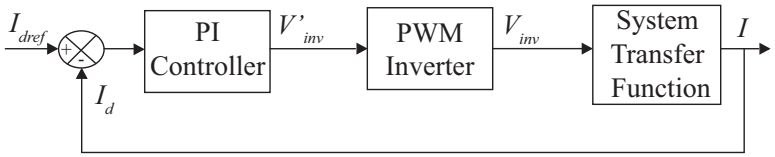


Figure 5. General block diagram for the inner current control.

For control purposes, the inverter can be considered as an ideal power transformer with a time delay. The inverter output voltage tracks the voltage reference signal with an average time delay equal to half the switching cycle and produced by the inverter switches. Hence, the general expression is:

$$V'_{inv}(s) \frac{1}{1 + T_a \cdot s} = V_{inv}(s), \tag{3}$$

where $T_a = T_{switch}/2$.

The phase voltages and currents in Figure 1 are given by:

$$V_{abc} = Ri_{abc} + L \frac{di_{abc}}{dt} + V_{abc\_inv}, \tag{4}$$

where V_{abc} and i_{abc} are AC voltages and currents, respectively, and V_{abc_inv} is the inverter voltage. R and L are the resistance and filter inductance between the converter and the AC system. Using the

abc to *d-q* transformations, the three-phase inverter currents and voltages are expressed in the *d-q* reference frame as:

$$V_d = Ri_d + L\frac{di_d}{dt} - \omega Li_q + V_{dinv}, \tag{5}$$

$$V_q = Ri_q + L\frac{di_q}{dt} + \omega Li_d + V_{qinv}, \tag{6}$$

which are rotating synchronously at the AC frequency ω. Similarly, in the output side:

$$I_{dc} = C\frac{dV_{dc}}{dt} + I_L. \tag{7}$$

Observe that Equations (5) and (6) are similar; therefore, only the *d*-axis equations will be used from now on. The inner loop current controllers for i_d provides the output voltage reference signals, V_d, which are fed into the inverter. By using (5),

$$V_{dinv} = (i_{dref} - i_d)\left(K_p + \frac{K_i}{s}\right)\frac{1}{1 + sT_a}. \tag{8}$$

Equations (5) and (6) have the frequency-induced terms, wLi_d and wLi_q, which produces a cross-coupling between d and q currents. This undesired cross-coupling term can be eliminated algebraically in the control loops, allowing an independent control in the d and q axis, respectively. The compensating terms used for decoupling the system input from the converter are defined as:

$$V'_{dinv} = -(i_{dref} - i_d)\left(K_p + \frac{K_i}{s}\right) + wLi_q + V_d, \tag{9}$$

by substitution of (9) in (3) and then combined with (5),

$$L\frac{di_d}{dt} + Ri_d = V_{dinv}, \tag{10}$$

applying a Laplace transformation, Equation (10) becomes,

$$sI_d(s) = -\frac{R}{L}I_d(s) + \frac{1}{L}V_{dinv}(s). \tag{11}$$

Thus,

$$I_d(s) = \frac{1}{sL + R}V_{dinv}(s), \tag{12}$$

and the system transfer function is:

$$G(s) = \frac{1}{R}\frac{1}{(1 + s\tau)}, \tag{13}$$

where the time constant is defined as $\tau = L/R$.

Let us consider that the cross-coupling terms in the *d-q* current equations, and the grid voltage components are disturbances, not present during the calculation of the *d-q* current control, but instead being numerically compensated by a feed-forward loop in the main harmonic current control loop. Then, the transfer function for the *d-q* fundamental and its harmonic currents is:

$$G(s) = \frac{i_{d\_h}(s)}{V_{dinv\_h}(s)} = \frac{i_{q\_h}(s)}{V_{qinv\_h}(s)} = \frac{i_h(s)}{V_{inv_h}(s)}, \tag{14}$$

where V_{dinv_h} and V_{qinv_h} are the *d-q* components of the average voltages generated by the inverter for the harmonic h, i_{d_h} and i_{q_h} are the *d-q* components for the current between the inverter and the grid for the harmonic h.

Observe in (13) that the system has a stable pole at $-R/L$. This pole can be cancelled by the zero provided by the PI controller, where Kp_{inv_h} and Ki_{inv_h} are the proportional and integral constants of the h harmonic in the PI current controller. Thus, $Ki_{inv\_h}/Kp_{inv\_h} = R/L$ and $Kp_{inv\_h}/L = 1/\tau_{inv\_h}$, where τ_{inv_h} is the time constant of the closed-loop system.

The average value of DC current for the active power filter, i_{dc}, can be represented in terms of the fundamental AC currents and the inverter modulator signals. In the *d-q* reference frame, this is:

$$i_{dc} = 3/4(m_{dinv}i_d + m_{qinv}i_q), \tag{15}$$

where m_{dinv} and m_{qinv} are the APF modulator signal. The *d-q* fundamental voltages, (5) and (6) can be represented in terms of the modulator signals and the DC voltage V_{dc}, where $V_{dinv} = V_{dc}m_{dinv}/2$ and $V_{qinv} = V_{dc}m_{qinv}/2$. Thus, by solving (5) and (6) for i_d and i_q currents and then substituting these values in (15), the following expression for the i_{dc} and the DC power produced, P_{dc}, are:

$$i_{dc} = \frac{3R}{2V_{dc}}(i_d^2 + i_q^2) + \frac{3L}{2V_{dc}}\left(i_d\frac{di_d}{dt} + i_q\frac{di_q}{dt}\right) - \frac{3}{2V_{dc}(V_d i_d)}, \tag{16}$$

$$i_{dc}V_{dc} = P_{dc} = \frac{3R}{2}(i_d^2 + i_q^2) + \frac{3L}{4}\frac{d}{dt}(i_d^2 + i_q^2) - \frac{3}{2}(V_d i_d). \tag{17}$$

Equation (17) shows that in the DC side, the APF power is composed by the sum of resistive losses on the AC side $(3 \cdot R(i_d^2 + i_q^2)/2)$, the energy stored in the inductance between the inverter and the AC grid $(3/4 \cdot L \cdot d/dt \cdot (i_d^2 + i_q^2)/2)$ and the AC active power $(3/2 \cdot (V_d i_d))$. Since resistive losses are very small, they can be neglected from the dynamic equation of P_{dc}, (17). Furthermore, for low values of L, the energy stored in the inductance can also be neglected. Thus, the final equation describing the dynamics of the DC voltage is simplified to:

$$\frac{C}{2}\frac{dv_{dc}^2}{dt} = P_{load} + \left(-\frac{3}{2}(V_d i_d)\right), \tag{18}$$

where C is the circuit DC capacitance. In order to deal with linear terms (assuming that V_d is constant), the output variable of the DC-plant is selected to be the square of the capacitor voltage (i.e., a representation for the energy in the capacitor). Thus, selecting the square of the capacitor voltage $w = V_{dc}^2$ and considering P_{load} a disturbance, not present during the calculation of the voltage controller, the transfer function for the DC-plant can be presented as:

$$\frac{w(s)}{i_d(s)} = P_w(s) = -\frac{3V_d}{Cs}. \tag{19}$$

From (19), the plant $P_w(s)$ has a pole in the origin, and therefore, it is susceptible to disturbances. In order to improve the disturbance rejection of plant $P_w(s)$, an additional control loop is required to speed up the plant natural response, which can be incorporated into the controller design. This control loop is designed to move the pole away from the origin into the negative side of the real axis. The configuration for the additional control loop is shown in Figure 6. By adding a feedback loop of gain G_w, as shown in Figure 6, the transfer function of the improved plant $M_{dc}(s)$ is:

$$M_w(s) = -\frac{P_w(s)}{1 + P_w(s)G_w} = -\frac{3V_d}{Cs + 3V_d G_w}. \tag{20}$$

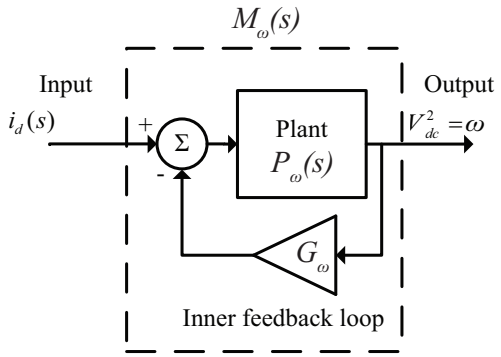


Figure 6. The inner feedback loop applied to improve the load disturbance rejection of the DC voltage plant.

As shown in Equation (20), the artificial pole added by the inner feedback loop has a value of $3V_dG_w$. This value must be selected according to the desired speed of response; the larger the value of G_w, the faster the speed of response, which means a better disturbance rejection. Some control designers select G_w to make the plant dynamics as fast as the controller response time. The inner feedback loop can be implemented in the digital controller scheme by making the current control signal of the controller equal to,

$$i_d(s) = i'_d(s) - G_w w, \tag{21}$$

where $i'_d(s)$ is the controller output. Once the inner feedback loop has been added to the DC voltage plant, the controller tuning can be made by means of zero-pole cancellation, since now, the DC voltage plant has a stable artificial pole at $-3V_dG_w$. This pole can be cancelled with the zero provided by the PI rotor speed controller defined as:

$$K_w(s) = \frac{Kp_w s + Ki_w}{s} = \frac{Kp_w}{s}\left(s + \frac{Ki_w}{Kp_w}\right), \tag{22}$$

where Kp_w and Ki_w are the proportional and integral constants of the DC voltage controller. Thus, by selecting $Ki_w/Kp_w = 3V_dG_w/C$ and $3Kp_wV_d/C = 1/\tau_w$, where τ_w is the time constant of $w = V_{dc}^2$ in the closed-loop system, then the open-loop controller gain is:

$$\iota_w(s) = K_w(s)M_w(s) = \left(\frac{3Kp_wV_d}{Cs}\right)\frac{\left(s + \frac{Ki_w}{Kp_w}\right)}{\left(s + \frac{3V_dG_w}{C}\right)} = \frac{1}{\tau_w s}, \tag{23}$$

and the closed loop transfer function:

$$B_{dc}(s) = \frac{V_{dc\_ref}^2(s)}{V_{dc}^2} = \frac{K_w(s)M_w(s)}{1 + K_w(s)M_w(s)} = \frac{\frac{1}{\tau_w s}}{1 + \frac{1}{\tau_w s}} = \frac{1}{\tau_w s + 1}, \tag{24}$$

which is a first-order transfer function with unitary gain. The selection of τ_w is chosen according to the desired speed of response of the closed loop system. It is recommended to set this loop at least three-times greater than the time response of the i_d control loop. Figure 7 shows the DC voltage control loop.

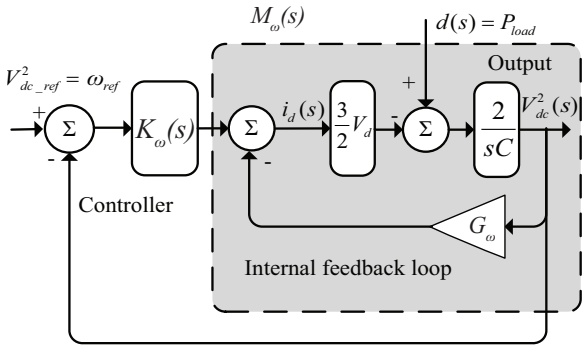


Figure 7. DC voltage control loop.

Figure 8 shows the Bode plots for the system in the DC voltage control loop. The transfer function for the DC voltage $P_w(s)$ is a single integrator, according to (19). After adding an additional control feedback loop, the improved plant of the DC voltage $M_w(s)$ now contains an artificial pole at 146 rad/s. This pole was selected to provide load disturbance rejection according to the closed loop dynamics, by means of a real pole. The Bode plot for the closed loop transfer function shows that the the DC controller loop performance is a first order transfer function.

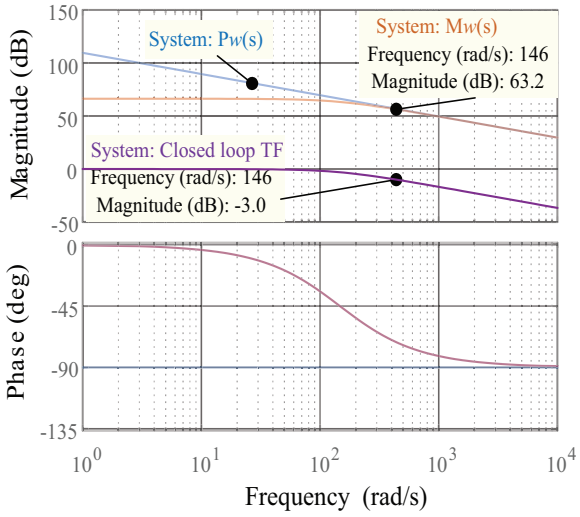


Figure 8. Bode diagram for the outer controller.

Figure 9 shows the Bode plots of the system in the current control loop. The transfer function for the plant that defines the current dynamics is a first order system. The closed loop transfer function includes the transfer function for the PI controller in cascade with a second order filter used to remove the AC components of the *d*-*q* harmonic currents. However, at the frequency of interest (299 rad/s), the dominant dynamics are mainly due to the plant and the PI controller.

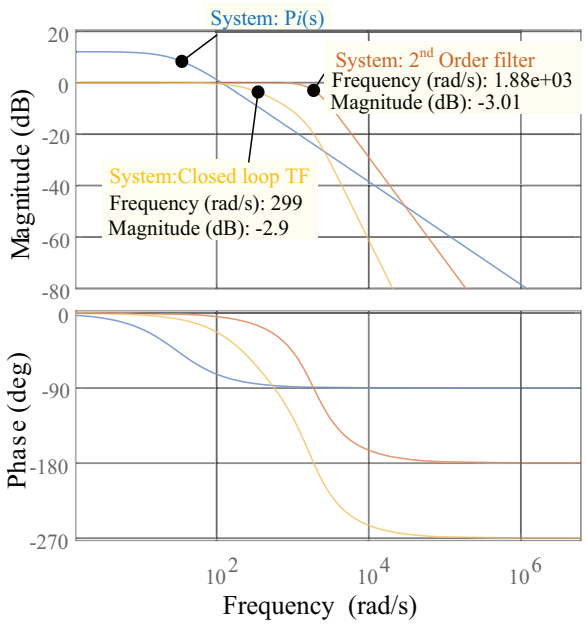


Figure 9. Bode diagram for the inner controller.

2.5. The Reactive Power Controllers

The reactive power dynamics is defined by:

$$Q = -\frac{3}{2} V_d i_q, \tag{25}$$

where Q is the reactive power. According to (25), the relationship between the amount of Q current and the inverter reactive power is directly proportional if the AC voltage is assumed to have a constant value. Because of this, a simple integral controller is enough to control the reactive power with first order dynamics and zero steady state error. The transfer function, G_Q, from the reactive power Q to the i_q current is given by:

$$G_Q = \frac{i_q}{Q} = -\frac{2}{3V_d}. \tag{26}$$

In case of an integral controller of the type $C_Q(s) = Ki_Q/s$, where Ki_Q is the integral constant of the reactive power controller, G_Q is added in cascade, and the following open loop expression is obtained:

$$A_Q(s) = G_Q \cdot C_Q(s) = -\frac{2Ki_Q}{3V_d s}. \tag{27}$$

If Ki_Q is selected to have a value of $Ki_Q = -3V_d\alpha_Q/2$, where α_Q can be regarded as the closed loop bandwidth of the controller, then the open loop expression $A_Q(s)$ and the closed loop expression $E_Q(s)$ from the reactive power reference Q_{ref} to Q are:

$$A_Q(s) = -\frac{2}{3V_d s}\left(-\frac{3V_d\alpha_Q}{2}\right) = \frac{\alpha_Q}{s}, \tag{28}$$

$$E_P(s) = \frac{Q}{Q_{ref}} = \frac{A_Q(s)}{1 + A_Q(s)} = \frac{\alpha_Q}{s + \alpha_Q}. \tag{29}$$

As seen in Equation (29) the closed loop dynamics for the active power control loop are a first order system with a closed loop bandwidth of α_Q. The value of α_Q can be selected for a given rise time of the control variable by the following formulations for first order systems:

$$\alpha_Q \approx \frac{0.35}{t_{r\_Q}}(\text{Hz}) \quad \text{or} \quad \alpha_Q \approx \frac{2.2}{t_{r\_Q}}(\text{rad}), \tag{30}$$

where t_{r_Q} is the desired rise time for the closed loop system. Figure 10 shows the block diagram for the reactive power control loop.

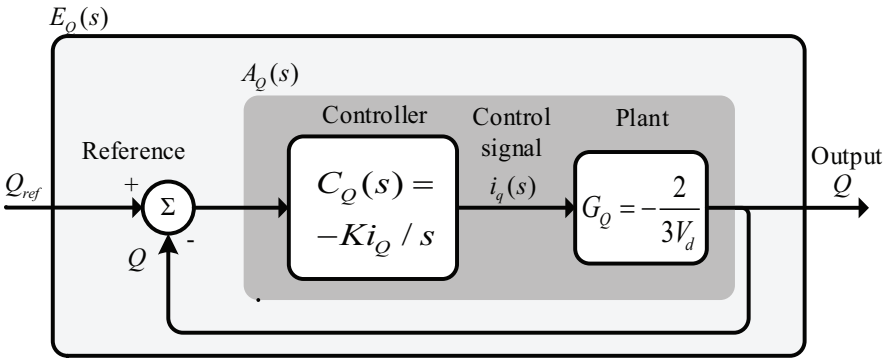


Figure 10. Schematic diagram for the reactive power control loop.

2.6. Three-Dimensional Space Vector Modulator

The 3D-SVPWM algorithm allows one to calculate efficiently the commutation sequence by using four state vectors, which are adjacent to the reference vector. The algorithm also determines the respective commutation times for the power electronic devices in the three-level converter [39,40]. The reference vector can be represented by a tetrahedron whose vertices are the state vectors of the switching sequence. Figure 11 shows the generalized 3D space for a three-level NPC inverter. In this figure, 0, 1 and 2 represent the different DC levels, where 0 is the lower DC level, 1 is the connection between the neutral point and each converter phase and 2 is the higher DC level. The multilevel control region is divided into several sub-cubes, and the first step of the modulation algorithm is to find the sub-cube where the reference vector is pointing. Considering this sub-cube using *abc* coordinates and changing the origin coordinates to the nearest (0, 0, 0) sub cube vertex, the problem is reduced to a two-level case because the two-level control region is one sub-cube. Therefore, the reference vector is pointing to a tetrahedron. The tetrahedron vertices are the switching sequence state vectors. The modulation algorithm input is a normalized voltage vector. The normalization depends only on the number of inverter levels n and the DC voltage level at the inverter input. The modulation algorithm takes, as the origin, the coordinates (0, 0, 0), so that the standard reference voltage must be displaced, as shown in Figure 12.

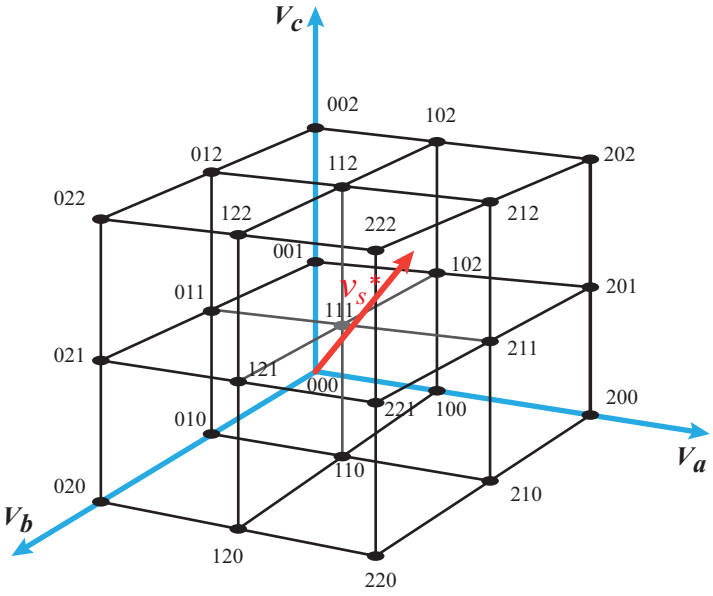


Figure 11. Generalized 3D space for a three-level NPC inverter.

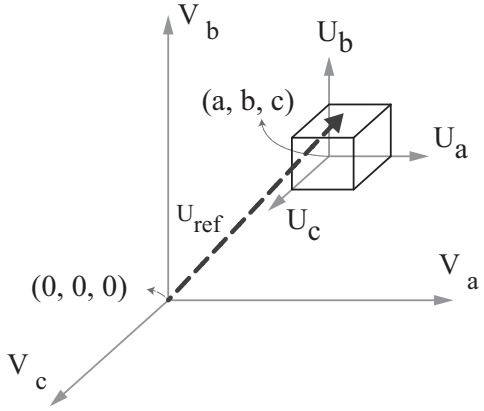


Figure 12. Sub-cube and the reference vector.

Six tetrahedrons should be studied for each sub-cube. Therefore, it is required to define these possible tetrahedrons where the reference vector can be found. The desired tetrahedron can be easily found using comparisons with the three planes at 45° within the three-dimensional space, which directly defines the six tetrahedrons within the sub-cube. A maximum of three comparisons is necessary to find the desired tetrahedron. Figure 13 shows the six tetrahedrons with corresponding state vectors where the reference vector can be found. The computational load is always the same, being independent of the number of inverter levels.

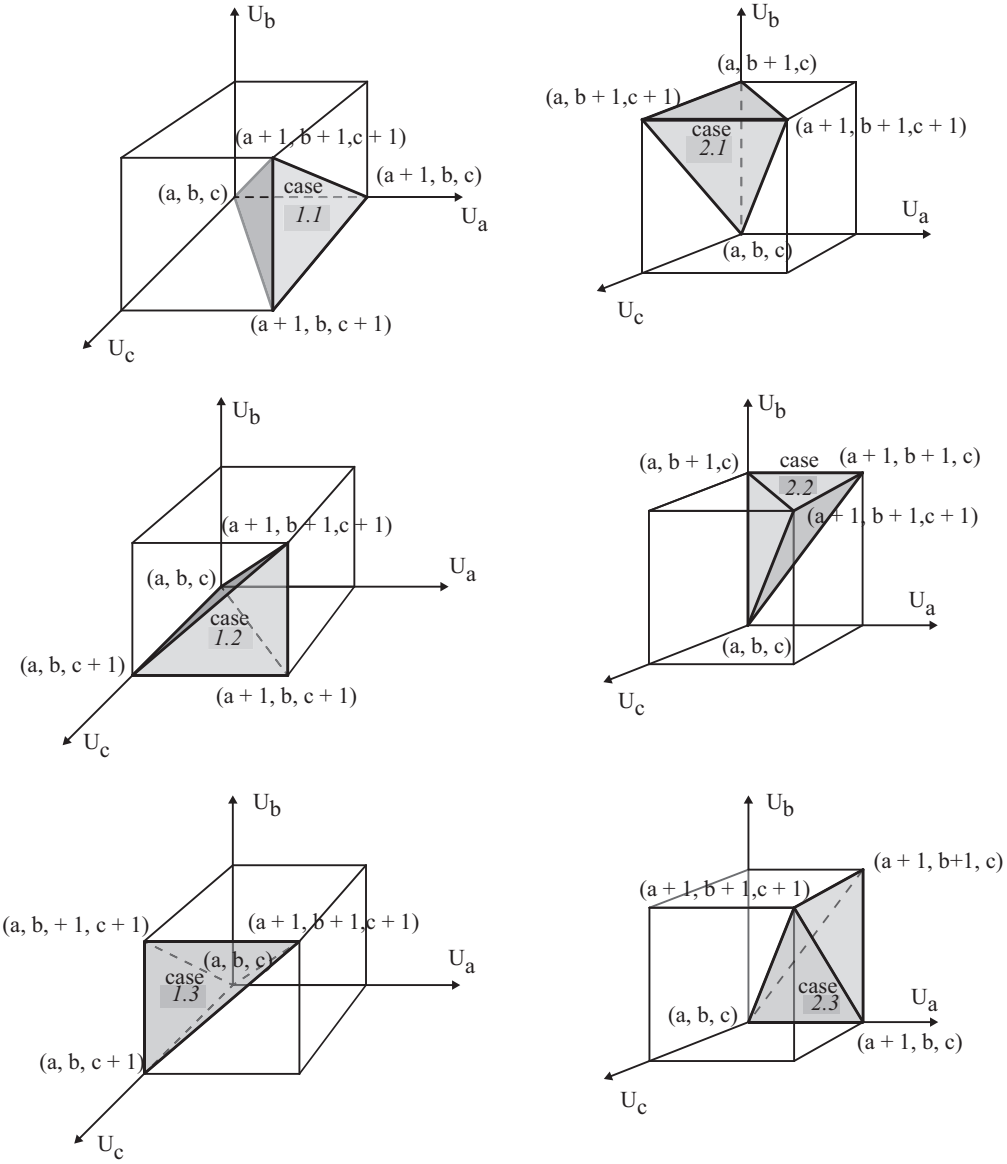


Figure 13. Tetrahedrons in a sub-cube with corresponding state vectors.

Figure 14 shows the flowchart for the 3D-SVPWM algorithm for calculating the tetrahedron where the reference vector is localized and the corresponding state vectors. Figure 15 shows the complete block diagram of the 3D-SVPWM algorithm. Once the state vector, generated by the reference vector, is defined, the switching times must be calculated. The algorithm generates, as output, the matrix shown in (31) with four state vectors.

$$Sec = \begin{pmatrix} S_a^1 & S_a^2 & S_a^3 & S_a^4 \\ S_b^1 & S_b^2 & S_b^3 & S_b^4 \\ S_c^1 & S_c^2 & S_c^3 & S_c^4 \end{pmatrix}, \tag{31}$$

Thus, the associated switching times are defined by:

$$t = \begin{pmatrix} S_1 \\ S_2 \\ S_3 \\ S_4 \end{pmatrix}. \tag{32}$$

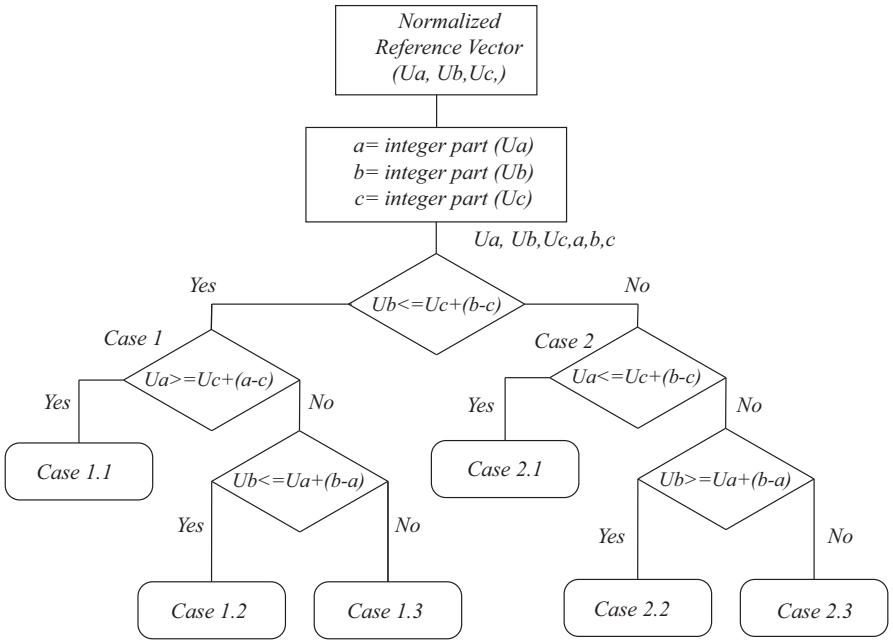


Figure 14. Flowchart for the Three-Dimensional Space Vector Modulator (3D-SVPWM) algorithm.

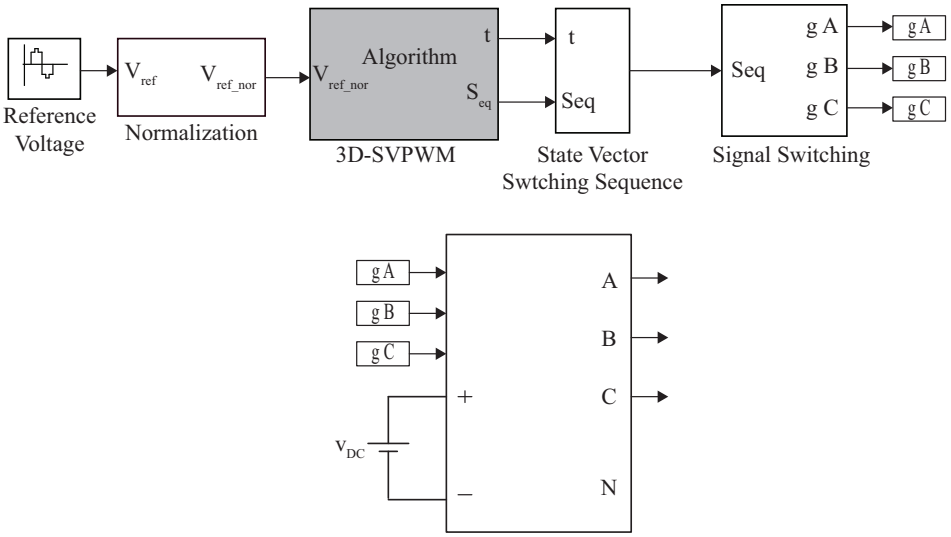


Figure 15. Block diagram for the 3D-SVPWM algorithm.

3. Experimental Work

This section describes the computer simulations and experimental results obtained in the APF prototype build up according to the methodology proposed in Section 2.

3.1. Computer Simulations

The APF performance was simulated first in MATLAB/Simulink, 2014b® in order to verify their operational characteristics and to assess the convenience of building up the prototype shown in Figure 1. In the computer simulations, a three-phase rectifier was used as a nonlinear load connected to the grid at 100 V, 60 Hz through filtering inductors with L = 8.4 mH. The APF maintains a DC voltage up to 250 V by using a capacitor C = 820 µF. Table 2 shows some cases of study regarding selective harmonic compensation; the numbers in this table represent the proportion of harmonic compensation considered. For example, 1 represents 100% compensation, and so on. It is important to remark that the THD obtained after using the APF and compensating all of the harmonic currents is below 5%, which complies with regulations. The THD obtained without using the APF is 27.4%.

Table 2. Study cases for selective harmonic compensation.

CASE	HARMONICS				
	5th	7th	11th	13th	THD
1	1	1	1	1	4.2%
2	1	0	0	0	10.8%
3	1	0.5	0.5	0.5	6.3%
4	0.5	0.5	0.5	0.5	12.2%
5	0.5	0	0	0	15.1%
6	0.5	1	1	1	11.2%
7	0	1	1	1	21.5%

Figure 16 shows graphically the current waveforms' performance before and after current compensation at t = 0.8962 s. In this figure, the benefits of using the compensation levels shown in Table 2, Case 1, are evident. For example, in this particular case, the THD is reduced from 27.4% to 4.2%. Figure 17 shows the process for harmonic current compensation using the proposed APF and the waveforms shown in Figure 16. First, from the contaminated signal shown in Figure 17a, the reference filtered current is obtained (Figure 17b), which is a mixture of different harmonics. Figure 17c shows the opposite currents generated by the multilevel inverter, which must be injected into the system for harmonic current compensation. The final outcome of this process is a signal Figure 17d with a smaller waveform distortion and a new improved THD equal to 4.2%. On the other hand, Figure 18 shows the THDs obtained for the different harmonic currents with and without compensation, Cases 1, 2, 5 and 7 from Table 2. In general, the computer simulations show that the selection of the harmonic currents to compensate and the percentage of compensation have a significant impact on the THD. The computer simulations also show that the methodology proposed is capable of eliminating harmonic currents with good results. Thus, it was decided to build up the APF prototype.

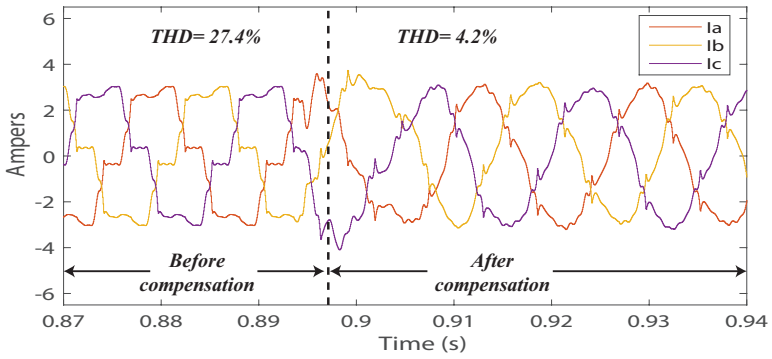


Figure 16. Three phase grid currents before and after compensation.

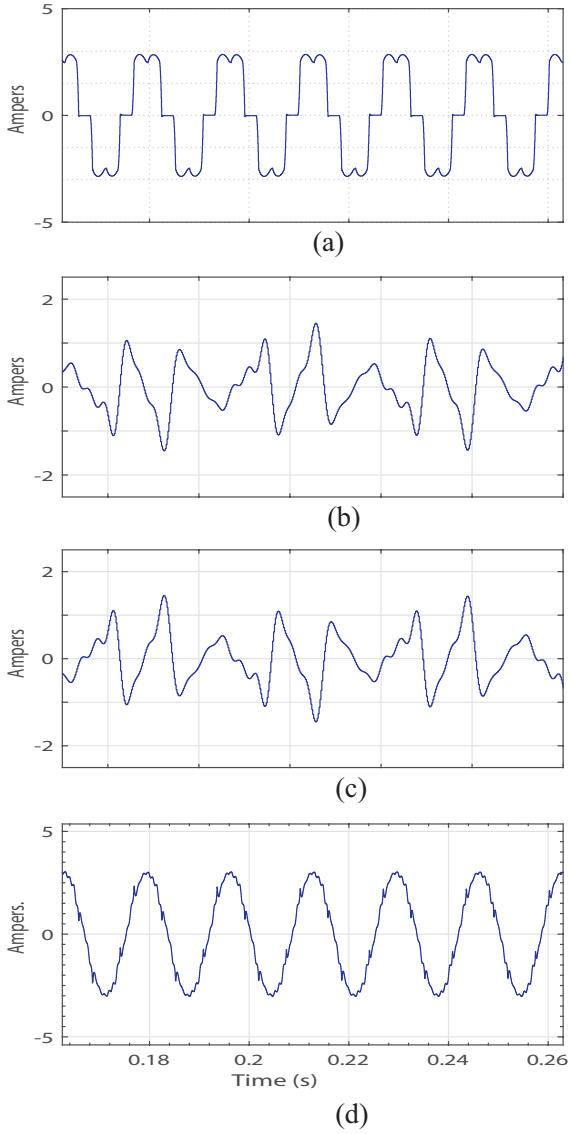


Figure 17. Harmonic current compensation process for phase *a*: (**a**) grid current without compensation; (**b**) reference filtered current; (**c**) injected current into the system; and (**d**) grid current compensated.

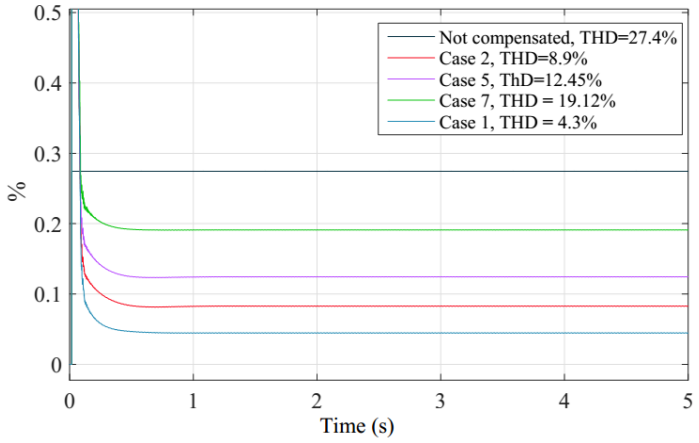


Figure 18. Harmonic distortion for Cases 1, 2, 5 and 7 from Table 2 and grid current without compensation.

3.2. Experimental Results

An APF prototype with selective harmonic compensation was built up, rated 1 kW three-phase combined with a non-linear load based on a three-phase diode rectifier with a controlled resistive load in the DC side of 48 Ω. The APF is connected to 40-V AC with a DC bus voltage of 150 V. The control algorithm consisting of the reference compensating current calculation and the proposed controller technique for selective harmonic compensation was implemented in the 32-bit digital signal processing F28335, at a switching frequency of 16 kHz. Figure 19 shows the setup used in the laboratory during prototype testing. Figure 20 shows the measured three-phase voltages, the measured grid current compensated and the original polluted load current measured for phase *a*. In this figure, the grid currents are compensated up to the 13th harmonic, as shown in Case 1 of Table 2. In general, the measured results in the APF prototype are quite similar to the calculated results in the computer simulations, which gives confidence in both the APF computational model and the experimental prototype. In order to illustrate the APF advantages in the case of selective harmonic control, the measured and calculated harmonics currents for Cases 7, 5, 2 and 1 in Table 2 are shown in Figures 16–19, respectively. Each of these cases tries to reduce the waveform distortion by using different strategies of harmonic compensation, leading to different THD improvements indexes. Observe in Figures 21–24 that measured and calculated currents have similar waveforms and that the THD is different for each case (Table 2), according to the strategy of harmonic compensation selected, as expected. From the different cases under analysis, the fifth harmonic has a greater impact in THD reduction. For example, in Case 2, the fifth harmonic is fully compensated in order to obtain a TDH = 10.8%. However, in Cases 5 and 7, the fifth harmonic is not fully compensated, and even though, the other harmonics are compensated, the THD is still higher than in Case 2. These experimental and computer simulations show the advantages of using a suitable strategy for harmonic compensation and THD improvement, where the selective harmonic compensation implemented in the proposed APF prototype is a useful tool (individual or group of harmonics).

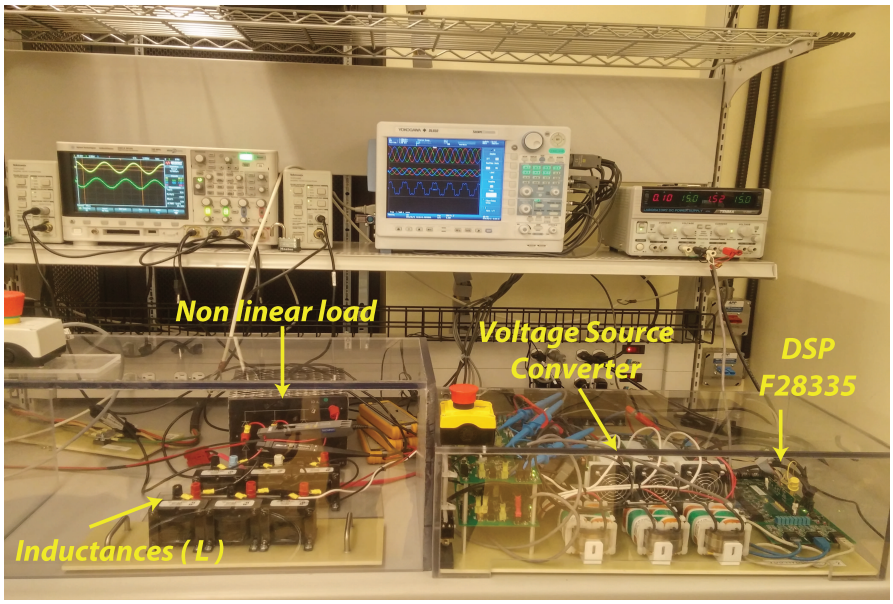


Figure 19. Laboratory setup used for the experiments.

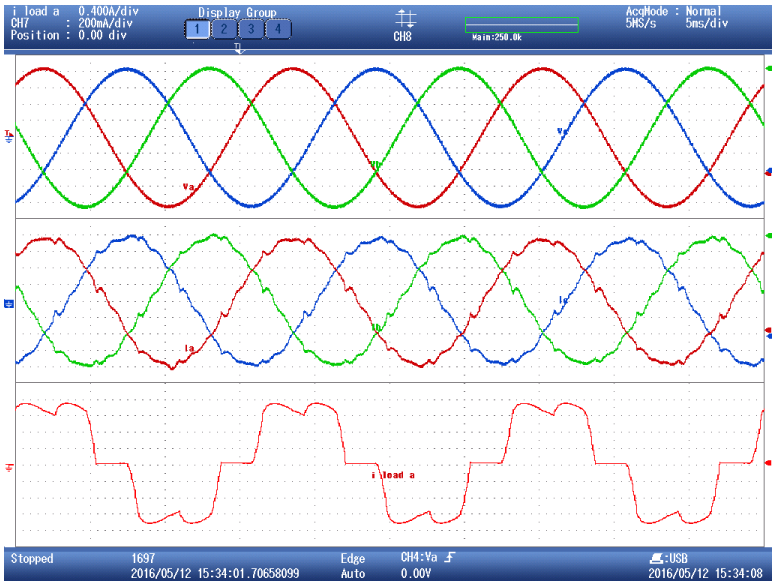
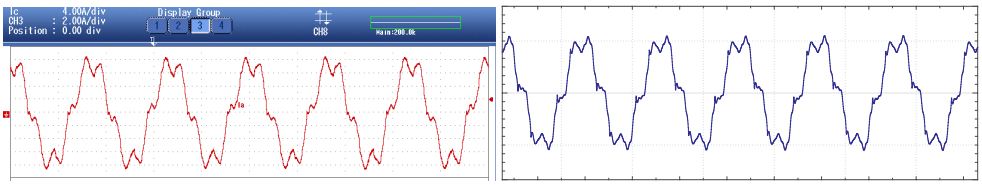
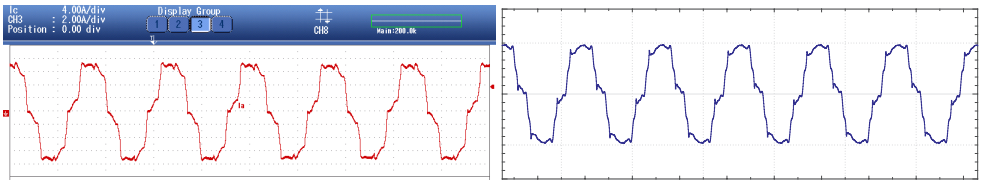


Figure 20. Three phase voltages, three-phase grid currents compensated and initial polluted current load in phase *a*.



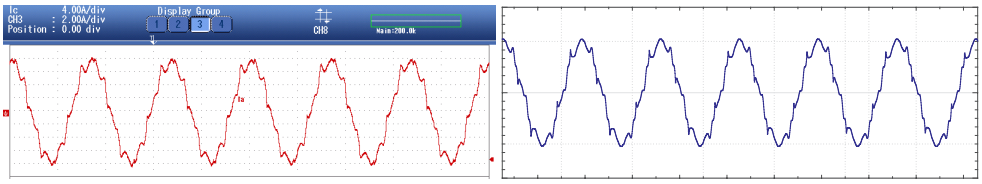
(a) (b)

Figure 21. Grid current waveform for Case 7, THD = 21.5%: (**a**) measured current; (**b**) simulated current.



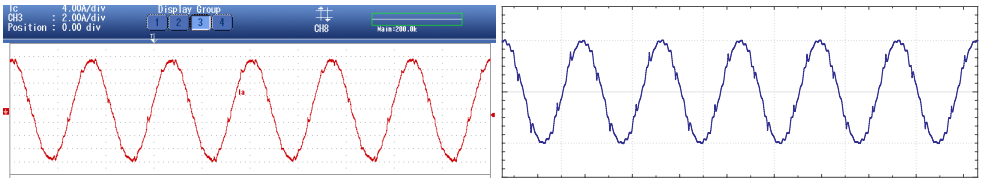
(a) (b)

Figure 22. Grid current waveform for Case 5, THD = 15.1%: (**a**) measured current; (**b**) simulated current.



(a) (b)

Figure 23. Grid current waveform for Case 2, THD = 10.8%: (**a**) measured current; (**b**) simulated current.



(a) (b)

Figure 24. Grid current waveform for Case 1, THD = 4.2%: (**a**) measured current; (**b**) simulated current.

4. Conclusions

This paper presents the development and assessment of a new APF for improving power quality and reactive compensation in domestic, commercial and industrial environments. The APF prototype is a three-phase, three-level NPC inverter with total or selective harmonic compensation capabilities using several SRF. The use of SRF combined with an LPF facilitates individual harmonic control using *d*-*q* signals. In general, the different design equations and control rules are easy to obtain and can be implemented in a straightforward manner. The use of several SRF controllers allows a selective harmonic compensation, which improves energy management after implementing a particular harmonic elimination strategy for a given scenery. Furthermore, the harmonic compensation is carried out without steady state error in a PI controller. A key stage in the APF performance is the accurate generation of any harmonic current, with low harmonic content. This is achieved by using three-level inverter and 3D-SVPWM techniques.

Due to the above characteristics, the proposed APF based in a three-level converter is an attractive alternative to be applied in power quality improvement at distribution and sub-transmission systems. Simulation and experimental results validate the design approach used and the general APF performance. This can be observed in the comparison of the simulated and measured result in the lab prototype.

Author Contributions: José Luis Monroy-Morales contributed to obtaining the selective harmonics compensation algorithm, experimental work and wrote part of the paper. David Campos-Gaona developed the DC voltage and reactive power control algorithm and also collaborated with the experimental work. Máximo Hernández-Ángeles designed the inner and outer controller and participated in the NPC topology. Rafael Peña-Alzola implemented the 3D-SVPWM and took part in the simulations results. José Leonardo Guardado-Zavala collaborated with the NPC multilevel topology, the analysis of the reference frames and wrote the paper. All authors reviewed the paper.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

AC	Alternating Current
APFs	Active Power Filters
DC	Direct Current
DSP	Digital Signal Processor
HVDC	High Voltage Direct Current
LPF	Low Pass Filter
NPC	Neutral Point Clamped
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SRF	Synchronous Rotating Frame
STATCOM	Static Synchronous Compensator
THD	Total Harmonic Distortion
VSC	Voltage Source Converter
3D-SVPWM	Three-Dimensional Space Vector Modulation

References

1. Hashempour, M.M.; Savaghebi, M.; Vasquez, J.C.; Guerrero, J.M. A control architecture to coordinate distributed generators and active power filters coexisting in a microgrid. *IEEE Trans. Smart Grid* **2016**, *7*, 2325–2336.
2. Cirrincione, M.; Pucci, M.; Vitale, G. A single-phase dg generation unit with shunt active power filter capability by adaptive neural filtering. *IEEE Trans. Ind. Electron.* **2008**, *55*, 2093–2110.
3. Zhang, C.; Chen, Q.; Zhao, Y.; Li, D.; Xiong, Y. A novel active power filter for high-voltage power distribution systems application. *IEEE Trans. Power Deliv.* **2007**, *22*, 911–918.
4. Kunjumuhammed, L.P.; Mishra, M.K. A control algorithm for single-phase active power filter under non-stiff voltage source. *IEEE Trans. Power Electron.* **2006**, *21*, 822–825..
5. Singh, B.; Al-Haddad, K.; Chandra, A. A review of active filters for power quality improvement. *IEEE Trans. Ind. Electron.* **1999**, *46*, 960–971.
6. Santos, W.R.N.; De Moura Fernandes, E.; Da Silva, E.R.C.; Jacobina, C.B.; Oliveira, A.C.; Santos, P.M. Transformerless single-phase universal active filter with ups features and reduced number of electronic power switches. *IEEE Trans. Power Electron.* **2016**, *31*, 4111–4120.
7. Mannen, T.; Fujita, H. A dc capacitor voltage control method for active power filters using modified reference including the theoretically derived voltage ripple. *IEEE Trans. Ind. Appl.* **2016**, *52*, 4179–4187.
8. Du, T.; Chen, Y.; Sun, S.; Wang, J. Design of Active Power Filter Control System Based on DSP. In Proceedings of the Second International Conference on Intelligent Networks and Intelligent Systems, Tianjin, China, 1–3 November 2009; pp. 585–588.
9. Xiao, J.; Zhang, X.; Wen, S.; Liu, Z. Active power filter design for improving power quality. In Proceedings of the International Conference on advanced mechatronic Systems, Beijing, China, 22–24 August 2015.
10. Nohra, A.F.H.; Kanaan, H.Y.; Fadel, M. A Control Strategy in Active Power Filter for System Quality Improvement. In Proceedings of the 2nd IEEE Conference on Power Engineering and Renewable Energy (ICPERE), Bali, Indonesia, 9–11 December 2014.
11. Antoniewicz, K.; Jasiski, M.; Kamierkowski, M.P. Model predictive control of three-level four-leg flying capacitor converter operating as shunt active power filter. In Proceedings of the IEEE International Conference on Industrial Technology (ICIT), Seville, Spain, 17–19 March 2015; pp. 2288–2294.
12. Akagi, H.; Kanazawa, Y.; Nabae, A. Instantaneous reactive power compensators comprising switching devices without energy storage components. *IEEE Trans. Ind. Appl.* **1984**, *IA-20*, 625–630.
13. Bhattacharya, S.; Divan, D. Synchronous frame based controller implementation for a hybrid series active filter system. In Proceedings of the Thirtieth IAS Annual Industry Applications Conference, Orlando, FL, USA, 8–12 October 1995.
14. Wu, J.C.; Jou, H.L. Simplified control method for the singlephase active power filter. *IEE Proc. Electr. Power Appl.* **1996**, *143*, 219–224.
15. Wang, L.; Lam, C.S.; Wong, M.C.; Dai, N.Y.; Lao, K.W.; Wong, C.K. Non-linear adaptive hysteresis band pulsewidth modulation control for hybrid active power filters to reduce switching loss. *IET Power Electron.* **2015**, *8*, 2156–2167.
16. Kuo, H.H.; Yeh, S.N.; Hwang, J.C. Novel analytical model for design and implementation of three-phase active power filter controller. *IEE Proc. Electr. Power Appl.* **2001**, *148*, 369–383.
17. Zhou, K.; Wang, D. Relationship between space-vector modulation and three-phase carrier-based pwm: A comprehensive analysis [three-phase inverters]. *IEEE Trans. Ind. Electron.* **2002**, *49*, 186–196.
18. Ahmed, W.; Syed, M.U.A.; Franquelo, L.G.; Prats, M.M.; Kolomyjski, W. Comparative study of SVPWM (space vector pulse width modulation) and SPWM (sinusoidal pulse width modulation) based three phase voltage source inverters for variable speed drive. *Mater. Sci. Eng.* **2013**, doi:10.1088/1757-899X/51/1/012027.
19. Leon, J.I.; Portillo, R.; Franquelo, L.G.; Prats, M.M.; Kolomyjski, W. New state vectors selection using space vector modulation in three dimensional control regions for multilevel converters. *IEEE Int. Symp. Ind. Electron.* **2006**, *2*, 1376–1381.

20. Xiang, L.; YunXiang, X.; Yu, W. A Simplified 3D-SVPWM Algorithm for Three-phase Four-wire Shunt Active Power Filter. In Proceedings of the International Conference on Electrical Machines and Systems (ICEMS), Hangzhou, China, 22–25 October 2014; pp. 1457–1462.
21. Lin, X.; Gao, S.; Li, J.; Lei, H.; Kang, Y. A new control strategy to balance neutral-point voltage in three-level npc inverter. In Proceedings of the 2011 IEEE 8th International Conference on Power Electronics and ECCE Asia (ICPE ECCE), Jeju, Korea, 30 May–3 June 2011; pp. 2593–2597.
22. Rodriguez, J.; Bernet, S.; Steimer, P.K.; Lizama, I.E. A survey on neutral-point-clamped inverters. *IEEE Trans. Ind. Electron.* **2010**, *57*, 2219–2230.
23. Albatran, S.; Fu, Y.; Albanna, A. Comprehensive mathematical description and harmonic analysis of hybrid two-dimensional–three-dimensional space vector modulation. *IEEE Trans. Ind. Electron.* **2014**, *61*, 3327–3336.
24. Muangjai, W.; Premrudeepreechacharn, S. Implementation of a carrier-based three-dimensional space vector pwm technique for three-phase four-leg voltage source converter with microcontroller. In Proceedings of the 4th IEEE Conference on Industrial Electronics and Applications, Xi'an, China, 25–27 May 2009; pp. 837–841.
25. Renge, M.M.; Suryawanshi, H.M. Three-dimensional spacevector modulation to reduce common-mode voltage for multilevel inverter. *IEEE Trans. Ind. Electron.* **2010**, *57*, 2324–2331.
26. Gonzalez, R.; Gubia, E.; Lopez, J.; Marroyo, L. Transformerless single-phase multilevel-based photovoltaic inverter. *IEEE Trans. Ind. Electron.* **2008**, *55*, 2694–2702.
27. Alepuz, S.; Busquets-Monge, S.; Bordonau, J.; Gago, J.; Gonzalez, D.; Balcells, J. Interfacing renewable energy sources to the utility grid using a three-level inverter. *IEEE Trans. Ind. Electron.* **2006**, *53*, 1504–1511.
28. Carrasco, J.M.; Franquelo, L.G.; Bialasiewicz, J.T.; Galvan, E.; PortilloGuisado, R.C.; Prats, M.A.M.; Leon, J.I.; Moreno-Alfonso, N. Power-electronic systems for the grid integration of renewable energy sources: A survey. *IEEE Trans. Ind. Electron.* **2006**, *53*, 1002–1016.
29. Kouro, S.; Malinowski, M.; Gopakumar, K.; Pou, J.; Franquelo, L.G.; Wu, B.; Rodriguez, J.; Perez, M.A.; Leon, J.I. Recent advances and industrial applications of multilevel converters. *IEEE Trans. Ind. Electron.* **2010**, *57*, 2553–2580.
30. Barros, J.D.; Silva, J.F.A.; Jesus, G.A. Fast-predictive optimal control of npc multilevel converters. *IEEE Trans. Ind. Electron.* **2013**, *60*, 619–627.
31. Honade, T.; Udapure, S.; Timande, S.; Rodge, S. Comparative study between two and three level converter for electric application. *Int. J. Adv. Eng. Technol.* **2016**, *9*, 210–217.
32. Goetz, S.; Zhongxi, L.; Liang, X.; Zhang, C.; Lukic, M.; Peterchev, A.V. Control of modular multilevel converter with parallel connectivity—Application to battery system. *IEEE Trans. Power Electron.* **2016**, doi:10.1109/TPEL.2016.2645884.
33. Sanz, I.; Moranchel, M.; Bueno, E.J.; Rodriguez, F.J. Analysis of medium voltage modular multilevel converters for FACTS applications. In Proceedings of the 42nd IEEE Annual Conference of the Industrial Electronics Society (IECON), Florence, Italy, 23–26 October 2016; pp. 6459–6464.
34. Boppana, S.; Mangadevi Relangi, V.; Bueno Rao, S. Hybrid asymmetrical multilevel inverter for hybrid wind-PV power generation system. In Proceedings of the International Conference on Electrical, Electronics, Signals, Communication and Optimization (EESCO), Visakhapatnam, India, 24–25 January 2015; pp. 1–6.
35. Aissani, M.; Aliouane, K. Three-Dimensional Space Vector Modulation for Four-Leg Voltage-Source Converter used as an active compensator. In Proceedings of the International Symposium on Power Electronics, Electrical Drives, Automation and Motion, Pisa, Italy, 14–16 June 2010; pp. 1416–1421.
36. Suh, J.-H.; Choi, C.-H.; Hyun, D.-S. A new simplified space-vector pwm method for three-level inverters. In Proceedings of the Fourteenth Annual Applied Power Electronics Conference and Exposition (APEC '99), Dallas, TX, USA, 14–18 March 1999; pp. 515–520.
37. Franquelo, L.G.; Prats, M.A.M.; Portillo, R.C.; Galvan, J.I.L.; Perales, M.A.; Carrasco, J.M.; Diez, E.G.; Jimenez, J.L.M. Three-dimensional space-vector modulation algorithm for four-leg multilevel converters using abc coordinates. *IEEE Trans. Ind. Electron.* **2006**, *53*, 458–466.
38. Asiminoaei, L.; Blaabjerg, F.; Hansen, S. Evaluation of Harmonic Detection Methods for Active Power Filter Applications. In Proceedings of the Twentieth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Austin, TX, USA, 6–10 March 2005; pp. 635–641.

39. Martín Prats, M.A.; Franquelo, L.G.; Portillo, R.; León, J.I.; Galván, E.; Carrasco, J.M. A 3-D Space Vector Modulation Generalized Algorithm for Multilevel Converters. *IEEE Power Electron. Lett.* **2003**, *1*, 110–114.
40. Leon, J.I.; Vazquez, S.; Portillo, R.; Franquelo, L.G.; Carrasco, J.M.; Wheeler, P.W.; Watson, A.J. Three-dimensional feedforward space vector modulation applied to multilevel diode clamped converters. *IEEE Trans. Ind. Electron.* **2009**, *56*, 101–109.