

MMC with parallel-connected MOSFETs as an alternative to wide bandgap converters for LVDC distribution networks

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Abstract: Low-voltage direct-current (LVDC) networks offer improved conductor utilisation on existing infrastructure and reduced conversion stages, which can lead to a simpler and more efficient distribution network. However, LVDC networks must continue to support AC loads, requiring efficient, low-distortion DC–AC converters. Additionally, increasing numbers of DC loads on the LVAC network require controlled, low-distortion, unity power factor AC–DC converters with large capacity, and bi-directional capability. An AC–DC/DC–AC converter design is therefore proposed in this study to minimise conversion loss and maximise power quality. Comparative analysis is performed for a conventional IGBT two-level converter, a SiC MOSFET two-level converter, a Si MOSFET modular multi-level converter (MMC) and a GaN HEMT MMC, in terms of power loss, reliability, fault tolerance, converter cost and heatsink size. The analysis indicates that the five-level MMC with parallel-connected Si MOSFETs is an efficient, cost-effective converter for low-voltage converter applications. MMC converters suffer negligible switching loss, which enables reduced device switching without loss penalty from increased harmonics and filtering. Optimal extent of parallel-connection for MOSFETs in an MMC is investigated. Experimental results are presented to show the reduction in device stress and electromagnetic interference generating transients through the use of reduced switching and device parallel-connection.

1 Introduction

There have been reported cases of distribution networks operating close to their capacity limits [1]. DC networks are being suggested as a means of addressing the issue of converter rich AC networks and improving conductor utilisation, thus increasing network capacity using existing infrastructure. Reports state that low-voltage direct-current (LVDC) technology could provide large power capacities without replacing the existing cables [2–4]. Furthermore, LVDC networks present the additional benefit of no reactive power flow and allow reduction in the number of conversion stages [5–7]. However, these systems will retain the need to supply local AC loads which must be provided by DC–AC converters meeting the same stringent performance criteria outlined above for AC–DC converters supplying DC loads such as electric vehicles (EVs). Issues of power quality also affect LVDC networks and are complicated by the need to suppress DC harmonics associated with single-phase loads and to have resilience to DC network faults.

Meanwhile, increasing load demands, distributed generation, and the growing use of electricity for heating and vehicle transport contribute significant strains on existing LVAC distribution networks [1]. These increasing numbers of DC loads require controlled low distortion, unity power factor AC–DC converters with increasing capacities as well as bi-directional capacity. In the UK, statistics show that full penetration of EVs is predicted to increase total electricity consumption by ~50% [8]. EV chargers present much high power loads operating at higher frequency and higher voltage than the existing numerous lighter power electronic loads (such as PC's, phone chargers etc.), driving a need to facilitate the adoption of high performance converters capable of handling high power, frequency and voltage. These loads must be supplied whilst meeting strict harmonic limits and avoiding issues of circulating currents and control band oscillations associated with power electronic rich networks. This growth drives a critical need for improved converter performance in terms of efficiency, power quality and control.

The consequent number of converters required, when LVDC networks are combined with high numbers of EVs, further increases the pressure to improve converter efficiency as losses from

thousands of converters accumulate, and underlines the imperative to meet strict harmonic standards to ensure continued grid stability [9–11]. To date, higher power applications have been met using two-level insulated-gate bipolar transistor (IGBT) inverters, however IGBT devices are now at the limit of performance. Two solutions can be proposed for this. Wide bandgap (WBG) devices are now available with appropriate voltage and power ratings. The exploitation of WBG fast switching behaviour can be used to increase modulating frequency while simultaneously increasing efficiency compared with IGBT. Higher modulating frequency in turn allows smaller, lower loss filters. Basic circuit topology remains unchanged but the devices are expensive and their high speed can introduce electromagnetic interference (EMI) issues [12]. Gate drivers for very fast switching devices can also be challenging to implement [13]. Alternatively, improved control and power quality can be facilitated at lower switching frequency by improvements in the converter output waveform, by using a stepped waveform such as that generated the modular multi-level converter (MMC) topology. A stepped waveform reduces the harmonic content of the output current and voltage, which allows a reduction in filter size and complexity and leads to reduced VAR consumption, simplified control, reduced circulating harmonic/reactive current, greater stability and less filter damping loss.

Multi-level converters allow the decoupling of power quality and device switching frequency. They offer the potential to drive down conversion loss but have received little attention at low voltage due to the apparent increase in complexity. This paper will investigate the potential benefits and limitations of multi-level techniques in comparison to the extension of two-level converters through the use of WBG devices.

In this study, a DC voltage of 600 V is selected with 10 kW, single-phase power transfer. There are many suitable converter topologies at this voltage, each with different advantages, and hence this research aims to provide a comparison of converter topologies, comparing efficiency, volume and reliability, for converters capable of meeting strict harmonic standards. Generally, the complexity of the circuit topology and the large number of capacitors required are the main limits of using flying

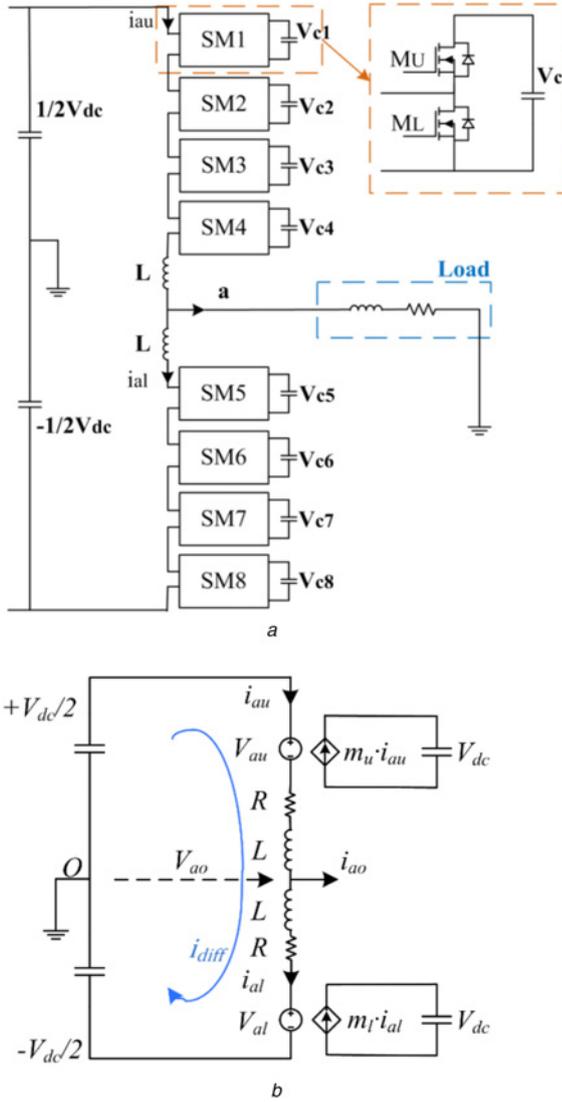


Fig. 1 Topology of a five-level MMC and average model of an MMC
a Topology of a Si MOSFET five-level MMC
b Average model of an MMC

capacitor converters [14]. For neutral point clamped (NPC) converters, additional inverter control may be required to balance the neutral point. The losses are not equally distributed in NPC converters, thus limiting current rating by the most stressed semiconductor devices [15, 16].

Three principal converters stand out as being the most suitable, innovative solutions for this application: Si metal–oxide–semiconductor field-effect transistor (MOSFET) MMC, GaN high-electron-mobility transistor (HEMT) MMC and SiC two-level [17]. Selecting which of these converters brings the best performance is non-trivial as efficiency is affected not only by semiconductor losses but also by the filtering required to meet harmonic standards. This research optimises the design of the three converters including filtering, and validates the outcome of the comparisons using experimental results for SiC and Si MOSFET. Discussion on reliability and fault tolerance differences between the three converters is also included, as well as a comparison of required heatsink volume.

Expected benefits of the low-voltage (LV) MMC as an alternative to two-level converters are summarised as: (i) continuous arm currents, (ii) negligible switching loss, allowing slowed switching, leading to reduced dv/dt , (iii) modular construction, (iv) no need of a DC-side filter, (v) better output waveform quality leading to

smaller AC filters, (vi) negligible switching losses and (vii) the ability to prevent capacitor discharging current. The modular structure of the MMC allows the use of lower voltage rated Si MOSFETs in place of IGBTs, allowing further loss reduction through parallel connection and synchronous rectification.

The two-level Si MOSFET converter is excluded because a Si MOSFET (≥ 600 V) has a larger power dissipation than an IGBT [18, 19].

2 Design optimisation for low-voltage converters: Si MOSFET MMC, GaN HEMT MMC and SiC two-level

2.1 Operating principle and component sizing of LV MMC type converter

2.1.1 Operating principle: The topology of a five-level MMC, where four submodules and one arm inductor form one arm, is shown in Fig. 1a. Fig. 1b illustrates the average model of a single-phase MMC. In each arm, R represents the semiconductors ohmic loss [20, 21].

This paper assumes that current suppression control eliminates all harmonics and the remaining circulating current (i_{diff}) has only a DC component I_{dc} . According to [22], arm currents can be expressed as (1) and (2), where I_{dc} is the DC component of i_{diff} and i_{ao} is the sinusoidal output current

$$i_{au} = i_{diff} + \frac{i_{ao}}{2} = I_{dc} + \frac{i_{ao}}{2} \quad (1)$$

$$i_{al} = i_{diff} - \frac{i_{ao}}{2} = I_{dc} - \frac{i_{ao}}{2} \quad (2)$$

2.1.2 Design of passive components (sizing capacitors and inductors): To reduce MMC bulk, capacitance is set to the minimum required to stay within $\pm 10\%$ voltage fluctuation [23]. The submodule capacitance, C_{sub} , is sized based on maximum energy deviation [24] (adapted for a two-phase-leg topology), so that submodule capacitance is given by (3) [25], where n is the number of submodules in one arm, ΔV_{max} is maximum voltage difference in p.u., M is the modulation index and $|\bar{S}|$ is apparent power

$$C_{sub} = \frac{n \cdot |\bar{S}|}{2\omega \cdot M \cdot V_{dc}^2 \cdot \Delta V_{max}} \quad (3)$$

While current suppression control effectively reduces second harmonic distortion, circulating currents at switching frequency can only be suppressed by arm inductance, since switching frequency exceeds controller bandwidth [24].

The difference between phase leg voltage and V_{dc} results in circulating current. If arm currents are dominated by DC and fundamental components (1) and (2), the voltage difference u_{diff} is given by the following equation [20]

$$\begin{aligned} u_{diff} &= \frac{V_{dc} - (v_{au} + v_{al})}{2} \\ &= \frac{n}{8C_{sub}} \left\{ -\frac{3}{4\omega} M \cdot I_{ao} \cdot \sin(2\omega t - \varphi) + \frac{1}{\omega} M^2 I_{dc} \cdot \sin(2\omega t) \right\} \end{aligned} \quad (4)$$

Peak-to-peak circulating current at the switching frequency is given by the following equation

$$I_{pp} = \frac{u_{diff}}{L_{arm}} \cdot \Delta T \quad (5)$$

ΔT is the time between switching, with its largest value equal to the inverse of switching frequency $1/f_s$, and the maximum value of I_{pp}

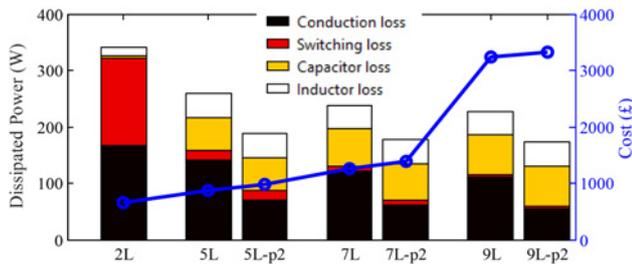


Fig. 2 Power loss and cost comparison for H-bridge two-level IGBT converter and different levels of Si MOSFET MMC at $M=0.57$, 10 kHz, 10 kW and unity power factor. 2L = two-level IGBT; 5L/7L/9L = five/seven/nine-level MMC without parallel connection; 5L-p2/7L-p2/9L-p2 = five/seven/nine-level MMC with two parallel-connected devices

is limited to 5% of the DC side current $I_d = 2I_{dc}$

$$I_{pp_max} = 0.05 \cdot I_d = 0.05 \cdot 2I_{dc} = 0.1I_{dc} \quad (6)$$

Minimum arm inductance is given by the following equation [25]

$$L_{arm} = \frac{5n}{4\omega C_{sub}f_s} \cdot \sqrt{(M^2 - 3)^2 + 9\tan^2\varphi} \quad (7)$$

2.2 Si MOSFET five-level MMC

According to [25], 18 mF capacitors are chosen for the two-level converter, which is calculated from the peak-to-peak energy deviation. By using (3), the required C_{sub} for different levels of MMC at $M=0.57$ (240 V_{rms} output) can be obtained and the calculated losses are compared in Fig. 2.

Interestingly, with increasing number of MMC levels, capacitor losses are almost constant, while semiconductor losses decrease gradually. Parallel-connection of ≥ 2 MOSFETs reduces conduction loss dramatically. Converter power loss calculation will be presented in Section 3.

Fig. 2 shows how converter cost increases significantly with higher converter levels, dominated by capacitor costs. Significant capacitor loss means that simply increasing the number of levels is counterproductive for efficiency, while also adding complexity, volume and cost. The five-level MMC with parallel-connected Si MOSFETs provides the optimum balance between control complexity, losses and costs.

2.3 GaN HEMT three-level MMC

Comparing available GaN HEMT devices showed that a GaN three-level MMC using 650 V GS66516T devices promises highest efficiency, as illustrated in Table 1.

2.4 SiC two-level converter

With higher breakdown voltage [14], lower R_{on} and very low diode recovery loss, SiC MOSFETs are increasingly adopted for high efficiency. For LVDC at 600 V_{dc} a two-level converter is the most efficient SiC MOSFET topology. The 1.7 kV Cree CAS300M17BM2 device provides low R_{on} , as shown in Table 1.

3 Converter power loss estimation

3.1 Semiconductor losses

MOSFET and GaN transistor conduction loss is given by (8), assuming synchronous rectification [26, 27]

$$P_{con} = \frac{1}{T} \int_0^T (i_{DS}(t))^2 \cdot R_{on} dt \quad (8)$$

where i_{DS} is the drain-source current. R_{on} is the on-state resistance, given by the following equation [28]

$$R_{on} = R_{on_{25}} + k_{R_{on}} \cdot (T_j - 25) \quad (9)$$

where $R_{on_{25}}$ gives R_{on} at 25°C and $k_{R_{on}}$ is a coefficient obtained from the datasheet.

Interpolation of SiC datasheet switching loss predicted far lower loss than experimental SiC switching loss measured by the authors. Measured SiC switching loss at 600 V_{dc} is presented in Section 5.1, and is used for all loss comparisons.

Si MOSFET and GaN transistor switching loss is given by the following equation [29, 30]

$$P_{sw} = \frac{1}{2} I_{DS} V_{DS} (t_{off} + t_{on}) f_s \quad (10)$$

where t_{on} and t_{off} are the turn-on and turn-off times, respectively, and are obtained from switching gate charge Q_{sw} and average gate current I_{GS} [31]

$$t_{on} = t_{off} = \frac{Q_{sw}}{I_{GS}} \quad (11)$$

I_{GS} can be approximated by the Miller plateau gate current

$$I_{GS} = \frac{V_{GS} - V_P}{R_g} \quad (12)$$

where V_P is the Miller plateau voltage, and R_g denotes total gate resistance.

Diode switching loss is

$$P_{rr_D} = Q_{rr} \cdot V_D \cdot f_s \quad (13)$$

3.2 Capacitor loss calculation

At ≤ 400 V, electrolytic capacitors achieve small volume, but bulkier film capacitors provide low equivalent series resistance (ESR). A comparison between electrolytic and film capacitors in Table 2 reveals that with film capacitors, capacitor loss is almost eliminated at a cost of increased weight and volume. Currently, lower voltage film capacitors are unavailable so parameters in the second row of Table 2 are estimates provided by API capacitors.

For the MMC, submodule capacitor losses in upper and lower arms are given by (14) and (15), respectively

$$\bar{P}_{cap_U} = \frac{1}{2\pi} \int_0^{2\pi} m_u \cdot (i_{au}^2 \cdot ESR) d(\omega t) \quad (14)$$

$$\bar{P}_{cap_L} = \frac{1}{2\pi} \int_0^{2\pi} m_l \cdot (i_{al}^2 \cdot ESR) d(\omega t) \quad (15)$$

For the SiC two-level converter, loss occurs in the DC-side capacitor. Using peak energy deviation [24, 25] it can be shown that the required capacitance is given by the following equation

$$C_{dc} = \frac{\Delta E_{dc}}{4V_{dc}^2 \Delta V_{max}} \quad (16)$$

DC-side capacitor current, $i_{cap}(t)$, is assumed to contain all of the AC components of the upper switch current

$$i_{cap}(t) = \frac{1}{2} I_{ao} \sin(\omega t - \varphi) - \frac{1}{4} M I_{ao} \cos(2\omega t - \varphi) \quad (17)$$

Table 1 Parameter comparison between different types of devices

	SiC MOSFET		GaN HEMT			Si MOSFET	
available voltage ratings	1.7 kV^a	1.2 kV	650 V^a	100 V	400 V	200 V^a	100 V
no. of levels	two-level	two-level	three-level	nine-level	three-level	five-level	nine-level
device	CAS300M17BM2	C2M0025120D	GS66516T	GS61008T	IRFP360	IRFP4668	IRFP4110
R_{on} , m Ω	8	25	27	7.4	200	8	3.7

^aDevices selected in this study.

DC-side capacitor loss is then found from the following equation

$$P_{C_{dc}} = \frac{1}{2\pi} \int_0^{2\pi} \left(i_{cap}^2(t) \cdot ESR \right) d(\omega t) \quad (18)$$

3.3 Inductor loss

3.3.1 MMC arm inductor loss: Using (10) and (14), the minimum arm inductance for a 10 kW, $M=0.57$, $f_s=10$ kHz, $V_{dc}=600$ V, $\Delta V_{max}=0.1$ MMC operating at unity power factor is 1.5 mH. Air-gapped Blinzinger ferrite E160/56/36 cores [33] were used to minimise inductor loss. Inductor loss is calculated using (21) and (22)

$$\sqrt{I_{dc}^2 + \left(\frac{I_{a0}}{2} \right)^2} = 22.4 \text{ A} \quad (19)$$

$$P_{copper_arm} = I_{dc}^2 R_{wire} + \frac{(I_{a0}/2)^2}{2} R_{wire} = 47.8 \text{ W} \quad (20)$$

Harmonic analysis calculations show that ferrite core loss may be neglected. With four arm inductors in total, MMC inductor loss is 192 W regardless of the number of levels.

3.3.2 Two-level converter inductor loss: Analysis of single-phase two-level converter harmonic performance showed that 1.7 mH of AC-side inductance is required to maintain harmonics below 5% of fundamental current. Blinzinger E160/56/36 cores [33] were used again. Harmonic analysis of the two-level converter with 1.7 mH of converter-side inductance showed significant harmonics at the switching frequency of 10 kHz, and hence with skin effect, total loss in the AC-side inductor is 268 W.

In addition, to keep DC-side currents below 5% of DC input current, a DC-side inductance of 6.5 mH is required. Using the Blinzinger E160/56/36 cores again total DC-side inductor loss is estimated to be 88.5 W.

Total inductor loss for the two-level converter is therefore 356.5 W.

4 Comparative study of converters

Three converter topologies based on Si MOSFET, SiC and GaN devices are proposed. Parallel connection of switching devices is explored to reduce conduction losses and heatsink sizes are compared.

Table 2 Comparison between electrolytic and film capacitors

	Capacitance, μF	Voltage, V	Weight, g	Volume, cc	ESR, m Ω	Part number
electrolytic	2200	350	280	221	28	B43456A4228M000
film	2300	250	370	420	0.8	estimated by <i>API Capacitors</i> ^a
	2400	450	1985	1613	0.2	DCHCH07240JH00KS00
	2030	600	1760	1480	1.6	DCP6107203ER00

This product is not available for sale. Parameters are estimated by *API Capacitors* [32].

4.1 Power loss – optimal number of parallel-connected devices

As shown in Fig. 2, parallel connection can significantly reduce converter losses. With many parallel-connected devices, the effect of track resistance becomes more significant [30], imposing a limit on parallel connection. In addition, this section discusses the current unbalance limits for parallel connection.

Power losses for different numbers of parallel-connected devices are plotted in Fig. 3. Track resistance is seen to roughly limit the benefit of parallel connection, with respect to efficiency, to four devices. With four IRFP4668 devices in parallel, total current rating is now 800 A, bringing strong potential reliability benefits to the Si MOSFET MMC in terms of device stress compared with the SiC module current limit of 300 A, and a current limit of 240 A for GaN three-level MMC with four parallel devices.

For the MMC, low switching loss permits slower turn-on/off without undue impact on loss, enabling a lower EMI solution [27], in contrast to the SiC two-level converter where high switching loss prohibits slow turn-on/off.

In Fig. 3a, the Si and GaN MMC offer lowest loss. Device packaging and footprint area impact parasitic resistance and inductance incurred by parallel connection. For an LVDC MMC converter using Si MOSFETs all devices are available in TO-247 packaging. Laying out four TO-247 devices in the most efficient manner leads to a volume of around 16 cm³ which is around 21% of the predicted heatsink volume. Hence, for around four devices in parallel, device packaging and size are a lesser concern compared with gate-drive complexity and efficiency when establishing optimal parallel connection. For four TO-247 devices laid out efficiently and using slowed switching, gate threshold tolerances have far more impact on switching synchronisation than different gate track lengths imposed by layout, hence efficiency dictates optimal parallel connection for Si MOSFETs. Switch timing is experimentally investigated below.

Parallel connection of many surface mount GaN devices may be more practical. However, currently GaN devices are expensive, and the diminishing improvement in efficiency with increased parallel connection beyond four to six must be considered alongside the expense of more devices.

4.2 Reliability

The luxury of being able to reduce switching speed in both Si and GaN MMC also improves reliability by allowing switching transients to be reduced and hence minimising voltage stress due to overshoot, as will be demonstrated in Section 5. In addition,

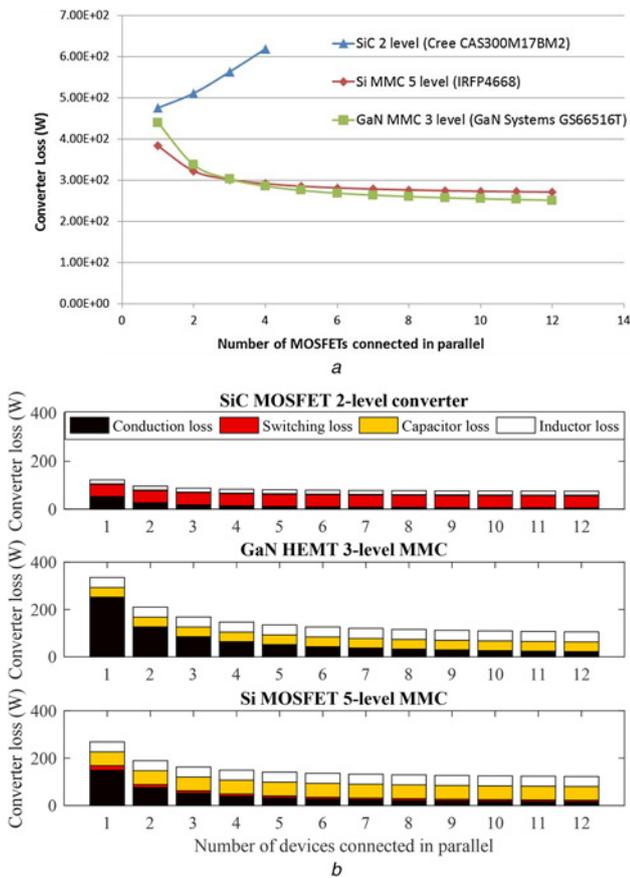


Fig. 3 Losses in converters with parallel-connected devices for an SiC MOSFET two-level converter, a GaN HEMT three-level and a Si MOSFET five-level MMC at 10 kW, 10 kHz, 600 V_{dc}, $M = 0.57$ and unity power factor
a Converter loss as a function of the number of parallel-connected devices
b Converter loss distribution as a function of the number of parallel-connected devices

the availability of low-cost, high current rating Si MOSFETs minimises current related device stress. Since device stress is a significant cause of converter failure, converter reliability seems likely to noticeably improve with the use of Si or GaN MMC, thus mitigating any reduction in reliability that can be attributed to increased complexity.

In [34], for photovoltaic applications, it is concluded that SiC offers a superior solution to Si IGBT due to a combination of lower life-cycle costs, lower part count, higher efficiency and power density. In [35], gate reliability of SiC power devices is found to be problematic, however, [36] suggests that up to date SiC devices suffer reduced gate reliability issues.

GaN brings the advantage of very fast switching, but this comes at the cost of increased gate-drive complexity, and increased risk of oscillation [13], both of which are likely to impact reliability. Mean time to failure for the Si MOSFET is around 1.5×10^3 h [37], while with GaN it is around 1.9×10^6 h [38], suggesting that the GaN power devices are less reliable.

Table 3 Heatsink sizing for the IGBT two-level converter

	P_{arm} , W	$R_{\theta(I-S)}$, °C/W	Required $R_{\theta(S-A)}$, °C/W
IGBT	59.2	0.51	0.71
diode	21	0.61	
Heatsink	$h \times w \times l$, mm	Volume, cm ³	Heatsink $R_{\theta(S-A)}$, °C/W
FISCHER ELEKTRONIK SK 47/100 SA	80 × 200 × 100	1600	0.7

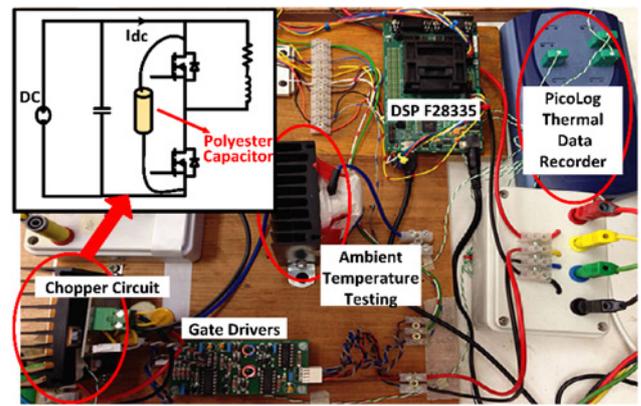


Fig. 4 Experimental test rig for power loss measurement

The SiC converter contains eight times fewer power switches than the Si MOSFET five-level MMC, and if the reliability of both semiconductor switch types were equal, and if we ignore the reduced stresses on the devices in the MMC topology, this would equate to an improvement in reliability of eight times. Hence, there is a complex balance required to compare the reliability of the converters. At this time, quantifying the potential reliability improvements offered by reduced voltage stress in MMC topologies and the relative impact of SiC gate reliability in two-level converters is an area of interest which longer term industrial studies will demonstrate in time.

4.3 Fault tolerance

The choice of converter topology will have implications for the fault response of LVDC networks, in particular severe pole-pole short circuits. The use of conventional two-level converters results in rapid rise in fault current associated with the discharge of converter DC side capacitance accompanied by AC fault contribution which builds through the converter body diodes as the DC voltage collapses below the envelope of the AC network [39]. Once the DC rail fully collapses both current components are transferred to the diode path placing significant stress on the converter power modules. Fast acting DC protection is therefore required to prevent both de-energisation of the network and damage to converters.

The impact of converter topology has seen significant research in high-voltage DC applications. The adoption of the MMC topology can prevent the capacitive discharge component of the DC fault current, however the basic topology is still subject to fault current through the module diodes. The use of reverse blocking converters such as the full-bridge and half-bridge MMC has the ability to block both capacitor discharge and AC contribution to the DC fault [40]. Improved fault behaviour is achieved at the expense of additional devices and conduction loss.

MMC-based converters can bring the same functionality to LVDC systems. In these cases, the lower operating voltage provides greater degrees of freedom in the design. For instance, mixed device ratings may allow the use of fewer reverse blocking cells giving fault tolerance while minimising impact on overall converter loss.

An additional interesting point is that parallel connection in MMC leads to high transient overload capacity allowing faults to trip conventional protection whilst at the same time reducing operational losses.

4.4 Cost

Fig. 2 demonstrates the impact of increasing number of levels on Si MOSFET MMC cost, giving a cost of around £1000 for the parallel-connected five-level case. For comparison, GaN three-level MMC costs around £1150, and SiC two-level converter around £1500. Si MOSFET MMC currently offers the lowest cost solution out of the three compared converters.

4.5 Thermal design and heatsink sizing

4.5.1 Deriving thermal resistance: Thermal design is carried out for 10 kW SiC MOSFET two-level, GaN HEMT three-level MMC and Si MOSFET five-level MMC converters with four parallel-connected devices (‘three converters’), and compared with a 10 kW IGBT two-level converter. To follow the approach in [26] most thermal resistances can be obtained from the datasheet. Only the Si MOSFET datasheet provides the case-to-heatsink thermal resistance, $R_{\theta(C-S)}$, which is affected by the contact quality [41]. SiC MOSFET/GaN HEMT $R_{\theta(C-S)}$ is estimated by the following equation

$$R_{\theta(C-S)SiC} = \frac{A_{Si}}{A_{SiC}} R_{\theta(C-S)Si} \quad (21)$$

where A_{Si} and A_{SiC} are the contact areas for the Si and SiC devices, and $R_{\theta(C-S)Si}$ is the datasheet Si MOSFET $R_{\theta(C-S)}$ [42].

To mount the optimal top-side cooled GaN HEMT device, a pedestal copper block is required [43], but the copper block has negligible thermal resistance.

4.5.2 Heatsink sizing: IGBT two-level converter losses in one arm with $M = 0.57$, $T_j = 125^\circ\text{C}$ are listed in Table 3, along with required heatsink volume.

Power loss and required heatsink volume are listed in Table 4 for the ‘three converters’. Despite similar loss in the GaN three-level MMC compared with the Si five-level converter, the small GaN transistor package leads to larger $R_{\theta(C-S)}$, and hence double the heatsink volume. Even when compared with GaN three-level MMC, the heatsink volume required for a conventional IGBT two-level converter is over ten times larger.

5 Experimental results and analysis

5.1 Thermal measurement for the validation of power loss calculation

5.1.1 Experimental validation of Si MOSFET loss calculation: Measurement of loss in the complete MMC is not practical, so loss in a single MMC module operating at fixed 50% duty cycle was measured instead. Loss was measured by first calibrating heat rise on the heatsink as a function of dissipated power by passing DC power through the Si MOSFET switches to calibrate temperature rise as a function of power loss in the switches. The experimental test rig is shown in Fig. 4, containing a single Si MOSFET MMC module with an $R-L$ load, at 100 V_{dc} and 1–20 A AC-side load current range, using IRFB4127PbF MOSFETs.

Fig. 5 shows the estimated and measured power dissipation for synchronous and non-synchronous rectification cases, highlighting the benefit that synchronous rectification brings for MOSFETs.

Table 4 Heatsink comparison between three converters with four parallel-connected devices (calculated for one-phase leg). Heatsink manufacturer: FISCHER ELEKTRONIK

Converter type	P_{arm} , W	$R_{\theta(I-S)}$, °C/W	Required $R_{\theta(S-A)}$, °C/W	Heatsink part no.	$R_{\theta(S-A)}$, °C/W	Volume, cm ³
SiC MOSFET two-level	33.1	0.072	2.95	SK 81/75 SA	2.5	112.5
GaN three-level MMC	32.1	0.68	2.44	SK 81/100 SA	2.1	150
Si MOSFET five-level MMC	24.4	0.53	3.57	SK 81/50 SA	3.0	75

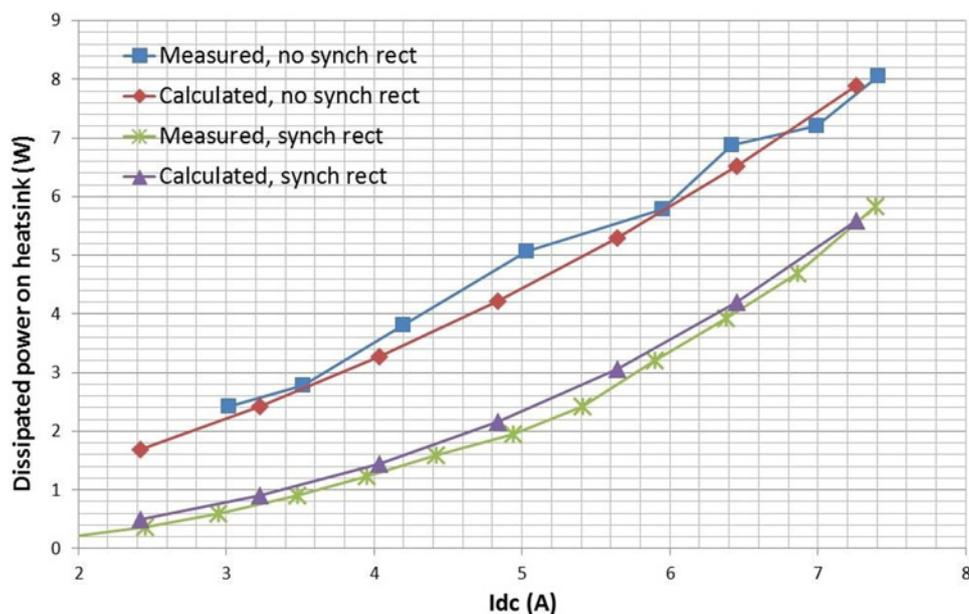


Fig. 5 Heat dissipation for one MMC submodule with and without synchronous rectification, allowing for track resistance

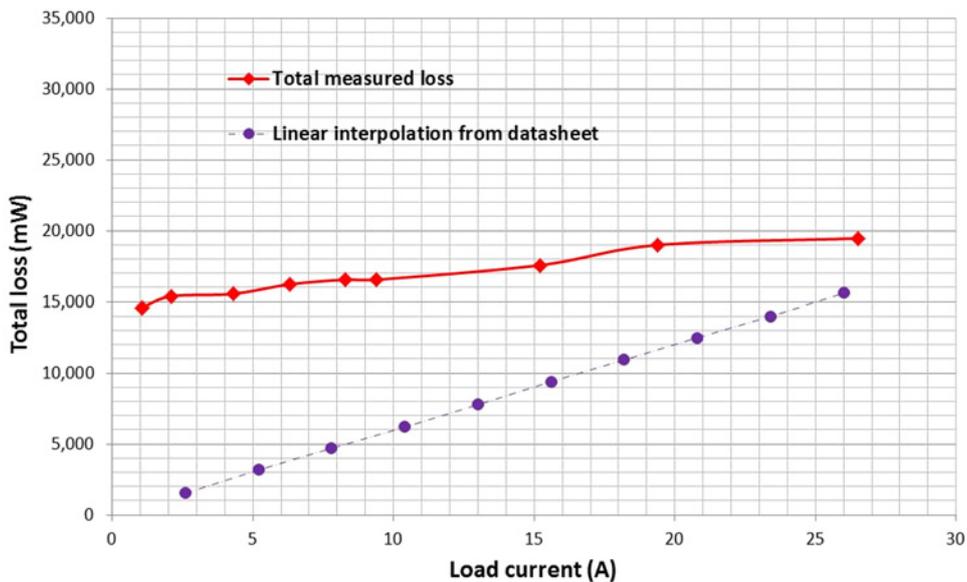


Fig. 6 Measured switching loss for the CAS300M17BM2 module, at 600 V, 10 kHz switching frequency

Track resistance power losses are included since device on-resistance is now so low that track resistance becomes relevant in a prototype such as was available during this study [27]. Fig. 5 shows that measured and calculated losses agree closely, validating the power loss calculation in Section 3.

5.1.2 Experimental measurement of SiC MOSFET loss: SiC losses were compared with losses calculated using interpolation

from datasheet switching loss. Heat rise for this large SiC module was found to be too small to measure accurately, however, smooth and relatively slow switching (compared with Si MOSFETs) allowed accurate determination of losses using conventional voltage and current measurements. Switching loss as a function of current is presented in Fig. 6, showing little variation in switching loss with load current at these low load currents. This is due to the dominance of capacitance effects in

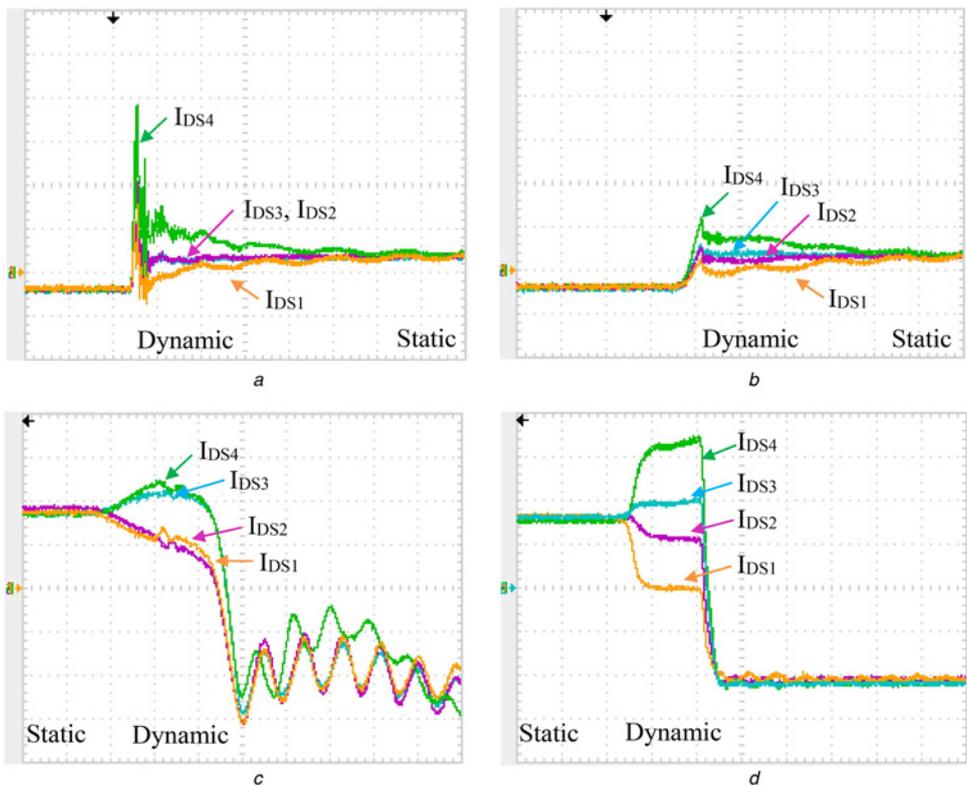


Fig. 7 Current sharing between four parallel-connected MOSFETs (IRFP4668s) with 16 A load current

- a Turn on with $R_G = 1 \Omega$ (1 $\mu\text{s}/\text{div}$, 5 A/div)
- b Turn on with $R_G = 100 \Omega$ (1 $\mu\text{s}/\text{div}$, 5 A/div)
- c Turn off with $R_G = 1 \Omega$ (100 ns/div, 1 A/div)
- d Turn off with $R_G = 100 \Omega$ (2.5 $\mu\text{s}/\text{div}$, 1 A/div)

SiC switching loss [44]. For accurate loss comparison with Si MOSFET devices measured switching loss was used to calculate SiC two-level converter efficiency. Conduction loss was found to agree with calculation.

5.2 Current sharing in parallel-connected MOSFETs

Parallel-connected devices are very desirable in MMC to reduce on-resistance since low device switching frequency of MMC means conduction loss dominates over switching loss. However, parallel connection of MOSFETs risks increased damage to devices during switching transitions if oscillations exist between parallel-connected devices. It is therefore important to investigate the behaviour of parallel-connected MOSFETs, and explore options to mitigate the risks caused by transient behaviour.

As increasing gate resistance slows down, switching speed EMI is reduced [27], and gate oscillations will be damped. However, increased gate resistance also exaggerates the spread in component tolerances leading to greater discrepancies in turn-on/off times. To explore the effects of increased gate resistance, current in individual devices in one submodule with four parallel-connected MOSFETs at 3 kHz switching frequency and 16 A load current, was measured. Non-symmetrical layouts lead to dynamic current imbalance, resulting in unbalanced switching losses [45], however with such low switching losses this effect is of no concern.

The dominant cause of static current unbalance is R_{on} mismatch. Experimental results in Fig. 7 show good static current balance.

Different individual device threshold voltages and trans-conductances lead to varying switching rates as seen in Fig. 7 where MOSFET4 turns on first. The Miller effect then slows down the rise in V_{GS} in the other three devices. The large current overshoot of MOSFET4 is caused by larger reverse recovery of its body diode resulting from its rapid turn-on transition. This dynamic current unbalance and the parasitic oscillations are exacerbated by the combined effects of the inductances, the gate and drain resistances, the gate–source capacitance and the drain–source capacitance [45, 46]. Considering so many factors affecting the switching performance, it is practically impossible to match the MOSFET switching transients [45].

However, Fig. 7 shows that the current overshoot is safe for all devices even at a gate resistance of 1 Ω , while with 100 Ω the current overshoot with four devices parallel connected is smaller than that for a single device switching with small gate resistance. As increased gate resistance slows down switching, oscillation and di/dt are attenuated significantly, reducing EMI. Fig. 7 clearly demonstrates that the MMC topology with increased gate resistance has significantly reduced device stress, while reduced ringing and slower transients will dramatically improve EMI, compared with a two-level converter.

6 Conclusions

The complex factors which must be considered when determining an optimal converter design for LVDC distribution networks have been thoroughly investigated. Power loss including semiconductor conduction, switching, capacitor and inductor losses was calculated for three different competing converter topologies. MMC topologies offer 200 W lower loss than the SiC two-level converter, while offering the possibility of fault tolerance with minimal impact on loss. Slowed switching with no loss penalty in MMC converters also offers improved reliability as switching waveforms presented here show reduced device stress, while EMI will also be significantly reduced. With by far the smallest heatsink volume Si MOSFET MMC offers a surprisingly competitively compact solution despite the requirement for a larger number of cell capacitors. GaN appears to offer highest efficiency by a small margin, but it remains to be seen how the high-speed, sensitive GaN gate drivers perform in terms of reliability, while reliability of the

GaN power devices appears to be lower than that of the Si MOSFET. However, since GaN is a new technology this reliability gap may close in time. In addition, counter-intuitively, the very small packaged GaN HEMT requires double the heatsink volume compared with Si MOSFET. The main advantage offered by the SiC two-level converter is simplicity, but the reliability history of SiC devices offsets this advantage, and with lower SiC two-level efficiency, the MMC topologies are more attractive. At this time, Si MOSFET MMC offers the lowest cost converter for this application, although the authors note that relative costs are likely to be subject to much change.

Therefore, for low-voltage, single-phase converters at 10 kW, Si MOSFET MMC offers the highest performance converter, with lowest cost, and small size.

Parallel connection of devices offers lower MMC loss and further reduction in devices stress, bringing reliability improvement, hence has been analysed during this research. Power loss calculations indicate that four devices in parallel is optimal for the MMC topologies, while parallel-connection was unhelpful for the SiC two-level converter due to the dominance of output capacitance related switching loss. Power loss was found to be the dominating factor dictating optimum extent of parallel connection. Experimental results for four devices in parallel showed good static current sharing, and with slowed switching demonstrated lower device stress and order of magnitude slower and smaller transients to generate EMI. Further work is required to fully quantify EMI reduction.

Calculated loss was successfully validated through experimental measurement for a single MMC module, and for a SiC half-bridge converter.

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8 References

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