Transient Stability Analysis in Multi-Terminal VSC-HVDC Grids

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***Abstract*—A novel approach to transient stability analysis in multi-terminal high voltage direct current (MTDC) grids is presented in this paper. A symmetrical three-phase fault in an ac grid connected to a rectifier terminal of the MTDC grid causes the power injected into the dc grid to decrease, which in turn leads to a lower dc voltage in the MTDC grid. If dc voltage drops below a critical voltage limit before the ac fault is cleared, then the dc grid becomes unstable and its operation is disrupted. An analytical approach is proposed in this paper to calculate the critical clearing time of a fault in an ac grid behind a rectifier terminal beyond which dc voltage collapse occurs. A five-terminal MTDC grid modeled in EMTDC/PSCAD is used to validate the results obtained with the analytical method.**

***Index Terms*--Critical clearing time, DC grid, Power System faults, MTDC, Transient stability**

I. INTRODUCTION

More and more Voltage Source Converter based High Voltage Direct Current (VSC-HVDC) transmissions links are coming up in the North Sea both for connection of offshore wind farm to onshore grids [1, 2] and for subsea interconnection of asynchronous power systems [3-5]. These point-to-point HVDC links will eventually be part of a larger DC grid with multiple connection points.

Considerable research has been conducted on modeling [6, 7], control [8-10] and steady-state operation [11, 12] of Multi-Terminal High Voltage DC (MTDC) grids. Transient stability studies of MTDC grids have focused on investigating converter control strategies that enhance the dynamic performance of the dc grid during an ac fault. Different control strategies for MTDC converters are presented in [13, 14], and it was shown that using a particle swarm optimization (PSO) method for controller tuning [13] and an adaptive current control limiter [14] improve the overall MTDC grid stability. Reference [15] explores a control method that limits the influence of unbalanced ac faults on the MTDC grid by eliminating double frequency oscillations in the active power flow.

In an MTDC grid with connection to offshore wind farms, a fault in onshore ac grid causes reduction in power transfer capacity of the MTDC converter terminal due to the low ac voltage. This leads to active power imbalance in the dc grid and increases the dc grid voltage. Control strategies proposed to limit dc over-voltage include reduction of wind farm power production [16-18] or the physical implementation of a chopper to dissipate the excess active power in the dc grid [19].

In multi-terminal or meshed dc networks, there will likely be converters and control systems supplied by different vendors and with slightly different design. To address this aspect, transmission system operators need to specify requirements for interoperability. One such requirement would concern the coordination of converter controls to ensure stable operation and protection against faults both on the ac and dc side. This paper presents a method for assessing transient stability in dc grids. A fault in an ac grid connected to a rectifier terminal of an MTDC causes reduction in power transfer capacity of the converter and therefore, reduction in power flow into the dc grid. During the transient disturbance period, the power demanded by the inverter terminals is met by the limited power transferred into the dc grid by the rectifiers and by the energy discharged from the capacitors in the dc grid. The discharge of the capacitors leads to reduction of dc grid voltage. If the ac fault is not cleared before dc voltage drops below a critical voltage limit, then the dc grid voltage will not be able to recover. This will lead to dc grid instability and subsequently to the interruption of the dc grid operation. It is of interest to know how fast the converter controls must react to avoid a collapse of the dc grid. Previous transient stability studies have focused on the transient performance of converter controllers and their parameter settings. Furthermore, only simulations were used to study dc grid stability issues. In contrast, this work proposes a novel analytical method for calculating duration of an ac fault beyond which dc voltage instability occurs. A conservative approach is taken and it is assumed that when the transient disturbance occurs, all converters in a dc grid are operating in constant power control mode apart

from one converter which is operating in dc droop control mode. In reality, converter controllers will be either designed with voltage droop or there will be an emergency mode of operation acting when dc voltage is outside a certain range. In this respect, the use of constant power control in the analysis represents the worst-case scenario where dc voltage drops rapidly because no converter terminal participates in dc voltage regulation and as such, the proposed method serves as a tool to assess how fast converter controllers need to react to a disturbance. An analytical method is proposed to calculate the critical dc voltage and critical clearing time of the fault in an ac grid behind a rectifier terminal beyond which dc voltage collapse occurs. A five-terminal MTDC grid modeled in EMTDC/PSCAD is used to validate the results obtained with the analytical method.

II. VSC Operation Range

This section discusses the safe operation range of a VSC converter in an MTDC network. Qualitative introduction is given based on inverter and rectifier mode of operation, and dc voltage and power flow control. Positive power flow is defined as power flow from ac grid into dc grid.

The shaded area in Fig. 1 defines the normal operating region of a VSC-HVDC converter where all the operating limits are respected. The operation region is constrained by maximum power capacity, maximum dc voltage level, maximum dc current and minimum dc voltage level. The first three constraints are due to thermal and insulations limits, and are crucial for protection of the converter and dc cables from damage under high voltage and/or current levels [10, 20]. The fourth constraint (i.e. minimum dc voltage level) is inherent to the working principle of VSC and is related to modulation index, converter topology and control implementation [10, 21]. In square wave modulation, the maximum possible overmodulation puts the limit on the minimum attainable dc voltage to $1.28V_{LL}$ where V_{LL} is the rms line-to-line voltage at the point-of-common-coupling.

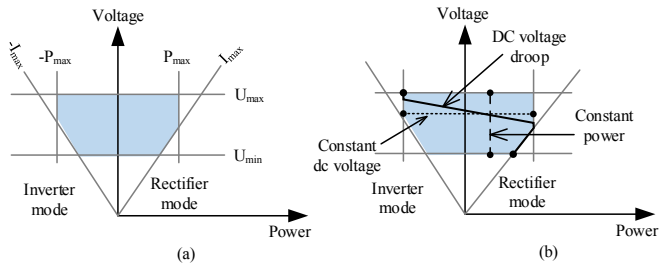

Fig. 1. Power vs. voltage capability diagram of a VSC-HVDC converter

The various dc voltage and power control strategies of MTDC converter terminals always lie within the boundaries of the normal operation region. Power vs. voltage characteristic lines for constant power control, dc voltage control and dc voltage droop control are shown in Fig. 1(b). Changing dc voltage and/or power references for the controllers moves the characteristic lines up or down (in cases of constant dc voltage and dc voltage droop control) or right or left (in case of constant power control). If for some reason, the operating point goes out of the shaded area and the controller is not able to bring it back to the normal operating region, a separate higher-level protection system may be activated to prevent damage due to overvoltage and/or overcurrent. The details of such protection system will not be discussed here. For simplicity, it is assumed that the VSC will trip immediately when the converter's operation goes outside the designated normal operating region.

III. Large Disturbance Stability in MTDC Grid

Transient stability in ac grids refers to the ability of a power system to maintain synchronism when subjected to severe disturbances like a fault on transmission lines, loss of generation or loss of a large load [22]. Similarly, in dc grids, transient stability can be defined as the ability of the dc grid to maintain dc voltage level when the system is subjected to large-scale disturbances such as converter outage, dc cable outage, dc faults and faults in the ac system connected to the MTDC [7].

Large-disturbance stability in multi-terminal dc grids can be understood by looking at the interaction between all rectifying converter units on one side and all inverting converter units on the other side. For illustration purposes, let us assume that the circuit in Fig. 2 represents an MTDC grid with aggregated rectifiers and inverters at each end. P_S refers to the aggregate power injected into the dc grid by the rectifiers and hence the terminal can be considered as a source converter. Likewise, P_L refers to the aggregate power withdrawn from the dc grid by the inverters and hence this terminal can be considered as a load converter. In order to simplify the analytical analysis, the dc grid line resistances and inductive elements are neglected. This simplification allows representation of all the dc capacitors at converter stations and the dc cable capacitances by a single shunt-connected capacitor (C_{agg}) between the two terminals: where C_{agg} is the total sum of all dc-bus and dc cable capacitances.

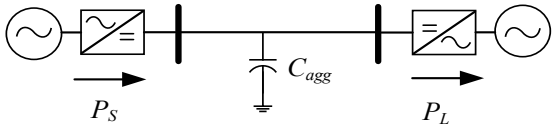

Fig. 2. Two-terminal equivalent circuit of an MTDC grid with aggregated rectifiers and inverters

The power vs. voltage characteristics of the aggregated rectifiers and inverters will be the sum of the power vs. voltage characteristics of the individual converters. If we assume that the rectifying converters have predominantly dc voltage droop characteristics and that of the inverting converters have predominantly constant power characteristics, then the power voltage characteristic curves of the source and load converters will resemble the curves shown in Fig. 3. The sum of dc voltage droop characteristic lines with different droop constants forms a non-linear curve consisting of different slopes. The P_S curves in Fig. 3 represent an approximation of combined characteristics lines of large number of dc voltage droop controlled rectifiers. Note that the characteristic curve for the load converter is laterally inverted since the power axis for this terminal is opposite to that of the source converter.

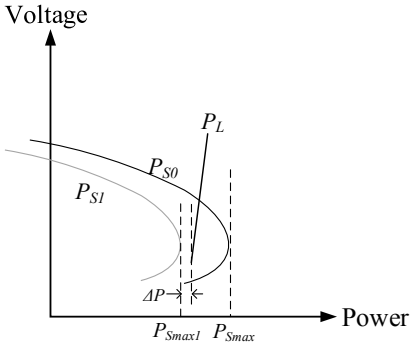

Fig. 3. Power vs. Voltage characteristics curve of aggregated rectifying and inverting converter terminals

The intersection between the aggregate power flow through the rectifiers and the aggregate power flow through the inverters approximately gives the total amount of power exchanged between ac grids via the MTDC grid. This is shown in Fig. 3 by the intersection of the characteristics curves of the aggregated rectifiers (P_{S0}) and the aggregated inverters (P_L). The lower intersection is unstable for small disturbances and only the upper intersection is a valid operating point. In steady state operation, P_L will always be lower than the maximum deliverable power of the aggregate rectifiers (P_{Smax}) as the power flow schedules always take into consideration the available loading capacity of the converters. However, transient disturbances such as sudden outage of a rectifier terminal or fault occurrence on the ac side of a rectifier terminal reduce the power transfer capacity of the aggregated rectifiers. Meaning, P_{S0} characteristic curve shifts to the left and P_{S1} becomes the new transient characteristic curve. When the transient maximum deliverable power of the aggregated rectifiers (P_{Smax1}) is lower than the power withdrawn by the aggregated inverters (P_L), then the difference ($\Delta P = P_{Smax1} - P_L$) will be supplied from the stored energy of the aggregated capacitor (C_{agg}). This stored capacitive energy is, however, very small and hence will last only very short duration without discharging the capacitor excessively. If the capacitors in the dc grid are discharged below a critical dc voltage level, the rectifiers' power transfer capabilities decrease further leading to dc voltage collapse.

If the cause of the disturbance is a fault within the dc grid or within the converter itself, then the problem will most likely persist resulting in dc voltage collapse followed by permanent disruption of power flow in the dc grid. However, ac faults are often temporary and power flow is usually restored after the clearance of the fault. In case of an ac fault behind a rectifier, if it is cleared before a critical dc voltage is reached, then the dc voltage will subsequently recover and stable power flow will resume. In addition to critical dc voltage level and the fault clearing time, dc voltage recovery also depends on whether or not there is enough deliverable power right after fault clearance that can meet the power demanded by the inverters and the power needed to recharge the capacitors.

This study focuses on cases where power injection into the dc grid is reduced because of an ac grid fault and consequently dc grid capacitive energy depletion occurs; leading to a dc voltage collapse. Converter trips due to low voltage limit or synchronization problems, in cases of unbalanced ac faults, are not considered.

IV. DC VOLTAGE STABILITY CRITERION

The two-terminal equivalent of an MTDC grid presented in Fig. 2 will be used to explain the dc voltage stability criterion. Fig. 4 shows stable power flow and dc voltage for an ac grid fault behind a rectifier unit. Δt is the fault clearing time and ΔP in Fig. 4(a) is the power supply gap in the dc grid during the transient disturbance. Thus, A_1 represents the energy deficit due to the reduced power injection caused by the ac fault. Since P_L remains constant during the fault, the energy deficit is covered by the energy discharged from the aggregated capacitor. A_2 represents the amount of energy needed to recharge the aggregated capacitor with the same amount of energy as it has lost during the fault. In order to maintain dc system stability after fault clearance, the inequality $A_2 \geq A_1$ must hold. The dc voltage stability phenomenon of dc grids has marked similarities with that of first-swing stability of synchronous generators in ac grids. However, A_2 in Fig. 4(a) is not bounded by a function of time unlike the same area in ac systems, which follows a sine curve. Due to this, the equal-area criterion in a dc grid does not specify the critical ac fault clearing time beyond which dc voltage collapse will be inevitable. Instead, the criterion indicates that if the dc voltage recovers after ac fault clearance, then the aggregated capacitor will be recharged with the same amount of energy as it lost during fault duration.

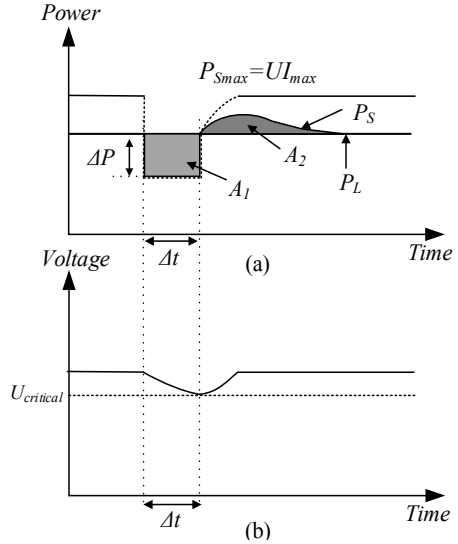

Fig. 4. Illustration of stable case of ac fault impact on dc power flow

The maximum deliverable power by a converter (P_{max}) is the product of dc bus voltage and maximum dc current of the converter (I_{max}). I_{max} is a known and fixed value for a converter, which means P_{max} is dependent on dc voltage and reduces with reduction in dc-bus voltage. After the fault is cleared, the maximum deliverable power by the aggregated rectifiers should be sufficient to meet the power demanded by the aggregated inverters (P_L). Furthermore, additional power flow is needed to recharge the capacitors and thereby to allow the dc voltage to return to the pre-disturbance level. If post disturbance P_{Smax} is higher than P_L, then the dc grid voltage will recover from the fault. Hence, the dc voltage level at which the post disturbance P_{Smax} equals P_L defines the *critical dc voltage level* ($U_{critical}$). The time it takes to reach $U_{critical}$ defines the

critical clearing time ($\Delta t_{critical}$). The ac fault behind the rectifier terminal needs to be cleared before $\Delta t_{critical}$ for dc grid voltage to recover and for dc power flow to continue uninterrupted.

V. Computation of Critical Clearing Time and Critical Voltage

The energy discharged from the capacitors in the dc grid during the fault period can be computed as:

$$\Delta P \Delta t = \frac{1}{2} C_{agg} \left(U_{initial}^2 - U_{final}^2 \right) \tag{1}$$

where $U_{initial}$ is the pre-fault dc voltage level and U_{final} is the dc voltage level when the ac fault is cleared. In order to achieve dc grid stability after fault clearance, the final voltage (U_{final}) should be greater than or equal to the critical dc voltage ($U_{critical}$) and the energy discharged from the capacitors should be less than the maximum amount of capacitive energy (E_{max}) that can be utilized for short-term power balancing in the dc grid. E_{max} is mathematically defined as:

$$U_{critical} \le U_{final} \tag{2}$$

$$\int_{t=0}^{\Delta t} \Delta P dt \le E_{\max} \tag{3}$$

where $E_{\max} = \frac{1}{2} C_{agg} \left(U_{initial}^2 - U_{critical}^2 \right)$

Furthermore, the rectifiers' available maximum power at critical dc voltage ($U_{critical}$) level should at least be equal to the power demanded by the inverters (P_L).

$$P_L \le P_{\max}(U_{critical}) \tag{4}$$

Equations (2) - (4) together define the dc voltage stability criterion.

The three-terminal dc grid shown in Fig. 5 is used as an example to explain how the critical dc voltage and critical clearing time are determined. Terminal-A operates in dc droop control mode and regulates the dc voltage and balances power, while terminals-B and C operate in constant power control mode injecting and withdrawing fixed amount of power, respectively. The initial steady state power flows at the three terminals are P_A^o , P_B^o and P_C^o .

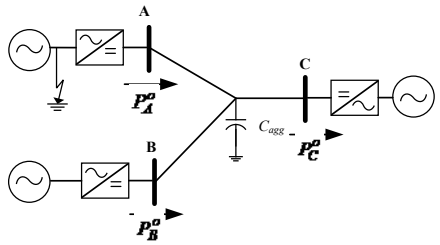

Fig. 5. A three terminal dc grid

Assume that a three phase to ground fault occurs behind terminal-A and as a result the power injected by this terminal into the dc grid is reduced from the pre-fault level of P_A^o to $P_A^{'}$. The power deficit (ΔP) of the dc grid during the ac fault becomes:

$$\Delta P = P_A^o - P_A^{'} \tag{5}$$

By substituting (5) into (3), the critical clearing time ($\Delta t_{critical}$) of an ac fault can be expressed in terms of $U_{critical}$ as:

$$\begin{aligned} &\int_{t=0}^{\Delta t} \Delta P dt \le \frac{1}{2} C_{agg} \left(U_{initial}^2 - U_{critical}^2 \right) \\ &\left(P_A^o - P_A^{'} \right) \Delta t_{critical} = \frac{1}{2} C_{agg} \left(U_{initial}^2 - U_{critical}^2 \right) \\ &\Delta t_{critical} = \frac{C_{agg} \left(U_{initial}^2 - U_{critical}^2 \right)}{2 \left(P_A^o - P_A^{'} \right)} \end{aligned} \tag{6}$$

Since terminals-B and C are operating in constant power control mode, the power flow at these terminals is unaffected by the low dc voltage during the fault and remains constant. Therefore, it is the maximum power transfer capacity of terminal-A that determines recovery of dc stability. In order to achieve stability, the power transfer capacity of terminal-A just after the fault clearance must be greater than or equal to the power transferred prior to the fault occurrence (P_A^o). This is expressed using (4) as:

$$\begin{aligned} P_A^o &\le P_{\mathrm{A\_max}}(U) \\ P_A^o &\le U I_{\mathrm{A\_max}} \end{aligned} \tag{7}$$

The critical dc voltage is the voltage level where the power transfer capability after the fault clearance ($P_{max}(U_{critical})$) equals P_A^o . This is mathematically given by:

$$U_{critical} = \frac{P_A^o}{I_{\max}} = \frac{P_A^o}{k I_N} \tag{8}$$

where the factor k describes dc overcurrent capability in terms of the rated dc current for terminal-A. I_{max} is a known fixed value for a converter and P_A^o has already been considered as a known value. Hence, the critical dc voltage ($U_{critical}$) can be computed right away from (8). Once $U_{critical}$ is known, the critical clearing time ($\Delta t_{critical}$) can computed from (6).

It should be noted $\Delta t_{critical}$ is related to $P_A^{'}$ and uncertainty in its values leads to variation in $\Delta t_{critical}$. The most conservative approach, which would give the shortest $\Delta t_{critical}$, is to assume $P_A^{'} = 0$.

VI. Simulation Studies

The proposed method of calculating critical dc voltage and critical clearing time was tested using the five-terminal MTDC system shown in Fig. 6. An average converter model with cascaded outer and inner vector control loops in dq-reference frame is used [8]. Converters connected to terminals 1 and 3 operate in rectifier mode while converters connected to terminals 2, 4 and 5 operate in inverter mode. All converters, except converter 1, operate in constant power operation mode, i.e.

injecting or withdrawing constant amount of power into and from the dc grid. Converter 1 operates in dc droop control mode controlling voltage and balancing power. Two cases were simulated, and their results were compared with the findings from the analytical method. In the first simulation case, only dc cable capacitances were used for the dc grid, while in the second simulation case, dc cable resistances and capacitance were used to model the dc grid. With these two cases, it is possible to analyze the effect of dc cable resistances in the results. The dc cable parameters used in the simulation analysis are shown in Fig. 6 and initial steady-state power flow for the different cases is presented in Table I.

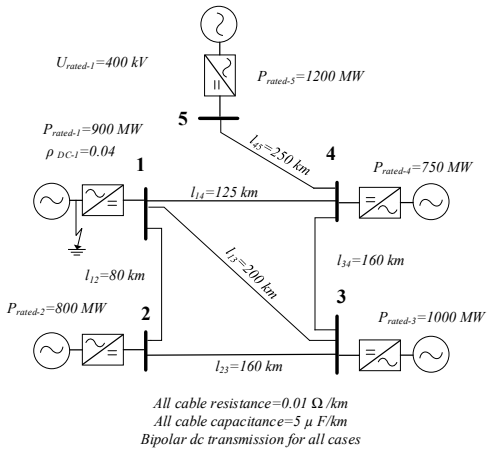

Fig. 6. Test MTDC system for the transient stability analysis

Table I. Initial steady state power flow for the test MTDC grid

	Terminal no.	1	2	3	4	5
Ratings	P_{rated} (MW)	900	800	1000	750	1200
	U_{rated} (kV)	400	400	400	400	400
Case 1	P^o (MW)	838	-400	675	-600	-513
	U^o (kV)	400	400	400	400	400
Case 2	P^o (MW)	838	-394.1	690	-600	-513
	U^o (kV)	400.96	399.99	401.2	397.1	390.53

As mentioned earlier, dc grid cable resistances and inductive elements are neglected to simplify the analytical analysis and allow representation of all the dc-bus capacitors and the dc line capacitors by a single shunt capacitor. Assuming a time constant of 5 ms for all converter dc-bus capacitances, the sum of all dc-bus capacitances in the system is calculated as:

$$\sum C_b = \frac{2\cdot\tau\cdot\sum_{i=1}^{5} P_{rated,i}}{U_{rated}^2} = \frac{2\cdot 5ms\cdot(900+800+1000+750+1200)MW}{(400kV)^2} = 290.625\mu F \quad (9)$$

Similarly, summing up all the dc cable capacitances:

$$\sum C_L = \frac{1}{2}\cdot 5\mu F/km\cdot(80+200+125+160+160+250)\text{km} = 2437.5\mu F \quad (10)$$

The total aggregated capacitance in the test MTDC grid is found by adding (9) and (10).

$$C_{agg} = \sum C_b + \sum C_L = 2728.125\mu F \quad (11)$$

Let us assume that Converter-1 in Fig. 6 is equipped with dc over-current controller which limits the dc current from exceeding 1.1 times the rated dc current. Therefore, I_{max} for Converter-1 becomes:

$$I_{\max} = kI_N = 1.1\cdot\frac{900MW}{400kV} = 2.475kA \quad (12)$$

A three-phase-to-ground fault in the ac grid behind Converter-1 results in reduction in power transferred into the dc grid from the pre-fault level 838MW to about 110MW. The critical dc voltage, based on (8), becomes:

$$U_{critical} = \frac{P_1^o}{I_{\max}} = \frac{838MW}{2.475kA} \approx 339kV \quad (13)$$

Then, the critical clearing time can be calculated using (6) as:

$$\Delta t_{critical} = \frac{C_{agg}\left(U_{initial}^2 - U_{critical}^2\right)}{2\left(P_A^o - P_A^{'}\right)} = \frac{2728.125\mu F\cdot\left(400^2 kV - 339^2 kV\right)}{2\cdot(838MW - 110MW)} = 84.5ms \quad (14)$$

In order to validate the analytical approach, the test MTDC grid was simulated in EMTDC/PSCAD. In the first simulation case, Case 1, only dc cable capacitances are used for dc grid modelling; similar to the analytical approach. In this ideal loss-less grid, the dc grid has a flat voltage profile of 400 kV at all terminals and the sum of all terminal power flows is zero. The initial steady-state power flows for Case 1 are presented in Table I. A three-phase short circuit fault was applied in the ac grid connected to converter-1 at 1.5 s into the simulation. A ground fault resistance of 0.12 Ω was selected to obtain 110 MW power flow at converter-1 during the fault. Fault clearing times both shorter than and close the calculated critical clearing time were simulated. The dynamic responses of the MTDC grid for three different fault clearing times are presented in Fig. 7 to Fig. 9.

First, the dc grid's transient response for a fault clearing time of 70 ms was studied. This fault clearing time is shorter than the analytically computed critical clearing time and therefore, it is expected that the MTDC grid will remain stable after the fault. Fig. 7 shows the response of the MTDC grid for an ac fault with 70ms duration.

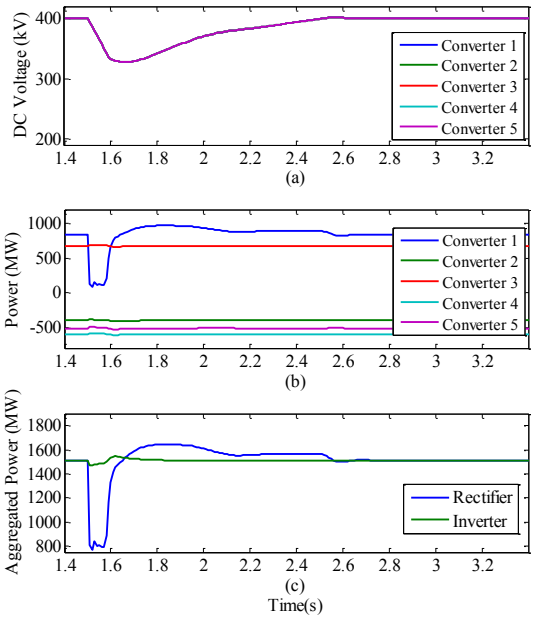

Fig. 7. MTDC response for ac fault duration of 70 ms: (a) DC voltage at each converter terminal, (b) DC power at each converter terminal, (c) Aggregated rectifier and converter power flows

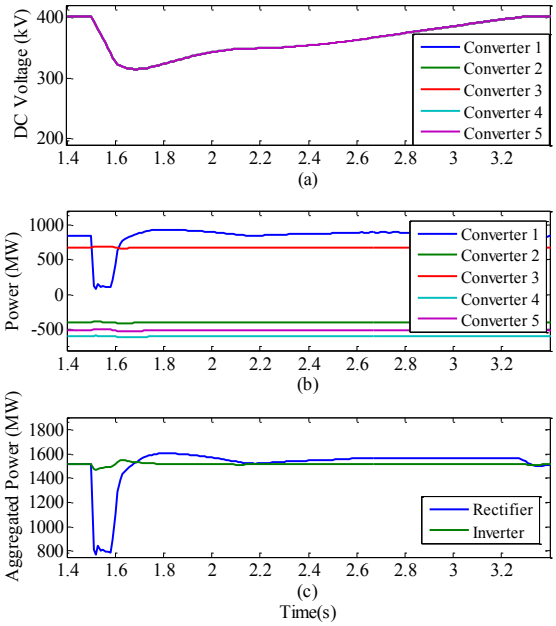

Fig. 8. MTDC response for ac fault duration of 85 ms: (a) DC voltage at each converter terminal, (b) DC power at each converter terminal, (c) Aggregated rectifier and converter power flows

It is clear from the plots in Fig. 7 that dc voltage recovers from the ac fault disturbance and dc grid operation continues uninterrupted. The top plot shows dc voltage measured at each converter terminal, while the middle plot shows power flow measured at the dc side of each terminal. The bottom plot shows the aggregated power flowing through the rectifiers (converter 1 & 3) and inverters (converters 2, 4 & 5) in the system. In steady state, the aggregated rectifier and aggregated inverter power flows are equal because it is a loss-less dc grid. However, during transient disturbance, there is a large difference between the two indicating dc grid power imbalances. Due to reduced power flow into the dc grid (see Fig. 7(b) and (c)) during the fault, the capacitors in the dc grid are discharged, leading to drop in dc voltage as shown in Fig. 7(a). When the fault is cleared, dc voltage starts to increase and eventually returns to the pre-fault level at around 2.6 s. From Fig. 7(b), it can be observed that only dc power flow at converter-1 is changed during the ac fault while the power flow at the other converters in the dc grid remains constant. This is due to the constant power control implemented in converters 2 to 5. The area enclosed by the aggregated rectifier and aggregated inverter power flow curves in Fig. 7(c) indicate the energy discharged from the capacitors during the fault and energy restored to the capacitors in the dc grid after the fault.

MTDC grid response for 85 ms ac fault duration is shown in Fig. 8. DC voltage recovers after the fault and the grid remains stable after the disturbance. However, the dc voltage recovery time is much longer compared to the recovery time for 70 ms fault duration shown in Fig. 7. The disturbance recovery time is also evident in Fig. 8(c), where area enclosed by aggregated rectifier and aggregated inverter power flow curves after the fault (area denoted by A_2 in Fig. 4) is narrow and long.

DC grid voltage collapses and dc grid operation is interrupted when the ac fault is cleared after 86 ms. Fig. 9 shows dc grid performance for ac fault duration of 86 ms.

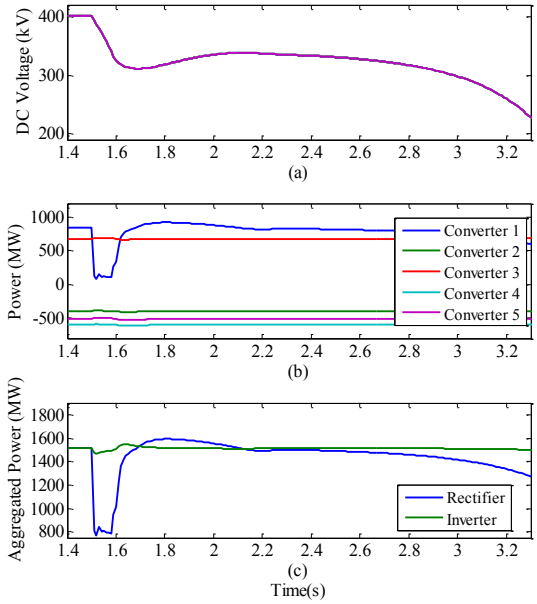

Fig. 9. MTDC response for ac fault duration of 86 ms: (a) DC voltage at each converter terminal, (b) DC power at each converter terminal, (c) Aggregated rectifier and converter power flows

From the simulation results, it can be concluded that the critical clearing time for the studied five terminal dc grid for the considered steady-state power flow and ac fault is 85ms. Therefore, a fault in the ac grid behind converter-1 that reduces dc grid power flow to 110 MW should be cleared at the latest after 85 ms. This fault clearing time is very close to the calculated critical fault clearing time of 84.5 ms. DC voltage

level right before the fault is cleared, is around 333 kV. However, dc voltage continues to drop (at a lower rate) until 1.69 s when the aggregated rectifier and inverter powers are equal. Therefore, the critical voltage level in the simulation, i.e. the voltage level at which post-disturbance aggregated rectifier and inverter powers are equal, is around 321 kV, while the calculated critical voltage level is 339 kV.

In the second simulation case, Case 2, dc cable capacitance and resistance parameters shown in Fig. 6 were used. This case is included to analyze the effect of dc cable resistances on the critical clearing time. The initial load flow for this case are presented in Table I. The power flow at converter-3 is changed (compared to Case 1) to account for the losses in the dc grid, and dc voltage is not the same at all terminals due to dc cable voltage drop. Similar to the previous case, a three-phase short circuit fault was applied in the ac grid behind converter-1 that resulted 110 MW power flow during the fault. It was found that the critical fault clearing is 80 ms, which is shorter than Case 1. However, the critical voltage level is on average around 320 kV, which is similar to Case 1.

The analysis presented above indicates converter terminals that are not affected by the disturbance are operating solely in constant power mode. Since the considered fault occurs behind the terminal that was regulating voltage, the dc grid voltage drops until the fault is cleared. In this respect, the above analysis represents the worst-case scenario (in respect to converter control), where critical fault clearing time is the shortest because dc voltage drop is not mitigated by controller actions of other converters in the system. As such, the proposed method can serve as a tool to assess how fast the converter controllers need to react on disturbances. However, in the real system, converters will participate in both power and voltage regulation. Therefore, the critical clearing time will be longer than the scenarios considered in this work.

VII. Conclusion

In this paper, a method for dc voltage transient stability analysis in MTDC has been presented. It is shown that if an ac grid fault resulting in reduction of the dc grid voltage is not cleared before the critical clearing time, the dc grid will become unstable and operation will be disrupted. The derivation of the analytical equation for the fault clearing time has been presented in the paper. With the help of a five-terminal dc grid model in PSCAD simulation software, the validity of the analytically estimated critical clearing time has been verified. The proposed method can be used as an aid to specify requirements for the design of the converter controls to manage faulty situations in the ac grid close to rectifier terminals.

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