Cascaded Commutation Circuit for a Hybrid DC Breaker with Dynamic Control on Fault Current and DC Breaker Voltage

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ABSTRACT

This paper proposed a cascaded commutation circuit based on current commutation approach for low-to-medium voltage DC fault current interruption, without snubber circuits, which slows the fault current *di/dt* prior to current-zero and the rate of rise of the transient recovery voltage *dv/dt* across the mechanical breaker contacts after current zero. The proposed dynamic control of the fault current *di/dt* and circuit breaker voltage dV_{VCB}/dt increase the fault current interruption capability at the first and second current-zeros. Detailed mathematical equations are presented to evaluate the operational waveform profile and the validity of the cascaded commutation principle is confirmed by simulation and experimental results at $600V_{dc}$, 110A and 330A.

Keywords: Hybrid DC Breaker, current commutation, current-zero, and fault interruption.

List of abbreviations

ABB	*Asea Brown Boveri Ltd*
AC	*Alternating current*
CBs	*Circuit breakers*
C	*Capacitance (F)*

C_C	*Commutation capacitance (F)*
$C_{C1,2,3}$	*Cascaded commutation capacitance (F)*
C_s	*Snubber capacitance (F)*
C_{bank}	*Capacitor bank (F)*
di/dt	*Decline rate of current before current-zero (kA/μs)*
dv/dt	*Rise rate of voltage across the opening contacts immediately after current-zero (kV/μs)*
dV_{VCB}/dt	*Rise rate of voltage across the VCB immediately after current-zero (kV/μs)*
DC	*Direct current*
HVDC	*High voltage direct current*
$i_{C1/2/3}$	*Cascaded counter current (A)*
i_T	*Current through the solid-state switches*
n	*Number of devices*
T_1-T_2-T_3-T_4-T_5-T_6	*Solid-state switches*
$\mathrm{T_{C1/2/3/4/5/6}}$	*Cascaded time intervals (μs)*
$V_{C_{C1}}$	*Voltage cross the commutation capacitor C_{C1}*
$V_{C_{C1,2}}$	*Voltage cross the series-connected commutation capacitor C_{C1} and C_{C2}*
$V_{C_{C1,2,3}}$	*Voltage cross the series-connected commutation capacitor C_{C1}, C_{C2} and C_{C3}.*

I. INTRODUCTION

The necessity of DC breaker topologies in low to medium voltage applications is paramount to the success of developing full DC systems either in localised grid infrastructure [1, 2] or commercial applications in avionics, automotive and telecommunications [3]. Fast interruption time, reliable and successful fault interruption are the main factors that contributes to the system rating of the downstream power electronics. Over de-rating on the power electronics to compromise on slow-switching DC breakers contributes to higher cost and lower efficiency [4]. Arc-flash hazard analysis in low and medium voltage DC systems has been extensively evaluated in [5, 6]. In particular to DC circuit breaker, arcing will occur when current-zero is not achieved during the breaker interruption process [7, 8].

(a) Mechanical circuit breaker techniques

DC fault current limitation through helical arc control and mechanical circuit breaker has been proposed in [9] and [10] respectively. Both studies utilise specific design on the mechanical circuit breaker to either control the arc formation [9] or use of Thomson coil [10] to limit and interrupt the fault current. However, the mechanical circuit breaker in [9] need to factor in the large internal blades structure to enhance arc and fault current control. Allowing arc formation can lead to subsequent structure failure and higher maintenance requirement. Although the response time of the mechanical breaker in [10] is lesser than 2ms, the full interruption time that is associated with the coil damping duration are larger than 10ms. This damping duration need to be considered in rapid fault current interruption. The mechanical circuit breaker technique in [11] demonstrated fast interruption time in micro-seconds range. The technique is based on generating a reverse current and an intense axial magnetic field by two helical flux compression generators. Although fast interruption time is achievable, the technique is limited by low probability of successful fault interruption due to single current-zero generation and reliability constraint by the requirement of significant magnetic field.

(b) Solid-state circuit breaker techniques

Alternate DC circuit breaker approaches that provide rapid fault current interruption has been reviewed in [12-14]. These approaches are based on solid-state circuit breakers which depend on the turning-off of the semiconductors to interrupt DC fault current. Fault current interruption time lesser than 1ms can be achieved and the system structures are normally simple with lesser components count. However, the main limiting factors that incurred with these approaches are the on-state power losses and the cooling requirements that are associated with the semiconductors. Although wide-band gap devices in [15, 16] has been proposed to reduce the

losses and cooling requirements, the semiconductors position on the DC line will need to sustain the DC input voltage and the induced inductive voltage during fault current interruption. High *di/dt* due to rapid fault current interruption will result in significant induced inductive voltage. The semiconductors will have to be series-connected to sustain these overvoltage and dynamic voltage sharing techniques [17] need to be integrated to prevent device failure.

(c) Hybrid circuit breaker techniques

The hybrid DC circuit breaker based on forced commutation principle has been extensively research in HVDC applications [18-21]. The main principle underlying these approaches is to introduce a current-zero to the mechanical circuit breaker before it attempts to interrupt the fault current, thereby reducing the possibility of arcing and decreases the fault current interruption time. Current-zero is achieved either through the series-connected semiconductor device [18] with the mechanical circuit breaker or the forced current commutation from the shunt-connected circuitry across the mechanical circuit breaker [19, 20]. The two stage operation demonstrated in [21] commutated the fault current into the capacitor in a controlled approach to achieve low voltage across the DC breaker during initial contact separation. Although successful fault interruption can be achieved with reduce voltage across the DC breaker as stated in [22], the semiconductors used in [21] need to be rated with respect to the Metal Oxide Varistor (MOV) clamping voltage. MOV is used in the final stage to limit the voltage across the DC breaker, which its clamping voltage can be twice of the DC input source. The fault current interruption time from hybrid DC circuit breaker is dependent on the mechanical circuit breaker opening under arc-less condition. These are generally longer than solid-state circuit breaker techniques and also consists of circuitry with more components count to achieve the current-zero condition. However, in DC applications where fault current interruption time is between the range of 2 to 5ms [23], hybrid DC circuit breaker techniques is preferred as the conduction loss is primarily dependent on the mechanical circuit breaker if forced current commutation circuitry is shunt across the circuit breaker. This is much lower than solid-state DC breaker and the physical disconnection of the current path is more reliable with mechanical circuit breaker. Also, the cooling requirement for the semiconductors are less as they are only operational during the fault condition.

The conditions associated with successful fault current interruption on DC circuit breaker has been evaluated in [22]. A lower fault current *di/dt* or dV_{VCB}/dt across the circuit breaker increase the successful interruption probability. This paper enhances the work carried out in [22] and proposed a cascaded forced current commutation circuitry that slows the fault current *di/dt* prior to current-zero and a low dV_{VCB}/dt voltage profile across the circuit breaker during the

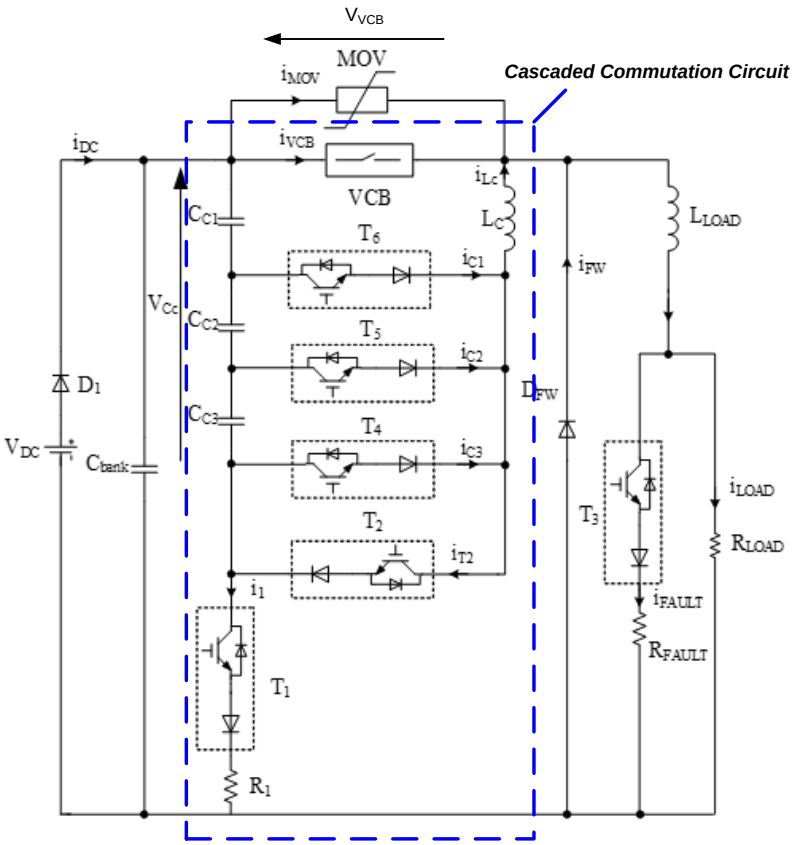
interruption process. The volume and cost of the proposed commutation circuit can be reduced with recent technological advances in power semiconductors devices [24, 25]. The availability of 6.5kV IGBTs [26] allows lesser cascaded voltage stages and this made the proposed hybrid DC circuit breaker well-suited in low to medium voltage level (1.2kV to 15kV) applications. Applications in high voltage level (>15kV) can still be established with increased cascaded voltage stages or utilizing next generation wide-band gap devices capable in excess of 10kV voltage rating [16, 25, 27, 28]. However, the cost comparisons on the proposed approach with others techniques and devices are not evaluated in this paper. The economic comparison on DC breaker topologies is presented in [29].

This paper focus and evaluate on the approach and technique that allows the control of the fault current di/dt and circuit breaker voltage dV_{VCB}/dt. The test-rigs involved in the evaluation are presented in [30].

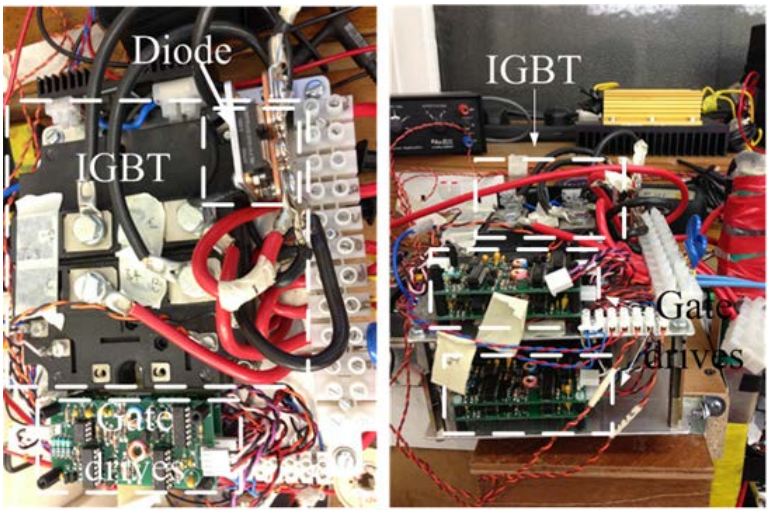
Section II in this paper defines the operating principles of the proposed commutation circuit with associated mathematical equations to confirm the waveform profiles. Section III presents the simulation and experimental results of successful current interruption at 110A and 330A.

II. Basic principles of the cascaded commutation circuit

Operation of the proposed cascaded commutation circuit in Fig. 1 involves three sequential processes, namely the preparation (or reset) of commutation circuit, the introduction of fault current, and initiation of the commutation circuit.



(a)



(b)

Fig. 1: *The cascaded commutation circuit of the hybrid breaker; VCB: vacuum circuit breaker and $T_{1,2,3,4,5,6}$: series diode and IGBT combination.*
(a) Cascaded commutation circuit diagram
(b) Pictorial view of the commutation circuit

The circuit consist of series-connected capacitors, such that $C_{C1} = C_{C2} = C_{C3}$ are in connection with solid-state switches *T4*-*T5*-*T6*. The proposed circuitry allow *n*+1 capacitors to be connected in series for higher DC voltage application and/or refined control of the dynamic *dV/dt* across the VCB. In this paper, three capacitors are series-connected for the circuit analysis and evaluation.

The three solid-state switches are controlled by sequential time intervals, overlapping for a short duration (1μs in this paper) to ensure commutation current continuity, as shown in Fig. 3(H). Under normal load conditions, only the VCB and T_1 are closed, transmitting power to load and to charge the commutation capacitors $C_{C1} - C_{C2} - C_{C3}$ with an initial voltage totalling V_{DC}, respectively while the other switches, *T2* to *T6*, are open. A DC fault is emulated by turning on *T3*, so that the energy stored in the capacitor bank C_{bank} is released through the load inductor L_{LOAD} into the fault resistor R_{FAULT}, to produce a high current through the VCB before the electrodes open. For commutation preparation, the commutation capacitors $C_{C1,2,3}$ are reversed charged by turning on *T2* after receiving the trip signal. Since $C_{C1} = C_{C2} = C_{C3}$, the voltage cross each capacitor is equal ($V_{C_{C1}} = V_{C_{C2}} = V_{C_{C3}}$). The fault clearance interruption procedure is shown in Fig. 2. For analysis convenience, the VCB arc voltage is ignored, being a low voltage.

(i) Time interval, $t_0 - t_{c0}$

At time t_1, the electrodes started to open introducing an arc voltage across the VCB. When a specific gap distance had been reached, at $t_2 = t_{c0}$ the solid-state switch *T4* is closed. Then, the resonant counter-current $i_{L_C} = i_{C3}$ produced by $L_C C_{C1,2,3}$ rises and forces the current $i_{VCB} = i_{FAULT}$ through the VCB to decrease. See loop $C_{C1,2,3} - VCB - L_C - T_4$.

(ii) Time interval, $t_{c0} - t_{c3}$

At t_{c1}, the counter-current $i_{L_C} = i_{C2}$ is switched into the loop $C_{C1,2} - VCB - L_C - T_5$ by turning on switch *T5*, then *T4* off; after obtaining energy from $L_C C_{C1,2}$ the current continues to rise until t_{c2}. Then the counter-current transfers into the next loop $C_{C1} - VCB - L_C - T_6$ as the solid-state switch *T6* is fired and *T5* is turned off, such that $i_{L_C} = i_{C1}$ is produced by $L_C C_{C1}$. When the counter-current reaches the fault current i_{FAULT} level (after a specifiable commutation time from t_{c0} to t_{c3}), the first VCB current-zero occurs at t_{c3} and i_{FAULT} is commutated into the loop $C_{bank} - C_{C1} - T_6 - L_C - L_{LOAD} - T_3 - R_{FAULT}$.

(iii) Time interval, t_{c3} - t_{c6}

Since only capacitor C_{C1} is operational, the voltage V_{VCB} across the VCB is forced to equal and track the residual capacitor voltage of $V_{C_{C1}}$ until voltage $V_{C_{C1}}$ approaches zero at t_{c4}. Then i_{FAULT} switches into the loop $C_{bank} - C_{C1,2} - T_5 - L_C - L_{LOAD} - T_3 - R_{FAULT}$ by turning on solid-state switch T_5, then is T_6 turned off. V_{VCB} tracks the residual voltage of $V_{C_{C1}}$ plus $V_{C_{C2}}$ until t_{c5} when the residual voltage $V_{C_{C1}} + V_{C_{C2}}$ approaches zero. Then the solid-state switch T_4 is fired and T_5 turned off, and i_{FAULT} enters the loop $C_{bank} - C_{C1,2,3} - T_4 - L_C - L_{LOAD} - T_3 - R_{FAULT}$. The VCB voltage starts to increase following the residual voltage $V_{C_{C1}} + V_{C_{C2}} + V_{C_{C3}}$. For a failed interruption at the first current-zero, i_{VCB} repeats the timing sequence to produce a second current-zero. A second commutation failure is deemed to specify interruption failure.

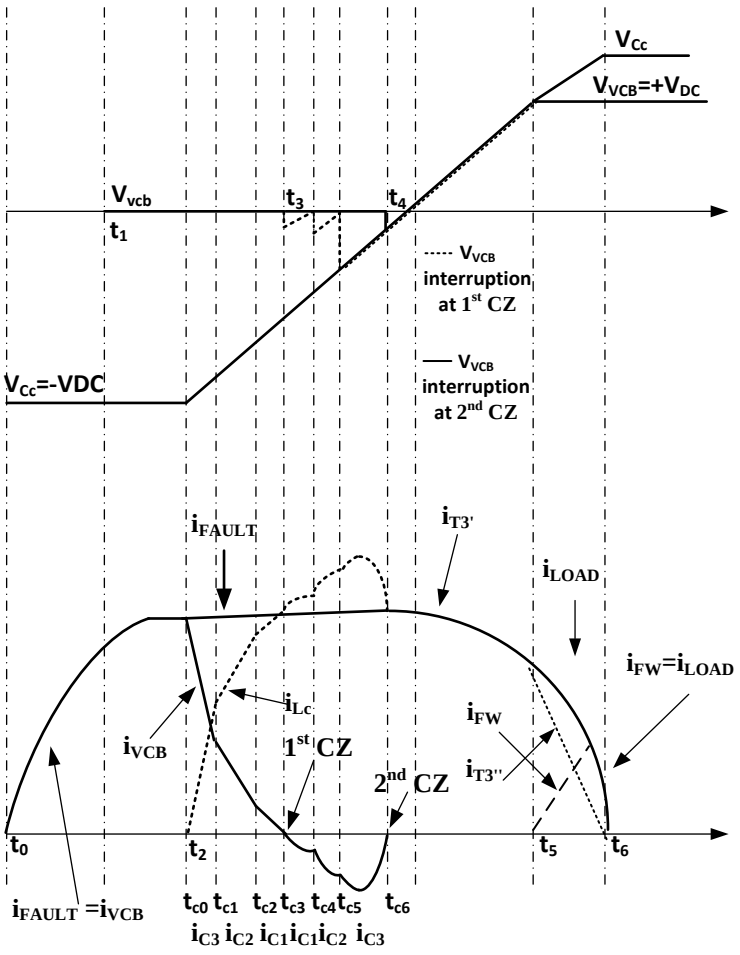
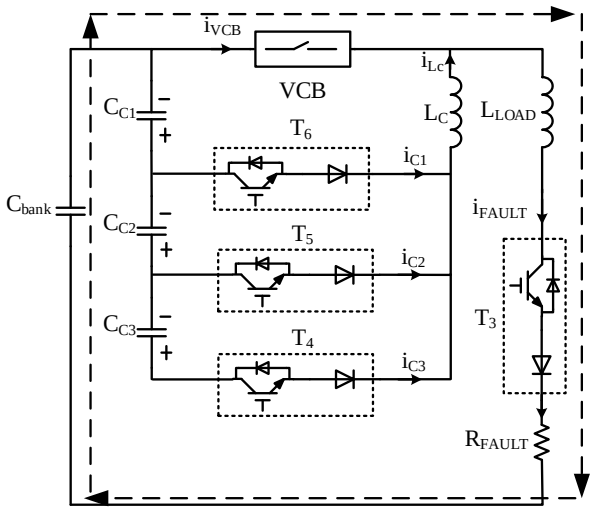


Fig. 2: *Operational sequence waveforms for the cascaded circuit; CZ current-zero crossing in the VCB.*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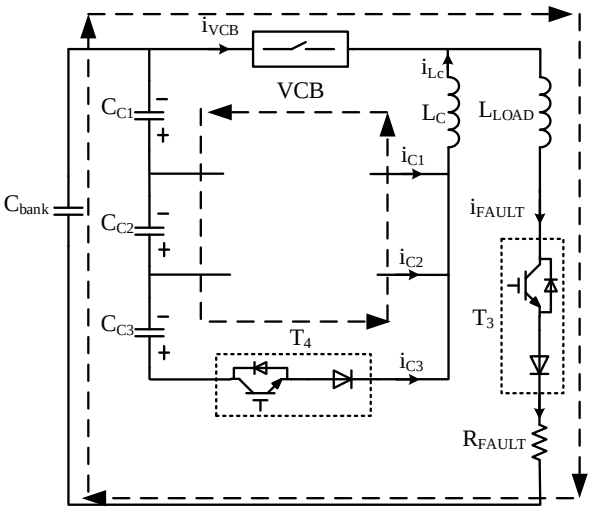
VCB
iLc
LC
LLOAD
CC1
T6
iC1
Cbank
CC2
T5
iC2
iFAULT
CC3
T4
iC3
T3
RFAULT

(A)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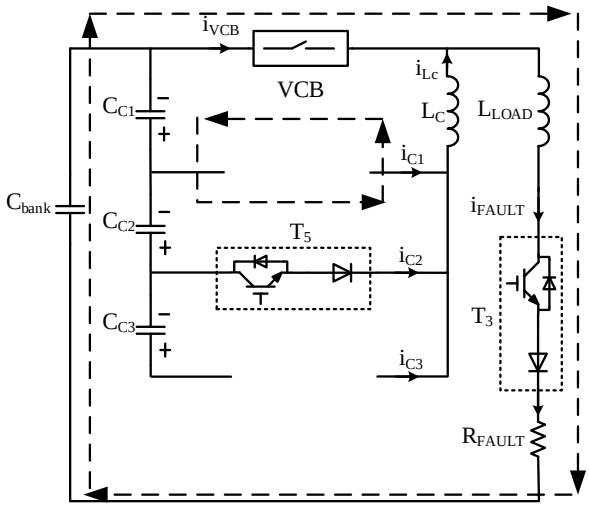
RFAULT

(B)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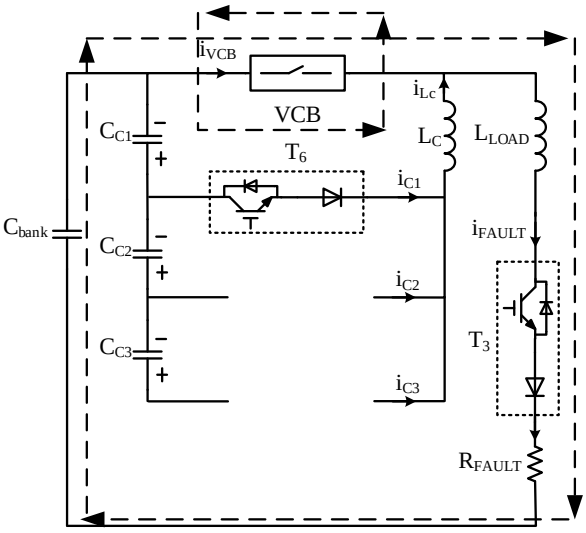
RFAULT

(C)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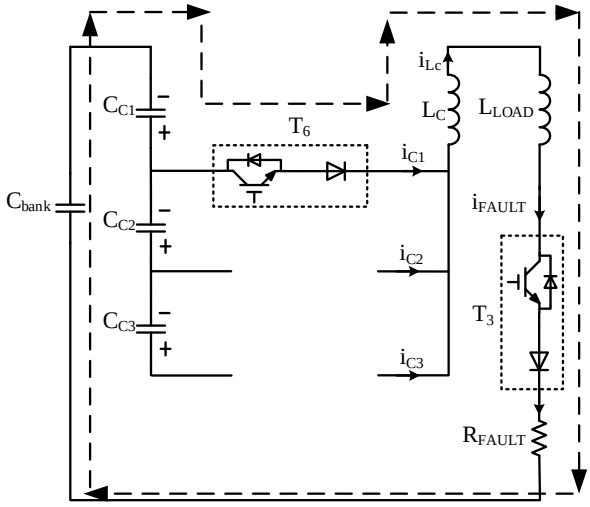
(D)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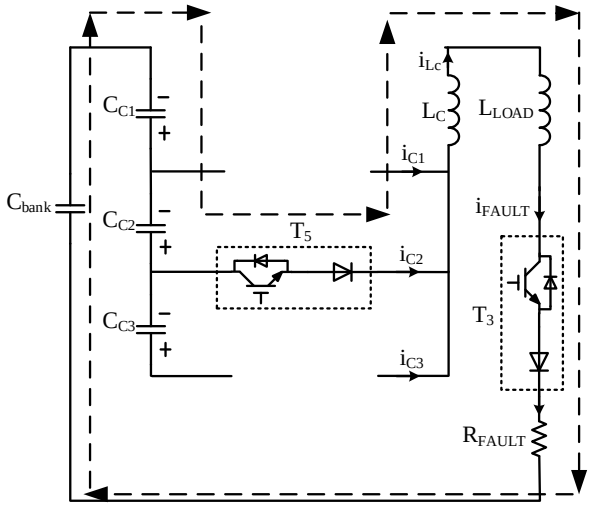
iC2
CC3
iC3
T3
RFAULT

(E)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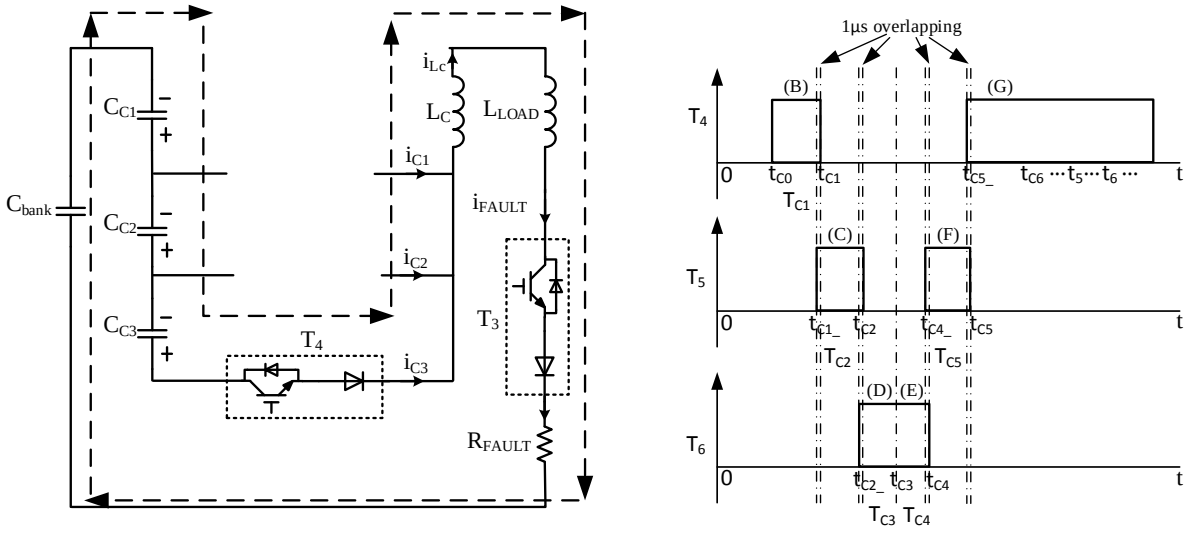
iC3
T3
RFAULT

(F)



(G) (H)

Fig. 3: *Interruption sequence of the cascaded commutation circuit.*

The mathematical description of the interruption sequences during commutation is based on the timing diagram in Fig. 3. For simplified analysis, the inductors are assumed linear, the voltage drops across all solid-state switches and the VCB state are zero during the on-state; due to large C_{bank}, its voltage is considered constant, charged to V_{DC}; the commutation capacitors have no circuit leakage paths when inactive; and finally, the VCB fault current i_{FAULT} is unchanged during the commutation process, since the commutation time is shorter than the fault-path time constant. A detailed solution is obtained by solving the differential equations corresponding to each interval; while the end state of one interval is the initial state of the following interval, thereby maintaining continuity between successive intervals.

(A) Prior to commutation circuit operation

Fig. 3(A) depicts the cascaded circuit when the VCB fault current has reached its expected value. The VCB electrodes have separated a specific distance. The commutation capacitor $C_{C1,2,3}$ has been reversed charging, so that the commutation circuit is ready to produce a counter-current through the VCB. In Fig. 3(H), to maintain cascaded commutation circuit continuity, solid-state switches T_4-T_5-T_6 are controlled through a sequence of six intervals with 1μs overlapping (intervals T_{C1}-T_{C2}-T_{C3}-T_{C4}-T_{C5}-T_{C6}). Intervals T_{C3} and T_{C4} use the same signal. Overlap ensures continuity, that is $t_{c1} = t_{c1\_}$, $t_{c2} = t_{c2\_}$, $t_{c4} = t_{c4\_}$, $t_{c5} = t_{c5\_}$.

(B) Time interval, $t_{c0} \le t \le t_{c1}$

At time $t_2 = t_{c0}$, switch T_4 is turned on to introduce counter-current i_{L_C} through the VCB, forcing the current i_{VCB} through the VCB to decrease. The relationships between i_{FAULT}, i_{VCB} and i_C is:

$$i_{FAULT} = i_{VCB} + i_{L_C} \quad \text{(A)} \tag{1}$$

where $i_{L_C} = i_{C3}$ and $C_{C1} = C_{C2} = C_{C2}$, thus the current i_{C3} through circuit loop $C_{C1,2,3} - VCB - L_C - T_4$ is defined by:

$$\frac{1}{C_{C1,2,3}} \int i_{C3} dt + L_C \frac{di_{C3}}{dt} = 0 \tag{2}$$

with the initial conditions

$$i_{C3}(t_{c0}) = 0 \text{ (A) and } V_{C_C}(t_{c0}) = -V_{DC} \quad \text{(V)}$$

which yield:

$$i_{C3}(t) = \frac{V_{DC}}{Z} \sin \omega_0 t \quad \text{(A)} \tag{3}$$

and

$$V_{C_{C1,2,3}}(t) = -V_{DC} \cos \omega_0 t \text{ (V)} \tag{4}$$

$$0 \le \omega_0 t \le \pi \quad \text{(rad)}$$

where $\omega_0 = 1/\sqrt{L_C C_{C1,2,3}}$ (rad/s)

$$Z = \sqrt{L_C / C_{C1,2,3}} \quad (\Omega)$$

$$C_{C1,2,3} = \tfrac{1}{3} C_{C1} = \tfrac{1}{3} C_{C2} = \tfrac{1}{3} C_{C3} \quad \text{(F)}$$

At the end of this interval, the voltage across the commutation capacitors $C_{C1,2,3}$ is $V_{C_{C1,2,3}} = V_{C_{C1,2,3}}(t_{c1})$, that is $V_{C_{C1}} = V_{C_{C2}} = V_{C_{C3}} = \tfrac{1}{3} V_{C_{C1,2,3}}(t_{c1})$; and the commutation current is $i_C = i_{C3}(t_{c1})$; thus the equation describing this interval T_{C1} is:

$$T_{C1} = t_{c1} - t_{c0} = \frac{-\sin^{-1} \frac{i_{C3}(t_{c1}) Z}{V_{DC}}}{\omega_0} \tag{5}$$

(C) Time interval, $t_{c1} \le t \le t_{c2}$

T_5 is turned on and T_4 off at t_{c1}, then the commutation current i_{L_C} diverts into the loop $C_{C1,2} - VCB - L_C - T_5$; thus equalling current i_{C2} which can be expressed by the differential equation:

$$\frac{1}{C_{C1,2}} \int i_{C2} dt + L_C \frac{di_{C2}}{dt} = 0 \tag{6}$$

with initial conditions

$$i_{C2}(t_{c1}) = i_{C3}(t_{c1}) \text{ (A) and } V_{C_{C1,2}}(t_{c1}) = \tfrac{2}{3} V_{C_{C1,2,3}}(t_{c1}) \quad \text{(V)}$$

which yield:

$$i_{C2}(t) = i_{C3}(t_{c1}) \cos \omega_{0'} t - \frac{2V_{C_{C1,2,3}}(t_{c1})}{3Z'} \sin \omega_{0'} t \text{ (A)} \quad (7)$$

and $$V_{C_{C1,2,}}(t) = Z' i_{C3}(t_{c1}) \sin \omega_{0'} t + \tfrac{2}{3} V_{C_{C1,2,3}}(t_{c1}) \cos \omega_0 t \text{ (V)} \quad (8)$$

$$0 \le \omega_0 t \le \pi \quad \text{(rad)}$$

where $\omega_{0'} = 1/\sqrt{L_C C_{C1,2}}$ (rad/s)

$$Z' = \sqrt{L_C / C_{C1,2}} \quad (\Omega)$$

$$C_{C1,2} = \tfrac{1}{2} C_{C1} = \tfrac{1}{2} C_{C2} = \tfrac{1}{2} C_{C3} \quad \text{(F)}$$

At the end of this interval, the voltage across the commutation capacitor $C_{C1,2}$ is $V_{C_{C1,2}} = V_{C_{C1,2,}}(t_{c2})$, where $V_{C_{C1}} = V_{C_{C2}} = \tfrac{1}{2} V_{C_{C1,2}}(t_{c2})$, $V_{C_{C3}} = \tfrac{1}{3} V_{C_{C1,2,3}}(t_{c1})$; and the commutation current is $i_{L_C} = i_{C2}(t_{c2})$; thus the equation for the time of this interval T_{C2} is:

$$T_{C2} = t_{c2} - t_{c1} = \frac{-\sin^{-1} \frac{V_{C_{C1,2}}(t_{c1}) \times i_{C2}(t_{c2}) + L_C \times i_{C2}(t_{c1}) \times \omega_{0'} \times A}{(C_{C1,2} \times \left(V_{C_{C1,2}}(t_{c1})\right)^2 + L_C \times \left(i_{C2}(t_{c1})\right)^2) \times \omega_{0'}}}{\omega_{0'}} \quad (9)$$

where $A = \sqrt{\frac{C_{C1,2} \times (V_{C_{C1,2}}(t_{c1}))^2 + L_C \times (i_{C2}(t_{c1}))^2 - L_C \times (i_{C2}(t_{c2}))^2}{L_C}}$

(D) Time interval, $t_{c2} \le t \le t_{c3}$

Solid-state switch T_6 is fired and T_5 is turned off at time t_{c2}, then the commutation current i_{L_C} enters the loop $C_{C1} - VCB - L_C - T_6$. The resulting current i_{C1} is defined by:

$$\frac{1}{C_{C1}} \int i_{C1} dt + L_C \frac{di_{C1}}{dt} = 0 \quad (10)$$

with the initial conditions

$$i_{C1}(t_{c2}) = i_{C2}(t_{c2}) \text{ (A) and } V_{C_{C1}}(t_{c2}) = \frac{V_{C_{C1,2}}(t_{c2})}{2} \text{ (V)}$$

which yield:

$$i_{C1}(t) = i_{C2}(t_{c2}) \cos \omega_{0''} t - \frac{V_{C_{C1,2}}(t_{c2})}{2Z''} \sin \omega_{0''} t \text{ (A)} \quad (11)$$

and $$V_{C_{C1}}(t) = Z'' i_{C2}(t_{c2}) \sin \omega_{0''} t + \frac{V_{C_{C1,2}}(t_{c2})}{2} \cos \omega_{0''} t \quad \text{(V)} \quad (12)$$

$$0 \le \omega_0 t \le \pi \quad \text{(rad)}$$

where $\omega_{0''} = 1/\sqrt{L_C C_{C1}}$ (rad/s)

$$Z'' = \sqrt{L_C / C_{C1}} \quad (\Omega)$$

$$C_{C1} = C_{C2} = C_{C3} \quad \text{(F)}$$

When the commutation current i_{C1} rises to equal the fault current, in the commutation period t_{c0} to t_{c3}, there is sufficient time for vacuum recovery, having introduced a VCB current-zero. Since the period of each interval has been calculated, it is possible to achieve the first current-zero occurring at time t_{c3}. This means $i_{C1}(t_{c3})$=$i_{FAULT}(t_{c3})$ and the commutation capacitor C_{C1}voltage is $V_{C_{C1}} = V_{C_{C1}}(t_{c3})$, and the other capacitor voltages are $V_{C_{C2}} = ½V_{C_{C1,2}}(t_{c2})$ and $V_{C_{C3}} = ⅓V_{C_{C1,2,3}}(t_{c1})$. The period of this interval T_{C3} is:

$$T_{C3}=t_{c3} - t_{c2} = \frac{-\sin^{-1}\frac{V_{C_{C1}}(t_{c1})\times i_{FAULT}(t_{c3})+L_C\times i_{C1}(t_{c2})\times\omega_0''\times A'}{(C_{C1}\times\left(V_{C_{C1}}(t_{c2})\right)^2+L_C\times(i_{C1}(t_{c2}))^2)\times\omega_0''}}{\omega_{0}''} \qquad (13)$$

where $A' = \sqrt{\frac{C_{C1}\times(V_{C_{C1}}(t_{c1}))^2+L_C\times(i_{C1}(t_{c2}))^2-L_{c}\times(i_{FAULT}(t_{c3}))^2}{L_C}}$

In summary, the commutation current i_{L_C}, before current-zero, can be described by the piecewise function:

$$i_C = \begin{cases} i_{C3}(t) i_{C3}(t) = \frac{V_{DC}}{Z}\sin\omega_0 t & (t_{c0} \le t \le t_{c1}) \\ i_{C2}(t) = i_{C3}(t_{c1})\cos\omega_0' t - \frac{2V_{C_{C1,2,3}}(t_{c1})}{3Z'}\sin\omega_0' t & (t_{c1} \le t \le t_{c2}) \\ i_{C1}(t) = i_{C2}(t_{c2})\cos\omega_0'' t - \frac{V_{C_{C1,2}}(t_{c2})}{2Z''}\sin\omega_0'' t & (t_{c2} \le t \le t_{c3}) \end{cases} \qquad (14)$$

(E) Time interval,$t_{c3} \le t \le t_{c4}$

i_{FAULT} is commutated into the loop $C_{bank} - C_{C1} - T_6 - L_C - L_{LOAD} - T_3 - R_{FAULT}$; but is still equal to i_{C1} which can be expressed by the differential equation:

$$\frac{1}{C_{C1}}\int i_{C1}dt + L_C\frac{di_{C1}}{dt} + L_{LOAD}\frac{di_{C1}}{dt} + i_{C1}R_{FAULT} = V_{DC} \qquad (15)$$

where the voltage across C_{bank} can be considered a DC source due to large C_{bank}, with the initial conditions

$$i_{C1}(t_{c3})=i_{FAULT}(t_{c3})\text{(A) and } V_{C_{C1}} = V_{C_{C1}}(t_{c3}) \quad \text{(V)}$$

Practically $R_{FAULT} < 2\sqrt{\frac{L_{LOAD}}{C_{C1}}}$, which yields:

$$i_{C1}(t) = 2K_1' e^{-\delta_2 t}\cos(\omega_3' t - \theta') \quad \text{(A)} \qquad (16)$$

$$V_{C_{C1}}(t) = \frac{2K_1'}{C_{C1}\omega_4'}[\cos(\beta_2' - \theta') - e^{-\delta_2 t}\cos(\omega_3' t - \theta' + \beta_2')] + V_{C_{C1}}(t_{c3}) \quad \text{(V)} \qquad (17)$$

where $\delta_2 = \frac{R_{FAULT}}{2(L_{LOAD}+L_C)}$; $\omega_3'^2 = \frac{1}{(L_{LOAD}+L_C)C_{C1}} - \left(\frac{R_{FAULT}}{2(L_{LOAD}+L_C)}\right)^2$

$\omega_4' = \sqrt{{\delta_2}^2 + \omega_3'^2}$; $\beta_2' = \tan^{-1}\frac{\omega_3'}{\delta_2}$

$$K_{1\prime} = \sqrt{\left(\frac{i_{FAULT}(t_{c3})}{2}\right)^2 + \left(\frac{\frac{V_{DC} - V_{C_{C1}}(t_{c3})}{L_{LOAD} + L_C} - \delta_2 i_{FAULT}(t_{c3})}{2\omega_{3\prime}}\right)^2}$$

$$\theta' = \tan^{-1} \frac{\frac{V_{DC} - V_{C_{C1}}(t_{c3})}{L_{LOAD} + L_C} - \delta_2 i_{FAULT}(t_{c3})}{\omega_{3\prime} i_{FAULT}(t_{c3})}$$

Only capacitor C_{C1} is introduced into this circuit, the VCB voltage V_{VCB} is clamped to the residual voltage $V_{C_{C1}}$ until the end of this interval, t_{c4}.

(F) Time interval, $t_{c4} \leq t \leq t_{c5}$

After turning switch T_5 on and T_6 off, the fault current i_{FAULT} diverts into loop $C_{bank} - C_{C1,2} - T_5 - L_C - L_{LOAD} - T_3 - R_{FAULT}$. This means i_{C2} becomes the continuity energy, and is defined by:

$$\frac{1}{C_{C1,2}} \int i_{C2} dt + L_C \frac{di_{C2}}{dt} + L_{LOAD} \frac{di_{C2}}{dt} + i_{C2} R_{FAULT} = V_{DC} \qquad (18)$$

where the voltage across C_{bank} can be considered a constant DC source due to large C_{bank}, with the initial conditions

$$i_{C2}(t_{c4}) = i_{FAULT}(t_{c4}) \text{(A)}$$

$$V_{C_{C1,2}}(t_{c4}) = V_{C_{C1}}(t_{c4}) + V_{C_{C2}}(t_{c4}) \quad \text{(V)}$$

where $V_{C_{C2}}(t_{c4}) = ½ V_{C_{C1,2}}(t_{c2})$, which yields

$$V_{C_{C1,2}}(t_{c4}) = V_{C_{C1}}(t_{c4}) + ½ V_{C_{C1,2}}(t_{c2}) \text{ (V)}$$

for $R_{FAULT} < 2\sqrt{\frac{L_{LOAD}}{C_{C1,2}}}$, thus:

$$i_{C1,2}(t) = 2K_{1,,} e^{-\delta_2 t} \cos(\omega_{3,,} t - \theta'') \text{ (A)} \qquad (19)$$

$$V_{C_{C1,2}}(t) = \frac{2K_{1,,}}{C_{C1,2}\omega_{4,,}} [\cos(\beta_{2,,} - \theta'') - e^{-\delta_2 t} \cos(\omega_{3,,} t - \theta'' + \beta_{2,,})]$$

$$+ V_{C_{C1,2}}(t_{c4}) \text{ (V)} \qquad (20)$$

where $\delta_2 = \frac{R_{FAULT}}{2(L_{LOAD}+L_C)}$; $\omega_{3,,}^2 = \frac{1}{(L_{LOAD}+L_C)C_{C1,2}} - \left(\frac{R_{FAULT}}{2(L_{LOAD}+L_C)}\right)^2$

$\omega_{4,,} = \sqrt{{\delta_2}^2 + \omega_{3,,}^2}$; $\beta_{2,,} = \tan^{-1} \frac{\omega_{3,,}}{\delta_2}$

$$K_{1,,} = \sqrt{\left(\frac{i_{FAULT}(t_{c4})}{2}\right)^2 + \left(\frac{\frac{V_{DC} - V_{C_{C1,2}}(t_{c4})}{L_{LOAD} + L_C} - \delta_2 i_{FAULT}(t_{c4})}{2\omega_{3,,}}\right)^2}$$

$$\theta'' = \tan^{-1}\frac{\frac{V_{DC} - V_{C_{C1,2}}(t_{c4})}{L_{LOAD} + L_C} - \delta_2 i_{FAULT}(t_{c4})}{\omega_{3,,} i_{FAULT}(t_{c4})}$$

Now, V_{VCB} tracks the residual voltage $V_{C_{C1}}$ plus $V_{C_{C2}}$ until time t_{c5}.

(G) Time interval,$t_{c5} \le t \le t_{c6}$

In this interval, i_{FAULT} enters loop $C_{bank} - C_{C1,2,3} - T_4 - L_C - L_{LOAD} - T_3 - R_{FAULT}$ by switching the T_4 on and T_5 off. By considering $C_{C1,2,3}$ as one effective capacitor the topology is the test circuit. The current i_{C3} for describing the fault current can be expressed by the differential equation:

$$\frac{1}{C_{C1,2,3}}\int i_{C3}dt + L_C\frac{di_{C3}}{dt} + L_{LOAD}\frac{di_{C3}}{dt} + i_{C3}R_{FAULT} = V_{DC} \qquad (21)$$

where the voltage across C_{bank} is considered DC due to large C_{bank}. with the initial conditions

$$i_{C3}(t_{c5}) = i_{FAULT}(t_{c5}) \text{(A)}$$

$$V_{C_{C1,2,3}}(t_{c5}) = V_{C_{C1,2}}(t_{c5}) + V_{C_{C3}}(t_{c5}) \text{ (V)}$$

where $V_{C_{C3}}(t_{c5}) = \frac{1}{3}V_{C_{C1,2,3}}(t_{c1})$, which yields

$$V_{C_{C1,2,3}}(t_{c5}) = V_{C_{C1,2}}(t_{c5}) + \frac{1}{3}V_{C_{C1,2,3}}(t_{c1}) \text{(V)}$$

for $R_{FAULT} < 2\sqrt{\frac{L_{LOAD}}{C_{C1,2,3}}}$:

$$i_{C3}(t) = 2K_{1,,,}e^{-\delta_2 t}\cos(\omega_{3,,,}t - \theta''') \quad \text{(A)} \qquad (22)$$

$$V_{C_{C1,2,3}}(t) = \frac{2K_{1,,,}}{C_{C1,2,3}\omega_{4,,,}}\cos(\beta_{2,,,} - \theta''')$$

$$-\frac{2K_{1,,,}}{C_{C1,2,3}\omega_{4,,,}}e^{-\delta_2 t}\cos(\omega_{3,,,}t - \theta''' + \beta_{2,,,})] + V_{C_{C1,2,3}}(t_{c5}) \text{ (V)}$$

where $\delta_2 = \frac{R_{FAULT}}{2(L_{LOAD}+L_C)}$; $\omega_{3,,,}^2 = \frac{1}{(L_{LOAD}+L_C)C_{C1,2,3}} - \left(\frac{R_{FAULT}}{2(L_{LOAD}+L_C)}\right)^2$

$\omega_{4,,,} = \sqrt{{\delta_2}^2 + \omega_{3,,,}^2}$; $\beta_{2,,,} = \tan^{-1}\frac{\omega_{3,,,}}{\delta_2}$

$$K_{1,,,} = \sqrt{(\frac{i_{FAULT}(t_{c5})}{2})^2 + (\frac{\frac{V_{DC} - V_{C_{C1,2,3}}(t_{c5})}{L_{LOAD} + L_C} - \delta_2 i_{FAULT}(t_{c5})}{2\omega_{3,,,}})^2}$$

$$\theta''' = \tan^{-1}\frac{\frac{V_{DC} - V_{C_{C1,2,3}}(t_{c5})}{L_{LOAD} + L_C} - \delta_2 i_{FAULT}(t_{c5})}{\omega_{3,,,} i_{FAULT}(t_{c5})}$$

The VCB voltage tracks the residual voltage $V_{C_{C1}} + V_{C_{C2}} + V_{C_{C3}}$ until interruption finishes. Then the commutation capacitors are reset, ready for the next interruption. The VCB voltage is dominated by the commutation capacitor voltage, thus it can be expressed by the following piecewise function:

$$V_{VCB} = \begin{cases} V_{C_{C1}}(t) = \frac{2K_{1'}}{C_{C1}\omega_{4'}}[\cos(\beta_{2'} - \theta') - e^{-\delta_2 t}\cos(\omega_{3'}t - \theta' + \beta_{2'})] + V_{C_{C1}}(t_{c3}) & (t_{c3} \le t \le t_{c4}) \\ V_{C_{C1,2}}(t) = \frac{2K_{1''}}{C_{C1,2}\omega_{4''}}[\cos(\beta_{2''} - \theta'') - e^{-\delta_2 t}\cos(\omega_{3''}t - \theta'' + \beta_{2''})] + V_{C_{C1,2}}(t_{c4}) & (t_{c4} \le t \le t_{c5}) \\ V_{C_{C1,2,3}}(t) = \frac{2K_{1'''}}{C_{C1,2,3}\omega_{4'''}}[\cos(\beta_{2'''} - \theta''') - e^{-\delta_2 t}\cos(\omega_{3'''}t - \theta''' + \beta_{2'''})] + V_{C_{C1,2,3}}(t_{c5}) & (t_{c5} \le t \le t_{c6}) \end{cases} \quad (23)$$

The fault current also can be represented by a piecewise function:

$$i_{FAULT} = \begin{cases} i_{C1}(t) = 2K_{1'}e^{-\delta_2 t}\cos(\omega_{3'}t - \theta') & (t_{c3} \le t \le t_{c4}) \\ i_{C1,2}(t) = 2K_{1''}e^{-\delta_2 t}\cos(\omega_{3''}t - \theta'') & (t_{c4} \le t \le t_{c5}) \\ i_{C3}(t) = 2K_{1'''}e^{-\delta_2 t}\cos(\omega_{3'''}t - \theta''') & (t_{c5} \le t \le t_{c6}) \end{cases} \quad (24)$$

In order to define the time intervals after VCB current zero, the performance of commutation capacitor voltage and current is investigated further. By comparing equations (23) to (24); they are similar expression except the initial conditions, including i_{FAULT}, commutation capacitance C_C, and initial capacitor voltage V_C. Since the fault path has a large time constant compared to the commutation circuit, the fault current i_{FAULT} can be considered constant during the commutation period.

Fig. 4(a) shows the commutation capacitor voltage and current. The current i_C through the commutation capacitor equals the fault current i_{FAULT}. Due to the stored magnetic energy transfer and the residual voltage of the commutation capacitor, there is an initial increase in i_C after the current-zero. Since the solid-state switches offer uni-directional conduction, the commutation capacitor should be fully charged and is kept unchanged when i_C reduces to zero.

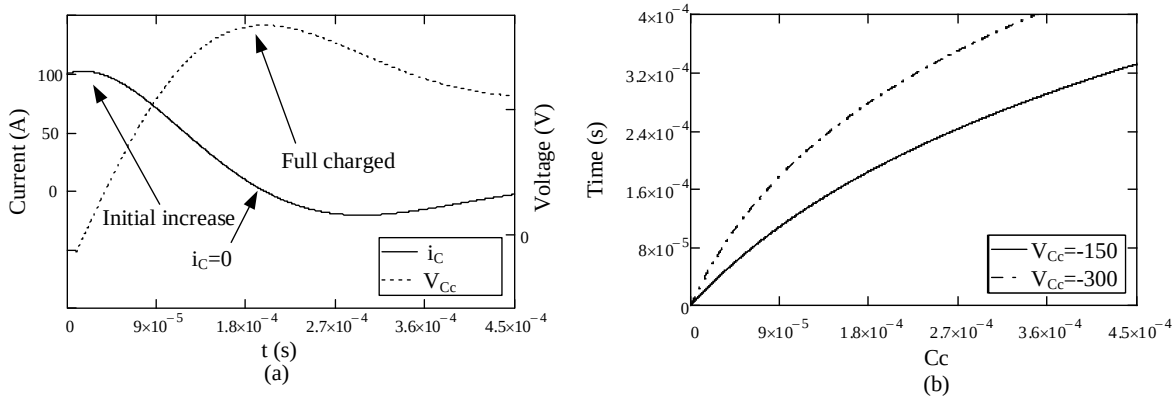


Fig. 4: *Commutation capacitor voltage and current profiles.*
(a) The performance of commutation capacitor current and voltage after current-zero and
(b) Maximum discharge time with two initial commutation capacitor voltages as a function of commutation capacitance.
($I_{FAULT} = 100\text{A}, V_{DC} = 600\text{V}, L_C = 49.4\mu\text{H}, L_{LOAD} = 1.7\text{mF}, R_{FAULT} = 6\Omega$)

The most significant design aspect is the period immediately following the current-zero in the VCB. Thus it is convenience to specify the duration from the initial residual capacitor voltage to when it retains zero charge. Due to the complexity of the commutation capacitor voltage equation, it is difficult to directly define a time interval equation. Capacitor voltage V_C approaches zero when i_C increases to its maximum. The approximate equation for the time interval after current-zero is obtained by equating the current differential equation (24) with zero, which gives:

$$T_C = -\frac{\ln(-\frac{e^{2j\theta}(\delta_2 + \omega_3 j)}{\delta_2 - \omega_3 j})j}{2\omega_3} \tag{25}$$

where $j = \sqrt{-1}$

Hence

$$T_{C4}=t_{c4} - t_{c3} = -\frac{\ln(-\frac{e^{2j\theta'}(\delta_2+\omega_{3\prime} j)}{\delta_2-\omega_{3\prime} j})j}{2\omega_{3\prime}} \tag{26}$$

$$T_{C5}=t_{c5} - t_{c4} = -\frac{\ln(-\frac{e^{2j\theta''}(\delta_2+\omega_{3\prime\prime} j)}{\delta_2-\omega_{3\prime\prime} j})j}{2\omega_{3\prime\prime}} \tag{27}$$

The plots in Fig. 4(b) are for equation (26) with two initial residual capacitor voltages. The time interval increases with an increase in commutation capacitance and its initial residual voltage.

Since these time intervals are based on maximum discharge ability for each commutation capacitor voltage, it ensures i_{VCB} produces second current-zero if interruption failure occurs at the first current-zero.

There are six sequential time intervals, T_{C1}-T_{C2}-T_{C3}-T_{C4}-T_{C5}-T_{C6}, in the operation cycle of the cascaded commutation circuit. T_{C3} and T_{C4} are from the same signal impulse, which triggers switches T_3-T_4-T_5 in the correct sequence. The first three time intervals T_{C1}-T_{C2}-T_{C3} involve the di/dt reduction while the remainder are for improving the re-applied dv_{VCB}/dt. Since T_{C3} and T_{C4} are derived from the same signal, they can be considered 'joined', linking the reducing current before current-zero and the increasing voltage after current-zero. They maintain continuity during commutation. This means, commutation current i_{L_C} has to rise to i_{FAULT} in first two time intervals. Assuming the fault current is commutated into the VCB at the end of the first interval; the interruption process can be expressed as follows:

$$T_{C10}=t_{c1}-t_{c0}=\frac{-\sin^{-1}\frac{i_{FAULT}(t_{c1})Z}{V_{DC}}}{\omega_0} \tag{28}$$

where $\omega_0=1/\sqrt{L_C C_{C1,2,3}}$ (rad/s)

If i_{FAULT} is commutated at t_{c2}, equation (9) for describing the time interval T_{C2} can be rewritten as:

$$T_{C20}=t_{c2}-t_{c1}=\frac{-\sin^{-1}\frac{V_{C_{C1,2}}(t_{c1})\times i_{FAULT}(t_{c2})+L_C\times i_{FAULT}(t_{c2})\times\omega_{0'}\times A}{\left(C_{C1,2}\times\left(V_{C_{C1,2}}(t_{c1})\right)^2+L_C\times\left(i_{FAULT}(t_{c2})\right)^2\right)\times\omega_{0'}}}{\omega_{0'}} \tag{29}$$

where $A=\sqrt{\frac{C_{C1,2}\times(V_{C_{C1,2}}(t_{c1}))^2+L_C\times(i_{FAULT}(t_{c2}))^2-L_C\times(i_{FAULT}(t_{c2}))^2}{L_C}}$

$$V_{C_{C1,2}}(t_{c1})=-⅔V_{DC}\cos\omega_0 t_{c1}$$

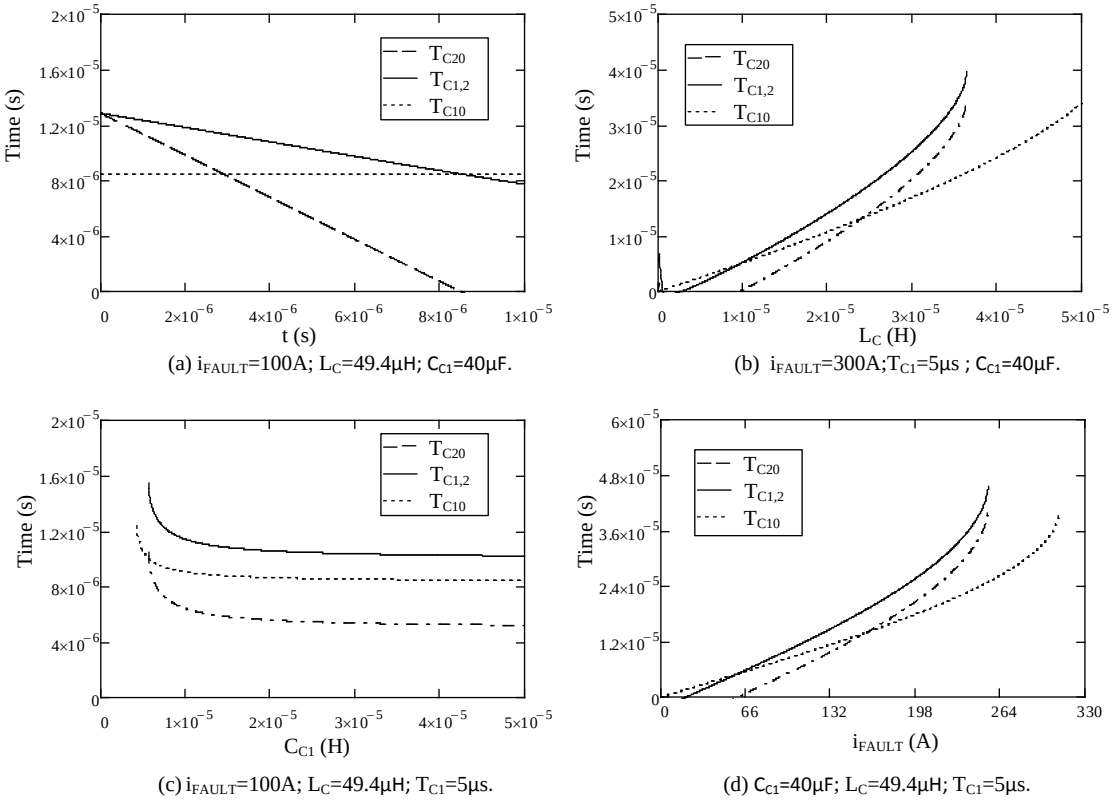
$i_{FAULT}(t_{c1})=i_{FAULT}(t_{c2})$ due to large time constant of the fault path. Now considering t_{c0} as a start point, $T_{C1}=t_{c1}-t_{c0}=t$, the total duration can be defined as:

$$T_{C1,2}=t_{c2}-t_{c0}=T_{C2}+T_{C1}=T_{C20}+t \tag{30}$$

To specify the time interval becomes a trade-off between T_{C1} and T_{C2}.

The graphs in Fig. 5 represent equations (29) to (31) for the different conditions but at a fixed 600V DC source. Based on the fixed fault current of 100A and commutation parameters including $L_C=49.4\mu H$ and $C_{C1}=40\mu F$, Fig. 5(a) compares the total duration $T_{C1,2}$ and second time interval T_{C20}, as well as the first current-zero time T_{C10} of the test circuit. It reveals how the di/dt is reduced by the cascaded circuit. The horizontal axis represents the first time interval, $T_{C1}=t_{c1}-t_{c0}=t$. The second time interval reduces as the first time interval increases, meaning a longer first time interval will result in less time for the second interval, thereby reducing$T_{C1,2}$. To maximise the cascaded circuit commutation time, the second time

interval should dominate commutation until current-zero. This means the switch T_5 turns on before T_4. However, since there is energy loss during capacitor voltage reversal, it is prudent to initialise the commutation current with maximum energy, then switch into the second path.



(a) i_{FAULT}=100A; L_C=49.4μH; C_{C1}=40μF.

(b) i_{FAULT}=300A;T_{C1}=5μs ; C_{C1}=40μF.

(c) i_{FAULT}=100A; L_C=49.4μH; T_{C1}=5μs.

(d) C_{C1}=40μF; L_C=49.4μH; T_{C1}=5μs.

Fig. 5: *Time interval maximum values as a function of circuit parameters, with a 600V DC source*
(a) First time interval
(b) Commutation inductance
(c) Commutation capacitance
(d) Interruption current

With fixed 300A fault current, $C_{C1} = 40\mu F$ and first time interval $T_{C1} = 5\mu s$, Fig. 5(b) shows the relationship between the time intervals and the commutation inductance L_C. With an increase in L_C the time intervals are increased. At low inductance, the time intervals have similar values. At higher inductance, the commutation time differences become tens of μs, which is significant with respect to the VCB, since the vacuum arc has a fast recovery rate [6, 31, 32]. It is not possible for interruption with low inductance, which corresponds to large di/dt. The objective of the cascaded circuit is to increase the interruption probability with relatively small commutation inductance at a short gap distance.

After utilizing a fixed fault current of 100A, $L_C = 49.4\mu H$, and a first time interval $T_{C1} = 5\mu s$, Fig. 5(c) shows that the commutation capacitance has little effect on the commutation time thereby does not influence the di/dt.

With a first time interval of 5μs and commutation parameters $L_C = 49.4\mu H$ and $C_{C1} = 40\mu F$, the relationship between the time intervals and the fault current is shown in Fig. 5(d). The time intervals display an ever-increasing trend with an increase in the fault current; but are similar at low i_{FAULT}.

In summary, although there are six time intervals, T_{C1}-T_{C2}-T_{C3}-T_{C4}-T_{C5}-$T_{C6,}$ in the cascaded circuit, only T_{C1}-T_{C2}-T_{C3}-T_{C4}-T_{C5} need to be specified because T_{C6} is a long signal impulse lasting until the end of the interruption. T_{C3}-T_{C4} are from same signal, thus there are only four signals to be processed. In order to specify these time intervals, the first two intervals should be defined first by utilizing equations (29) and (30). The remaining two can be obtained from equation (26) in terms of different initial conditions.

III. Simulation and experimental results

The cascaded hybrid circuit was PSPICE simulated with the results post-processed in MATLAB. For comparison convenience, the simulation and experimental results are presented side by side, left and right respectively.

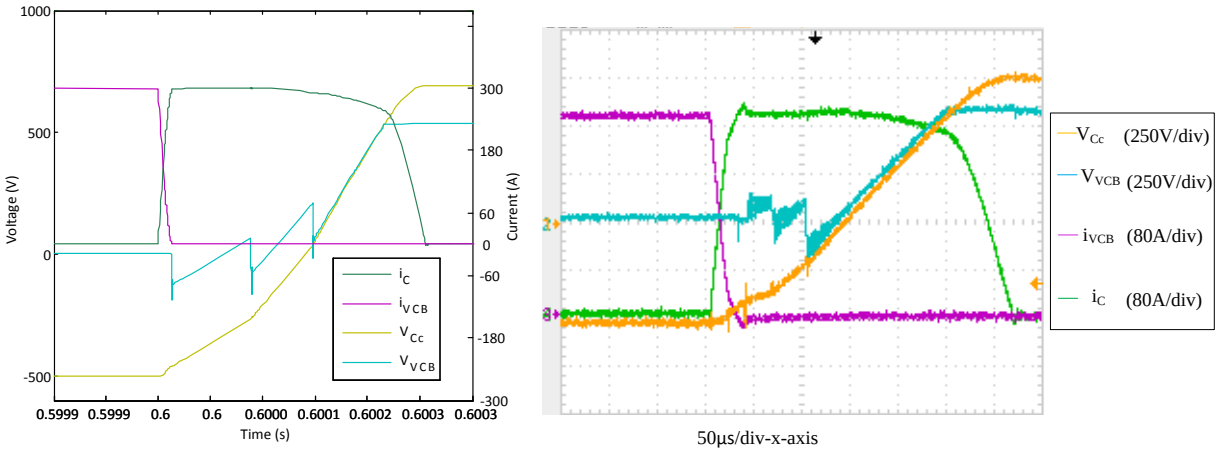
An AC vacuum breaker is used as the circuit breaker in the experiment. The breaker characteristics are shown in Table 1.

Table 1: Technical data on triple-pole vacuum circuit breaker [24].

Operating voltage, kV	1.2
Current rating, A	150
Max motor duty, kW	225
Max transformer duty, kVA	250
Closing coil closing, W 110A ac hold in, W	250 12
Weight of contactor, kg	4
Thermal rating (1s), kA	4
Mechanical life, cycles	5×10^6

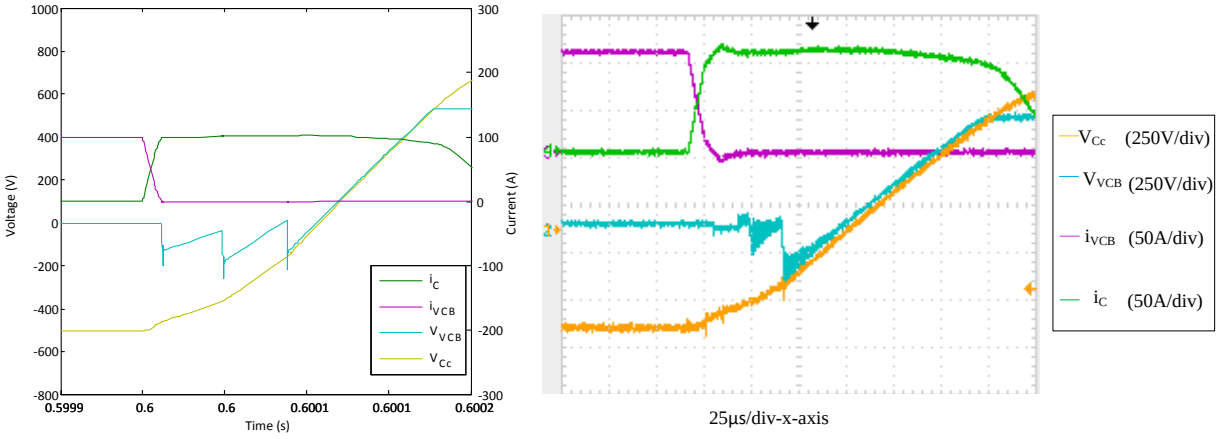
Fig. 6 and Fig. 7 show a successful interruption at first current-zero with 110A and 330A fault currents respectively. The general form and shape are the same in both cases. The VCB current i_{VCB} is reduced as the counter-current i_C rises, then the decline rate of i_{VCB} is modified when the commutation path is switched. After the current-zero the VCB experiences a stepped-shaped pulse, since the residual voltages across each commutation capacitor, $V_{C_{C1}} - V_{C_{C2}} - V_{C_{C3}}$, are charged step by step.

A successful interruption at a second current-zero with a 110A fault is shown in Fig. 8. i_{VCB} reaches a second current-zero with a lower amplitude due to the capacitors progressively discharging. The primary objective for the cascaded circuit is to improve the di/dt by increasing the commutation time, thereby increasing the interruption probability at the first current-zero.



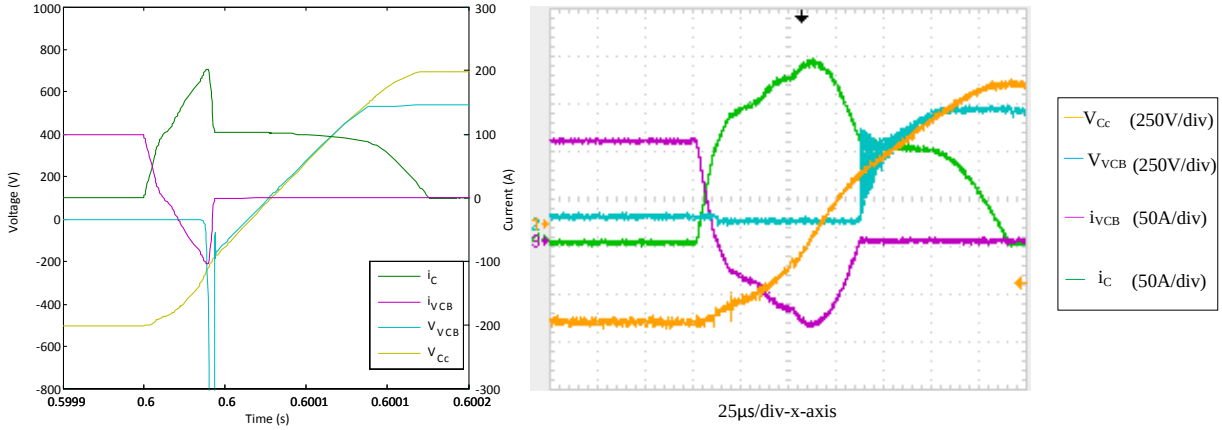
(a) (b)

Fig. 6: *Cascaded commutation circuit voltage and current at first current-zero interruption*
(a) Simulation results
(b) Experimental results
($V_{DC} = 600\text{V},\ C_{bank} = 7\text{mF},\ C_{C1,2,3} = 120\mu\text{F},\ R_1 = 200\Omega,\ L_C = 49.4\mu\text{H},\ L_{LOAD} = 1.7\text{mH},\ R_{LOAD} = 600\Omega,\ R_{FAULT} = 1.7\Omega$)



(a) (b)

Fig. 7: *Cascaded commutation circuit voltage and current at first current-zero interruption*
(a) Simulation result
(b) Experimental result
($V_{DC} = 600\text{V},\ C_{bank} = 7\text{mF},\ C_{C1,2,3} = 12.81\mu\text{F},\ R_1 = 200\Omega,\ L_C = 49.4\mu\text{H},\ L_{LOAD} = 1.7\text{mH},\ R_{LOAD} = 600\Omega,\ R_{FAULT} = 5.5\Omega$)



(a) (b)

Fig. 8: *Cascaded commutation circuit voltage and current in a successful interruption at the second current-zero interruption*

(a) Simulation results

(b) Experimental results

($V_{DC} = 600\text{V},\ C_{bank} = 7\text{mF},\ C_{C1,2,3} = 12.81\mu\text{F},\ R_1 = 200\Omega,\ L_C = 49.4\mu\text{H},\ L_{LOAD} = 1.7\text{mH},\ R_{LOAD} = 600\Omega,\ R_{FAULT} = 5.5\Omega$)

IV. CONCLUSION

This paper proposed a cascaded commutation circuit, without snubber circuits, inspiration by a saturable reactor which slowed the *di/dt* prior to current-zero and then produced a low voltage amplitude pulse. The validity of cascaded commutation principle was confirmed by simulation and experimentally. The experimental results are conducted at a lower power level in order to validate the commutation circuit performance.

Successful fault current interruption at the first and second current-zeros is achieved with decreased di/dt and dv_{VCB}/dt.The proposed cascaded commutation circuitry shows only three cascaded voltage stages but this can be increased, depending on the voltage resolution of the dV_{VCB}/dt and the DC system voltage. T_2 and T_4 in Fig. 1 can be combined into a single back-to-back configuration, saving two diodes, but is not shown in this paper to give circuit analysis simplicity. The proposed circuit architecture consist of a single IGBT device in each cascaded voltage stage, which its voltage rating is associated with its capacitor voltage level. Lower IGBT voltage devices can be used to reduce the power losses during the commutation process but will result in more cascaded voltage stages. However, the voltage resolution of dV_{VCB}/dt is increased.

Conventional series connected capacitors required shunted resistors for voltage balancing and discharge of the capacitors energy when the power system is disconnected. However, when this technique is employed in the proposed circuit, the capacitors voltage need to be trickled charge by T1 to maintain its DC voltages as DC fault does not occur frequently. This approach is currently employed in the proposed circuit. The alternative approach in the proposed technique is not using shunt resistor but overrate the capacitor voltage rating according to the capacitor tolerances. This eliminates the trickle charge process but required auxiliary circuit to discharge the capacitor energy when repair or maintenance work to the system is necessary.

Timing control on the respective gate signals in the three level cascaded voltage stages are accomplished by a mid-range 16-bit micro-controller (dsPIC30F2020), utilizing only 60% of the controller capability. The controller algorithm is not presented as the primary focus is to demonstrate the proposed commutation circuit performance. Isolation of the IGBT gate drives between each voltage stages can be accomplished by utilizing fibre-optic technologies, greatly enhancing the reliability of the cascaded commutation circuit.

The proposed technique is analysed and demonstrated under uni-directional DC current flow system. However, its feasibility in bidirectional DC current flow system is possible by replacing the diodes (*T2, T4, T5* and *T6*) in the cascaded commutation circuit with IGBTs. This

allows bidirectional current flow in the commutation circuit. Alternative control mechanism is needed for bidirectional DC current fault interruption. Detailed operational structure of the proposed technique for bidirectional current interruption is not presented in this paper.

Total failure in operation of the devices during fault condition can result DC arcing in the mechanical DC breaker. Failure Mode Evaluation Analysis (FMEA) on the proposed commutation circuit is not presented in this paper and is proposed for future works.

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