

High Speed Integrated Digital to Light Converter for Short Range Visible Light Communication

Aravind V. N. Jalajakumari, *Member IEEE*, Enyuan Xie, Jonathan McKendry, *Member IEEE*, Erdan Gu, Martin D. Dawson, *Fellow IEEE*, Harald Haas, *Member IEEE*, Robert K. Henderson, *Senior Member IEEE*

Abstract—Design details and characterisation results of an integrated digital to light converter (DLC) for short range visible light communication (VLC) is reported. The integrated DLC can generate 16 light intensity levels at fast switching speeds, up to 500 MHz, thus enabling fast intensity modulated VLC. Data rates up to 365 Mb/s are achieved with bit error rate (BER) 1×10^{-3} at a link distance of 5 cm and average electrical power efficiency of 70%. Optimisation in the micro light emitting diode (μ LED) manufacturing process has resulted in approximately three fold increase in data rate of the system. Spectrally efficient modulation schemes like orthogonal frequency division multiplexing (OFDM) and pulse amplitude modulation (PAM) are also demonstrated using this integrated system.

Keywords—Visible light communication, DLC, optical wireless communication, DAC, CMOS

I. INTRODUCTION

In visible light communication (VLC) the intensity of light is modulated to transmit digital data into free space [1]. The availability of the unregulated visible light spectrum and the finite radio frequency (RF) spectrum has led to research interest in VLC. High speed VLC systems require light sources with fast switch ON/OFF times to enable high speed communication. Semiconductor light emitting diodes (LEDs) are suitable candidates for this due to their high inherent bandwidth [2]. Another advantage of LEDs is that they can be controlled electronically. High speed VLC links have been realised using micro light emitting diodes (μ LEDs) [3], [4] and commercial LEDs [5], [6], [7]. These VLC links utilise a single LED to establish communications by varying either the voltage or current, thereby achieving intensity modulation.

A single VLC link can be established using multiple LEDs, whereby turning on more than one LED, the intensity of light generated can be varied [8]–[11]. This is achieved using a digital to light converter (DLC), where each input digital code translates to turning on a corresponding number of LEDs to represent a proportional intensity level. Fig. 1 shows a 2-bit DLC output LED operation at 2 different digital input codes. This method of varying the intensity of the light for modulation has advantages including power efficiency and assured monotonicity in the output power levels. Published driver

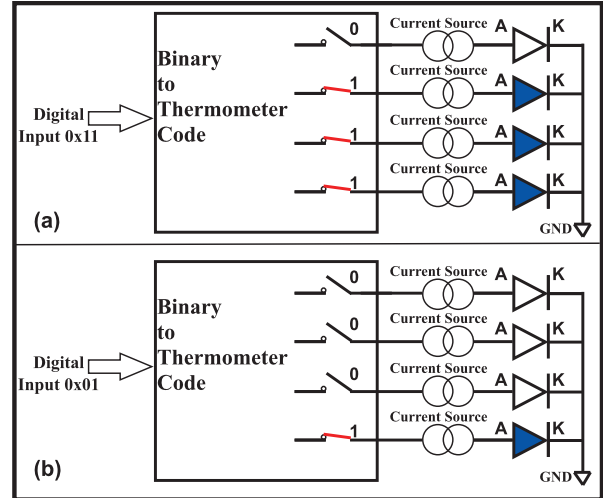


Fig. 1: Illustration of DLC system operation; (a) With digital input of 3 (0x11); (b) With digital input of 1 (0x01)

architectures [8], [9] utilise discrete components to realise such communication links, whereas [11] realises an integrated complimentary metal oxide semiconductor (CMOS) Gallium Nitride (GaN) DLC system. Effects of μ LED mismatch in such a system was studied in [10]. Symbol rates up to 100 MS/s have been achieved in [11] using 4-PAM and a voltage mode drive scheme.

In this study, a digital current mode driver is employed to drive an array of μ LEDs realising a DLC. An improved metallisation scheme has given a better linear response compared with [11]. Since the LED driver is a DLC, it has the flexibility to accept an incoming data stream generated with any standard modulation scheme, however results are presented only for OFDM modulation. In this paper, an integrated VLC transmitter is proposed with 16 μ LEDs wire bonded on top of a current steering digital-to-analog converter (DAC) based CMOS driver. Such a driver would be relevant to short range VLC applications including internet of things (IoT).

Aravind V. N. Jalajakumari, Harald Haas and Robert K. Henderson are with the School of Engineering, University of Edinburgh, Edinburgh, EH9 3JL, United Kingdom e-mail: [a.venugopalan, h.haas, robert.henderson]@ed.ac.uk

Enyuan Xie, Jonathan McKendry, Erdan Gu and Martin D. Dawson are with the Institute of Photonics, University of Strathclyde, Glasgow G1 1RD, United Kingdom. e-mail: [enyuan.xie, jonathan.mckendry, erdan.gu, m.dawson]@strath.ac.uk

The rest of the paper is organised as follows. Driver circuit architecture, μ LED array construction and wire bonding details are presented in Section II. In Section III the experimental setup is presented. In Section IV, DLC characteristics and data link measurement results are given. Conclusions are given in Section V.

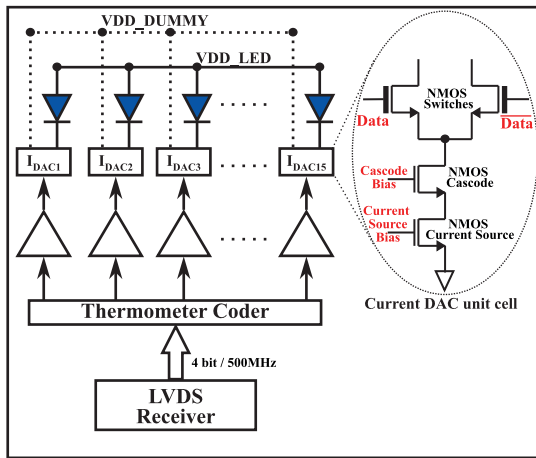


Fig. 2: Block diagram of DLC system with μ LED

II. SYSTEM DESCRIPTION

The integrated DLC consists of two components, namely a current steering DAC based CMOS LED driver and GaN based μ LED array with 16 μ LEDs.

A. Driver architecture

Fig. 2 shows the block diagram of the CMOS DLC. 4-bit data received through a high speed (500 MHz) low voltage differential signalling (LVDS) receiver is converted to a 16 bit thermometer code. Each bit in the thermometer code is converted to a differential mode signal and buffered, which controls 16 differential current cells (I_{DAC}). Each current cell has an adjustable output current (1mA to 16mA) and two output branches (differential structure), with out-of-phase currents, namely, main branch and dummy branch. The current cell architecture is also shown in Fig. 2.

A current cell consists of an N-channel metal oxide semiconductor field effect transistor (NMOS) current source transistor, cascode transistor and differential pair switches. It is capable of operating up to 500 MHz switching speeds. A high bit from the thermometer code will cause all current to flow through the main branch and no current through the dummy branch; a low bit will reverse the current flow. The main branch of each driver is connected to a customized pad opening onto which μ LEDs are wire bonded and dummy branch is tied to 1.8 V rail.

B. μ LED array construction

The GaN μ LED array is fabricated in a common anode process. Since the driver has NMOS current sources with open drain architecture which requires individual cathodes from each μ LED, a common anode construction is used. The μ LED arrays are fabricated from commercial 450 nm Indium Gallium Nitride (InGaN)/ Gallium Nitride (GaN) LED wafer grown on the sapphire substrate with c-plane (0001) surface orientation. Each one-dimensional linear array consists of 16 top-emitting μ LED elements. In order to be compatible with NMOS transistor-based drivers, these arrays have a reversed configuration compared with conventional ones [3]. Each μ LED element in these novel arrays is individually addressed

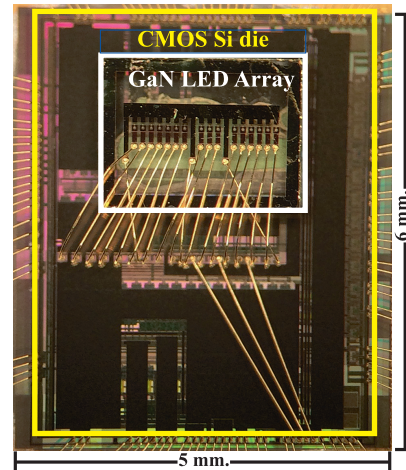


Fig. 3: Photograph of DLC system with μ LED

by its own n-type contact (cathode) with a shared p-type contact (anode). To achieve this configuration, 16 Gallium Nitride (GaN) mesas are firstly etched down onto the sapphire substrate by Cl₂-based inductively coupled plasma (ICP). Then, a disk-shaped μ LED element with a diameter of 24 μ m is generated on each mesa through another ICP etching to n-type GaN. These steps enable the isolation between the μ LED elements from the shared p-type and n-type GaN layers. After these etching steps, metal contact to p-type GaN is formed through e-beam evaporation and thermal annealing. Two metal schemes, 20 nm Pd (labelled as SEG1) and 10/20 nm Ni/Au (labelled as SEG2) are employed for comparison. Annealing conditions for the above schemes are 300 °C in Nitrogen (N₂) ambient and 500 °C in air ambient, respectively. The metallisation on the isolated n-type GaN mesa is formed by sputtering a Ti/Au (50/200 nm) metal bilayer. Then, a 300 nm thick SiO₂ layer is deposited by plasma enhanced chemical vapour deposition. After selectively removing SiO₂ on top of each element, another Ti/Au metal bilayer is deposited to interconnect LED elements and, thus, form a shared p-type contact (anode).

C. Wire bonding and Packaging

The CMOS LED driver and GaN μ LED array are wire bonded to establish electrical connectivity. Customised 60 μ m pads are provided at the centre of the CMOS LED driver to facilitate the wire bond. Standard 25 μ m gold wire is used for bonding purposes in Palomar 8000 bonding machine. Fig. 3 shows the bonded DLC chip. The bonded chip is packaged in a 120 pin ceramic pin grid array (CPGA) package with transparent lid.

III. EXPERIMENTAL SETUP

A printed circuit board (PCB) [12] with an off-the-shelf field programmable gate array (FPGA) daughter card (Opal Kelly XEM6310) is used to house the DLC chip. The main functions of the PCB are to provide adjustable external bias control, supply adequate power and control/data interface for the DLC chip. VDD_LED node is supplied from an external 8.2 V direct current (DC), whereas VDD_DUMMY is tied to 1.8 V internally through wire bonding (see Fig. 2). The serial

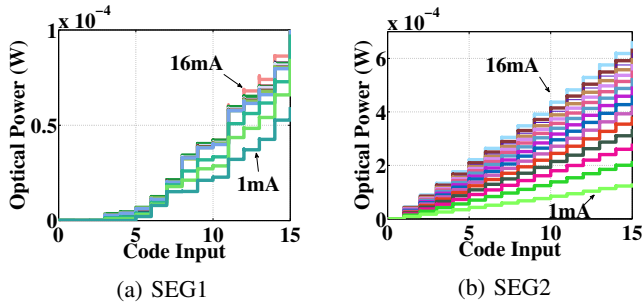


Fig. 4: Input-Output characteristics of SEG1 and SEG2 chips

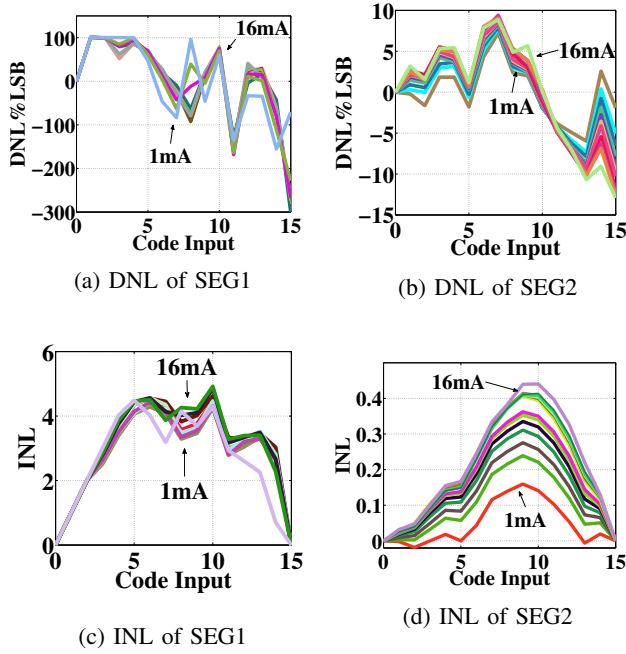


Fig. 5: DNL and INL of SEG1 and SEG2 chips

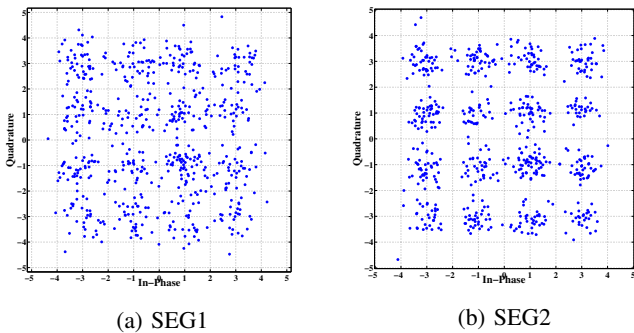


Fig. 6: 16-QAM constellation of SEG2 and SEG1 chips at a clock rate of 200MHz

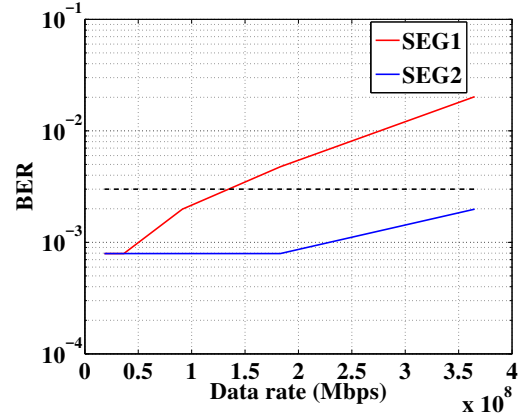


Fig. 7: BER of SEG1 and SEG2 chips at 16-QAM, 200 MHz

interface of the DLC chip enabled current variation during different experiments (1 mA - 16 mA). For the SEG2 chip the bias current was 8 mA at 8.2 V, whereas due to its inferior performance a higher bias current (11 mA) and voltage (11 V) was needed for the SEG1 chip to generate the same light output. Data to be transmitted through the μ LEDs and control signals for the DLC chip are generated in a personal computer (PC) and sent to the FPGA card through a universal serial bus (USB) interface. A custom receiver module [13] with electrical bandwidth of 850 MHz is used to receive the data. The receiver module has a Hamamatsu S8890 Si avalanche photodiode (APD), custom built concentrator and an off-the-shelf transimpedance amplifier (Maxim MAX3665). The received data is sampled using a digital storage oscilloscope (DSO) (Agilent 7402D) and processed offline in Matlab. The distance between the μ LED array and the APD receiver is 5 cm.

IV. DLC RESULTS

Various static characteristics of the DLC are measured to quantify its performance. These are input-output characteristics; differential non-linearity (DNL) [14], which is the difference between the actual output step and ideal least significant bit (LSB) step expressed in LSBs; and integral non-linearity (INL) [14], which is the difference between actual output and ideal output expressed in LSBs. All static measurements are performed at different bias current configurations (1 mA to 16 mA in steps of 1 mA).

A. Static characteristics

Input-output characteristics of both SEG1 and SEG2 are shown in Fig. 4. The output power of SEG2 is ~ 6 times that of SEG1. It can also be seen that the SEG2 chip offers better linearity over the code range compared with SEG1. Both SEG1 and SEG2 systems are monotonic due to the thermometer coding scheme in the DAC. Both DNL and INL of the 4 bit segmented DLC system are characterised. For 4-bit linearity, INL of the DLC system should be within 0.5 LSB which implies the DNL should be within ± 1 LSB. Fig. 5 shows DNL and INL for both SEG1 and SEG2 chips. The SEG2 chip has its DNL and INL within limits whereas the SEG1 chip does not due to its inferior linearity. The INL

performance of the SEG2 chip indicates 5 bits performance. Better linearity of SEG2 chip can be attributed to the contact metallisation scheme (Ni/Au) which gives better performance compared with SEG1 (Pd). The average power efficiency of the driver is calculated assuming a uniform distribution of ones and zeros in a random information signal thus on an average 8 LEDs are in ON state and 8 in the OFF state. An individual LED current of 16 mA, results in 128 mA current through both main and dummy branch. VDD_LED of 8.2 V (7 V across LED and 1.2 V across the driver) results in an average ON LED output power of 0.9 W and average ON driver power of 0.15 W. VDD_DUMMY of 1.8 V results in average OFF driver power of 0.23 W. Average power efficiency is the ratio of LED output power (0.9 W) to the total input power to the driver (0.9 + 0.23 + 0.15 W) is then 70%. It is possible to reduce the dummy node supply to 1.2 V, while keeping all of the transistors in saturation thereby maintaining linearity and reducing power dissipation further.

B. Data transmission results

A data rate up to 365 Mbps has been achieved with OFDM modulation (16 QAM, cyclic prefix (CP) = 10, 128 point fast Fourier transform (FFT)) while clocking the SEG2 chip at 200 MHz. A clipping limit of $\pm 3.2\sigma$, which results in negligible distortion [15], was used and kept constant for all experiments. Compared to discrete component DLC implementations [8], this is approximately a 10 fold increase in data rate. This is due to circuit miniaturisation, high bandwidth μ LEDs and a better metallisation scheme. Fig. 6 shows the constellation diagram for both SEG1 and SEG2 chips while transmitting data in the configuration mentioned above. It is evident from the constellation that the non-linear transfer characteristic of the SEG1 chip is worsening the BER. The data rate versus BER is shown in Fig. 7. The SEG2 chip has its BER within forward error correction (FEC) limits of 1×10^{-3} [16] up to 365 Mbps, and for the SEG1 chip the maximum possible data rate is ~ 130 Mbps. The OFDM bit stream length was 32 kbits limiting the BER to 7.9×10^{-4} . The link distance of 5 cm could be increased further by using additional optical components [17].

V. CONCLUSION

Integration of GaN μ LEDs and a CMOS LED driver into a single package has resulted in a short range VLC transmitter capable of transferring data up to few hundred Mbps. This DLC drive scheme combined with improvements in μ LED metallisation scheme are shown to be suited for complex modulation schemes such as OFDM whilst operating at high power efficiency. Applications such as IoT which require short range VLC transmission would benefit from this system.

VI. ACKNOWLEDGEMENTS

We gratefully acknowledge support by the School of Engineering at the University of Edinburgh for providing a scholarship for this work, which is aligned to the UK Engineering and Physical Sciences Research Council (EPSRC) project EP/K00042X/1. We would also like to thank Grahame Faulkner for providing the optical receiver and Dobroslav Tsonev for providing the decoding firmware.

REFERENCES

- [1] Y. Tanaka, T. Komine, S. Haruyama, and M. Nakagawa, "Indoor visible communication utilizing plural white LEDs as lighting," in *Personal, Indoor and Mobile Radio Communications, 2001 12th IEEE International Symposium on*, vol. 2, Sep 2001, pp. F-81–F-85 vol.2.
- [2] C.-H. Wu, G. Walter, H. W. Then, M. Feng, and N. Holonyak, "4-GHz modulation bandwidth of integrated 2×2 LED array," *Photonics Technology Letters, IEEE*, vol. 21, no. 24, pp. 1834–1836, Dec 2009.
- [3] J. J. D. McKendry *et al.*, "Individually addressable AlInGaN micro-LED arrays with CMOS control and subnanosecond output pulses," *Photonics Technology Letters, IEEE*, vol. 21, no. 12, pp. 811–813, 2009.
- [4] D. Tsonev *et al.*, "A 3-Gb/s single-LED OFDM-based wireless VLC link using a gallium nitride μ LED," *Photonics Technology Letters, IEEE*, vol. PP, no. 99, pp. 1–1, 2014.
- [5] J. Vucic, C. Kottke, S. Nerreter, K. D. Langer, and J. W. Walewski, "513 Mbit/s Visible Light Communications Link Based on DMT-Modulation of a White LED," *Journal of Lightwave Technology*, vol. 28, no. 24, pp. 3512–3518, Dec 2010.
- [6] N. Fujimoto and S. Yamamoto, "The fastest visible light transmissions of 662 Mb/s by a blue LED, 600 Mb/s by a red LED, and 520 Mb/s by a green LED based on simple OOK-NRZ modulation of a commercially available RGB-type white LED using pre-emphasis and post-equalizing techniques," in *Optical Communication (ECOC), 2014 European Conference on*, Sept 2014, pp. 1–3.
- [7] A. H. Azhar, T. A. Tran, and D. O'Brien, "A Gigabit/s Indoor Wireless Transmission Using MIMO-OFDM Visible-Light Communications," *Photonics Technology Letters, IEEE*, vol. 25, no. 2, pp. 171–174, 2013.
- [8] T. Fath, C. Heller, and H. Haas, "Optical Wireless Transmitter Employing Discrete Power Level Stepping," *Lightwave Technology, Journal of*, vol. 31, no. 11, pp. 1734–1743, June 2013.
- [9] J. Yew, S. Dissanayake, and J. Armstrong, "Performance of an experimental optical DAC used in a visible light communication system," in *Globecom Workshops (GC Wkshps), 2013 IEEE*, Dec 2013, pp. 1110–1115.
- [10] H. Qian, S. Zhao, S. Cai, and T. Zhou, "Digitally Controlled Micro-LED Array for Linear Visible Light Communication Systems," *Photonics Journal, IEEE*, vol. 7, no. 3, pp. 1–8, June 2015.
- [11] J. Herrnsdorf, J. McKendry, R. Ferreira, R. Henderson, S. Videv, S. Watson, H. Haas, A. Kelly, E. Gu, and M. Dawson, "Single-chip discrete multitone generation," in *Summer Topicals Meeting Series (SUM), 2015*, July 2015, pp. 47–48.
- [12] A. Jalajakumari, D. Tsonev, K. Cameron, H. Haas, and R. Henderson, "An energy efficient high-speed digital LED driver for visible light communications," in *Communications (ICC), 2015 IEEE International Conference on*, June 2015, pp. 5054–5059.
- [13] D. O'Brien, R. Turnbull, H. L. Minh, G. Faulkner, O. Bouchet, P. Porcon, M. El Tabach, E. Gueutier, M. Wolf, L. Grobe, and J. Li, "High-Speed Optical Wireless Demonstrators: Conclusions and Future Directions," *Lightwave Technology, Journal of*, vol. 30, no. 13, pp. 2181–2187, July 2012.
- [14] D. Johns, *Analog integrated circuit design*. New York: John Wiley & Sons, 1997.
- [15] S. Dimitrov, S. Sinanovic, and H. Haas, "Clipping noise in OFDM-based optical wireless communication systems," *IEEE Transactions on Communications*, vol. 60, no. 4, pp. 1072–1081, April 2012.
- [16] ITU-T, "G.975.1 : Forward error correction for high bit-rate dwdm submarine systems," 2004. [Online]. Available: <http://www.itu.int/rec/T-REC-G.975.1-200402-1/en>
- [17] S. Rajbhandari, H. Chun, G. Faulkner, D. O'Brien, A. V. N. Jalajakumari, K. Cameron, R. Henderson, E. Xie, J. J. D. McKendry, J. Herrnsdorf, E. Gu, M. D. Dawson, D. Tsonev, M. Ijaz, and H. Haas, "Multi-gigabit integrated MIMO visible light communication system: Progress and updates," in *2015 IEEE Summer Topicals Meeting Series (SUM)*, July 2015, pp. 230–231.