

Thyristor Based Modular Multilevel Converter with Active Full-bridge Chain-link for Forced Commutation

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Abstract—Voltage source converter (VSC) such as modular multilevel converter (MMC) has been intensively studied for high voltage direct current (HVDC) applications due to its flexible terminal voltage adjustment, compatibility with weak ac grid and independent active/reactive power control over conventional line-commutated-converter (LCC). However, LCC using thyristors still offers advantages such as high current capability and low semiconductor losses, making it dominant in the construction of large scale converter station. This paper investigates the potential of using thyristor to build the MMC sub-module circuitry, where an auxiliary full-bridge chain-link (FB-CL) is adopted for the controlled transition and forced commutation of main thyristor-bridge, forming the proposed active forced commutated (AFC) thyristor cell. The AFC-MMC combines the advantages of LCC and MMC by the hybrid use of thyristor and self-commutated device, including the high power capacity, optimized efficiency, flexible control and enhanced fault-tolerant ability.

Keywords—modular multilevel converter, thyristor, full-bridge IGBT chain-link, forced commutation, high power capacity, low semiconductor losses, dc fault reverse-blocking ability

I. INTRODUCTION

The construction of the high voltage direct current (HVDC) transmission system requires high capacity and fault-tolerant voltage source converters (VSCs) as the enabling technology to achieve reliable and flexible power flow dispatch. Among various emerging VSC candidates, the modular multilevel converter (MMC) achieves best compromise for a wide range of features such as modularity, improved power conversion efficiency, enhanced wave-shaping ability, continuous dc side current, smooth arm current and reduced dc fault transient current to meet the diverse grid requirements for power quality and reliability [1-7]. Also, MMC results in a reduction in total switching actions compared to conventional two-level VSC. Thus, significant gains in conversion efficiency are achieved through the near elimination of the switching loss; and its semiconductor losses are dominantly contributed by the switch conduction losses, which are further dictated by device on-state characteristics [3, 8]. At present, the on-state voltage drop and power capacity of reliable self-commutated power switches such as the insulated-gate-bipolar-transistor (IGBT) are still

uncompetitive compared to thyristor for similar power rating. For example, 4.5kV/1.8kA IGBT T1800GB45A has a typical forward voltage of 3.7V [9]; while taking the 4.8kV/1.77kA thyristor T1551N48TOH as its rival, the on-state voltage is only 1.57V~1.7V [10]. This implies the conduction losses (main contribution of the converter losses) in half-bridge (HB) MMC using IGBT can be roughly up to twice of that in LCC system given the same DC-link voltage and power rating. The latest generation of MMC HVDC converter station has achieved the semiconductor losses below 1%. However, in a hundreds of MW or GW level system, this power losses can be significant (comparable with large power wind turbines) and will require considerable cooling system installation. Hence, in large power HVDC transmission system, thyristor based line-commutated-converter (LCC) remains dominant by its low semiconductor losses but with its inherited weaknesses to be tolerated such as the power flow reversal difficulty in multi-terminal networks and incompatibility with weak ac grid due to lack of reactive power control, etc. [11-13].

HVDC transmission system is vulnerable to dc side pole-to-pole short circuit fault due to the uncontrolled fault current through the freewheeling diodes. In order to offer dc-fault ride through capability to the MMC, several new cell circuit beyond the basic HB cell has been developed such as the full-bridge (FB) module, mixed cell, clamped diode cell and asymmetrical transition cell. However, all these solutions have to result in reduced efficiency performances relative to HB-MMC, which are caused by the increased total semiconductor device number in the conduction paths [2, 6, 8, 14-16].

In an effort to further improve the efficiency of MMC and make it comparable with the conventional LCC, this paper proposes an investigation of active forced commutated (AFC) thyristor cells as its building block. In this way, several of the topological merits of MMC can be maintained including the independent active and reactive power control as in normal VSC; while achieving high power capability and low power losses that are close to LCC. The forced voltage commutation of the proposed cell is ensured by using an auxiliary chain-link (CL) of FB with self-commutated switches (IGBT is assumed) acting as a controlled voltage source and operating for only short period. In this manner, the majority of the power flows

The authors gratefully acknowledge the support from EPSRC grant EP/K035096/1: "Underpinning Power Electronics 2012 - Converters theme".

through the main thyristor bridge that has very low conduction losses. Also, the dc-fault blocking ability is achieved. Detailed analysis and simulation results for the proposed schemes are presented in later sections.

II. BASIC WORKING LAWS OF THE AFC CELL

The configuration of the proposed AFC cell is depicted in Fig. 1(a), where the series connections of thyristors Q_{1a} and Q_{2a} are employed as the main power switches with anti-parallel thyristor strings Q_{1b} and Q_{2b} for the current freewheeling under full range of power factors. The successful commutation of the thyristor-bridge is guaranteed by the active controlled FB-CL that provides reversible voltage to force the current of the thyristor to be zero and turn off. The auxiliary FB-CL is a string of FB modules using self-commutated IGBT, which provides the small amount of power necessary for the thyristor commutation. In this sense, the average power and cooling design of FB-CL can be light and compact without significant impact on the overall efficiency and power density.

In Fig. 1(a), the gate signals of Q_{1b} and Q_{2b} are determined by the arm current polarity. For example, if the arm current flows out of (into) terminal T_2 , the anti-parallel device Q_{1b} (Q_{2b}) sees no gate drive and remain shut down; while Q_{2b} (Q_{1b}) is kept to be triggered. On the other hand, the main switches Q_{1a} and Q_{2a} are switched by the gate signals coordinated with the controlled voltage source equivalent of the FB-CL for the forced commutation. If the sub-module blocked dc voltage is noted as V_{SM} . The FB-CL should be designed to have internal redundancy that facilitates its behavioral voltage trajectory be able to cross the envelope defined by $\pm\frac{1}{2}V_{SM}$. When the output voltage of FB-CL is higher (lower) than $+\frac{1}{2}V_{SM}$ ($-\frac{1}{2}V_{SM}$), the upper (lower) thyristor string can be reliably turned-off provided its gate signal is removed. The energy balancing of the FB-CL module capacitors inside the proposed AFC cell can be realized by the bipolar voltage generation capability of each FB module in coordination with the voltage sorting results and the load current polarity [17-19].

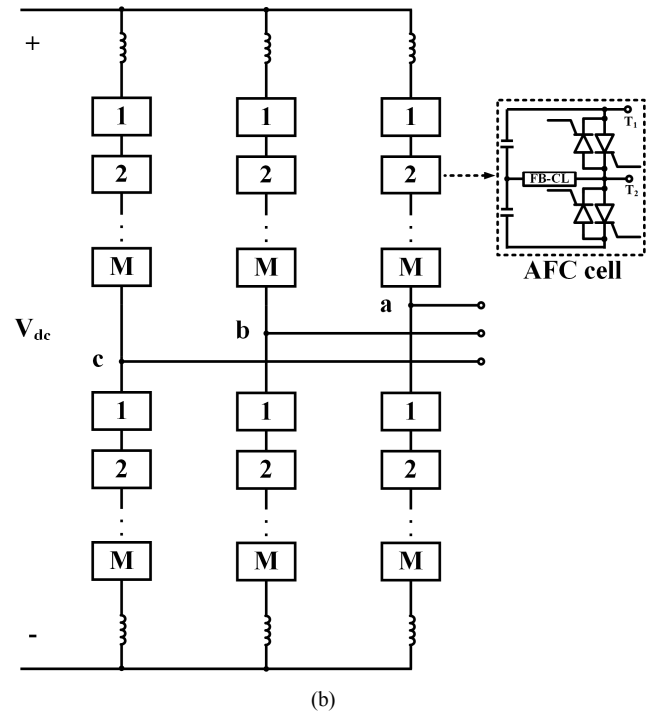
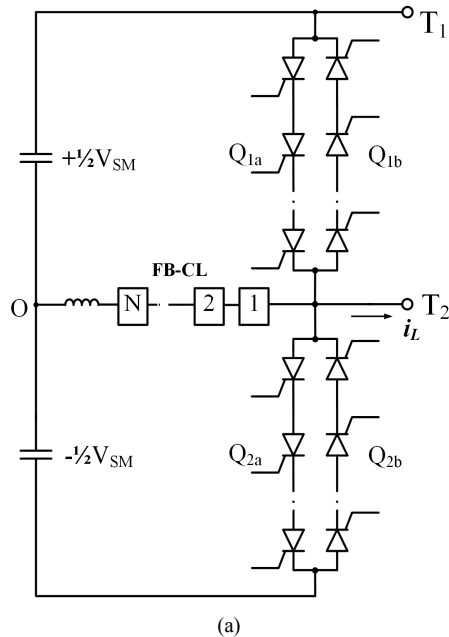


Fig. 1. Schematic of the proposed converter: (a) AFC cell with reverse-blocking capability; (b) AFC-MMC.

MMC using the proposed AFC cells is shown in Fig. 1(b). It is observed that the AFC cell is able to facilitate dc-fault reverse-blocking (RB) capability due to the use of anti-parallel thyristors. When dc short circuit fault is detected, all the gate signals of thyristors and the FB-CL will be blocked after the forced turned-off processes. In this manner, the total FB-CL capacitor voltage ($\frac{1}{2}V_{SM}$) can effectively decay the dc fault current.

Application of the AFC cell to MMC must consider that the switching delay of normal thyristor is much longer than IGBT (typically hundreds of microseconds); as a result, the cell number and sampling frequency of AFC-MMC should be chosen sufficient low. This requires each AFC cell to block high dc voltage, which can be implemented thanks to the mature and reliable series connection of thyristors. For example, if the turn-off time of the selected thyristor is $200\mu s$, a maximum five-level AFC-MMC blocking the full dc-link voltage up to similar level of LCC can be designed with four cells per arm and around 2ms sampling period in staircase mode, i.e. $M=4$ in Fig. 1(b). In this way, the signal channels and control complexity of global controller is reduced provided the modulation of each AFC cell is made autonomous. Also, it is noticed the auxiliary FB-CL operates only during the thyristor commutation process (around 10% of each period), leading to a low average power losses and low requirements on its thermal design.

With this scheme, the proposed converter inherits the topological advantages of MMC and at the same time improves the power capacity and efficiency enormously. It is capable of handling similar power level as the LCC while with reduced filtering size. The use of thyristor (low forward voltage drop) and its soft commutation contribute to higher power conversion

efficiency compared to IGBT based MMC. Therefore, although the maximum voltage level number is limited in the AFC-MMC due to the slow switching speed of the high capacity thyristor (larger filter size than IGBT solutions but smaller than LCC), the proposed scheme is still potentially applicable for HVDC transmission systems, where efficiency is paramount.

III. EFFICIENCY PERFORMANCE OF AFC-MMC

The use of the proposed AFC cell has significant influences on the overall conversion efficiency of the MMC. Generally, due to the reduced total switching instances offered by the topological merits, the total semiconductor losses of MMC are dominantly contributed by its conduction part, which can be calculated through the procedures as follows [20]:

- If the dc side current per phase is noted as I_d , and I_m is the ac side peak current, the conduction angles α and β for positive and negative arm current can be determined by (1).

$$\begin{cases} \alpha = \cos^{-1}\left(\frac{-2I_d}{I_m}\right) = \cos^{-1}\left(-\frac{1}{2}m \cos \varphi\right) \\ \beta = \cos^{-1}\left(\frac{2I_d}{I_m}\right) = \cos^{-1}\left(\frac{1}{2}m \cos \varphi\right) \end{cases} \quad (1)$$

- The forward voltage of power switch can be estimated by (2), where V_{T0} and r_T are the on-state voltage with zero current and slope resistance respectively.

$$V_T = r_T \cdot I_C + V_{T0} \quad (2)$$

- By integrating the instantaneous power of the thyristors over conduction periods, the average power dissipations of the main switches and free-wheeling devices P_A and P_B can be obtained by (3), where F represents the total number of devices in conduction path, φ is the power factor angel and m is the modulation index.

$$\begin{cases} P_A = \frac{I_m F}{16\pi} [(2r_T I_m m^2 \cos^2 \varphi + 4r_T I_m + 8m \cos \varphi V_{T0})\alpha \\ \quad + (3r_T m I_m \cos \varphi + 8V_{T0})\sqrt{4 - m^2 \cos^2 \varphi}] \\ P_B = \frac{I_m F}{16\pi} [(2r_T I_m m^2 \cos^2 \varphi + 4r_T I_m - 8m \cos \varphi V_{T0})\beta \\ \quad - (3r_T m I_m \cos \varphi - 8V_{T0})\sqrt{4 - m^2 \cos^2 \varphi}] \end{cases} \quad (3)$$

- Given the FB-CL conduction losses temporarily being neglected, the total conduction losses of the proposed AFC-MMC can be then estimated by adding the P_A and P_B as shown in (4).

$$P_T = \frac{I_m F}{16\pi} [8m \cos \varphi V_{T0} (\alpha - \beta) + 2\pi r_T I_m m^2 \cos^2 \varphi + 4\pi r_T I_m + 16V_{T0} \sqrt{4 - m^2 \cos^2 \varphi}] \quad (4)$$

In the proposed AFC-MMC, the total conduction losses are distributed between thyristors and IGBTs (as well as their anti-parallel diodes). In the majority of operation time, the power is dissipated by thyristors; while the IGBTs only conduct during

the commutation period. To keep the simplicity, a weighted coefficient κ is adopted in (5) to combine these two parts and achieve a total conduction loss evaluation for the AFC-MMC. In (5), P_I and P_D are the IGBT and anti-parallel diode losses calculated using the same method as in (3) for a conventional MMC [20]. In the proper operation of the AFC-MMC, κ is roughly 0.8-0.9 to guarantee the sufficient loss reduction. A case study using the thyristor and IGBT in Table 1 and $\kappa = 0.9$ for the conduction loss comparison under different power factors between the conventional MMC and the proposed converter are shown in Table 2 [8]; and the reduced conduction losses in the AFC-MMC can be observed.

$$P_{con} = \kappa \cdot P_T + (1 - \kappa) \cdot (P_I + P_D) \quad (5)$$

Table 1. Key parameters comparison for thyristor and IGBT at similar switching capacity [9, 10].

Device type	Model	Voltage rating	Current rating	On-state voltage
Thyristor	T1551N48TOH	4.8kV	1.77kA	1.57~1.7V
IGBT	T1800GB45A	4.5kV	1.8kA	3.7V

Table 2. Conduction losses of three-phase AFC-MMC and conventional MMC (dc-link voltage: 600kV; ac side line-to-line RMS:300kV; rated apparent power: 687MVA)

Converter type	Conduction losses		
	P=600MW, Q=0	P=0, Q=600MVar	P=600MW, Q=300MVar (lagging)
AFC-MMC	1.34MW (0.22%)	1.2MW (0.2%)	1.49MW (0.25%)
Conventional HB-MMC	2.69MW (0.45%)	2.34MW (0.39%)	2.84MW (0.47%)

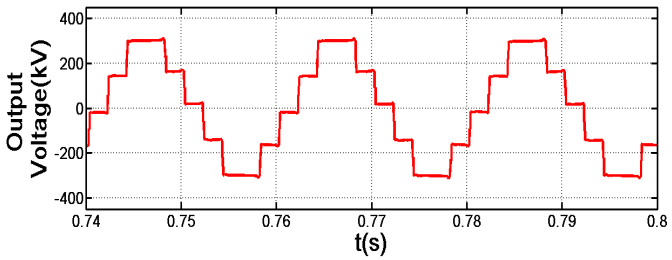
The switching losses of the converter are related to the total switching instances, which is reduced significantly in MMC compared to two-level VSC. The thyristors of AFC-MMC all experience soft switching processes; while the switching losses contributed from the IGBT part is influenced by the operation mode. If the AFC-MMC is operated in staircase mode, similar level of switching losses is expected as in conventional MMC but at the expense of lowering the wave quality. Practically, the selective harmonic optimization is able to achieve a trade-off between the two aspects of switching losses and harmonic distortions for specific requirement [21].

IV. SIMULATION RESULTS

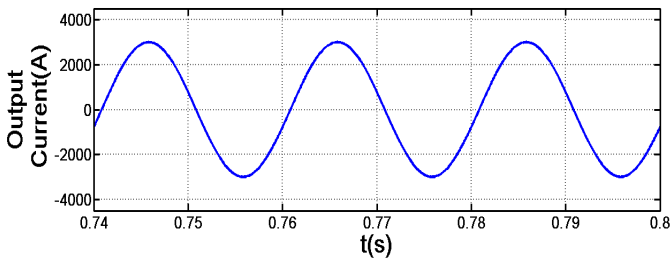
To verify the feasibility of this approach, an illustrative single-phase five-level AFC-MMC in stair-case mode has been simulated with the specifications as follows: dc-link voltage 600kV; AFC cell number per arm: M=4; ac side current: 3kA; modulation index: 0.973 (based on half dc-link voltage); cell capacitance: 0.5mF; arm inductance: 50mH; FB number per cell: N=11; FB-CL capacitance: 5mF. The detailed thyristor

model in Matlab/Simulink is used considering the latching current, recovery time and other parasitic parameters.

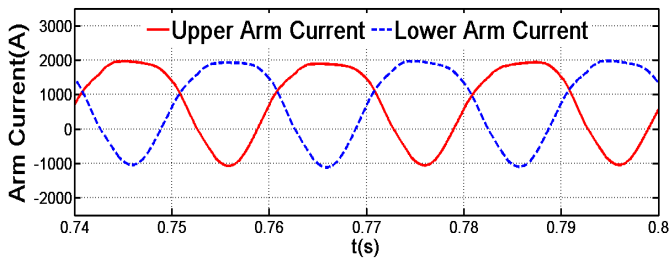
At first, with the power factor set to be 0.99, the resulted key voltage and current waveforms are summarized in Fig. 2. It is observed that the five-level staircase mode voltage waveform is able to be synthesized with the proposed AFC-MMC, and the successful commutation of thyristors can be implemented with output current level reaching 3kA, see Fig. 2(a) and (b). Also, the snapshot of the upper and lower arm currents can be demonstrated by Fig. 2(c), which agrees with the conventional MMC. Fig. 2(d)-(e) represent the capacitor voltage balancing results of the main cell capacitors as well as the auxiliary FB-CL module capacitors by utilizing the redundant switching states of the proposed converter.



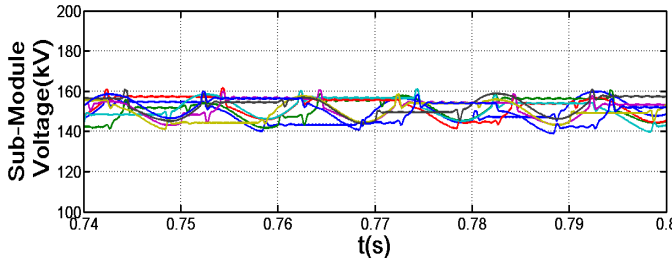
(a)



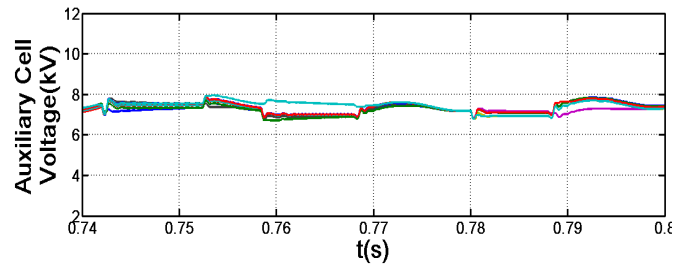
(b)



(c)



(d)

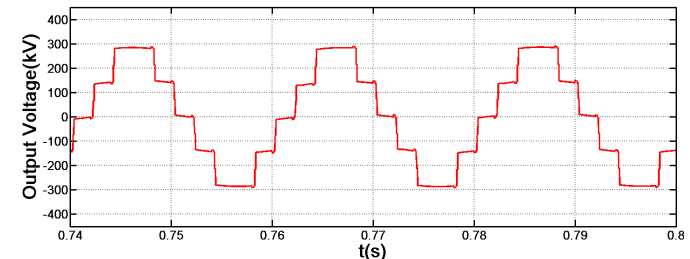


(e)

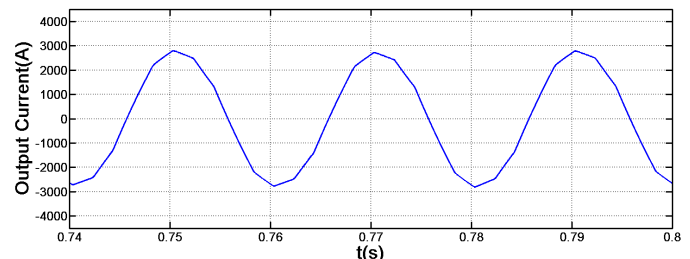
Fig. 2. The simulation results of detailed converter model for AFC-MMC with high power factor: (a) converter output voltage; (b) load current; (c) arm currents; (d) sub-module cell voltages; (e) auxiliary chain-link cell voltages.

Then, to evaluate the reactive power operation capability of the AFC-MMC, the power factor is adjusted to be 0.2 with lagging reactive power. Similarly, the key waveforms of the converter are displayed in Fig. 3, where the five-level staircase mode voltage waveform of the proposed AFC-MMC is shown as in Fig. 3(a), and the ac side current remains about 3kA but with approximate 80° lagging of the terminal voltage, see Fig. 3(b). In this case, the arm current snapshots are included in Fig. 3(c). Due to the low active power level in this operational case, the dc component current flowing in the arm of the AFC-MMC is decreased significantly compared to that in Fig. 2(c). Fig. 2(d)-(e) verify that both the voltages on the main sub-module cell capacitors and the auxiliary FB-CL module capacitors can be balanced with the cell energy balancing algorithms under lower power factor.

With the results presented in both Fig. 2 and Fig. 3, the proposed AFC-MMC has been verified to be able to offer four-quadrant operation capability.



(a)



(b)

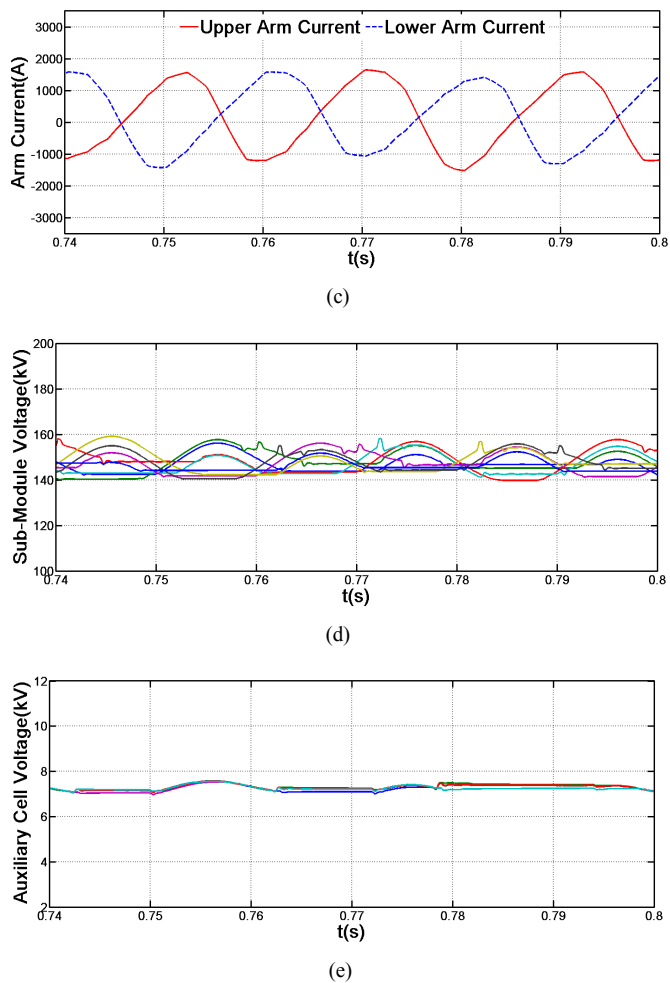


Fig. 3. The simulation results of detailed converter model for AFC-MMC with low power factor: (a) converter output voltage; (b) load current; (c) arm currents; (d) sub-module cell voltages; (e) auxiliary chain-link cell voltages.

In further, Fig. 4 (a) and (b) demonstrate the switching current and voltage waveforms of the thyristor in each cell during its commutation process. It is observed that the thyristor is able to be turned-off through the coordinated operation of the FB-CL, which implies that independent active and reactive power control ability can be achieved as in the conventional VSCs.

In another side, the main thyristors in the proposed AFC cell will experience soft switching processes thanks to the use of the FB-CL for controlled transition. As shown in Fig. 4 (a), the majority of the load current will flow through the low loss thyristors, contributing to an enhanced efficiency performance for the AFC-MMC. However, due to the slow recovery speed of the high capacity phase control thyristors, the wave quality of the converter terminal voltage contains certain amount of low order harmonics, which requires the use of active filtering or the passive tuned filters to meet the grid code.

With the development of the next generation wide bandgap devices such as the silicon-carbide (SiC) technology that offers higher operating temperatures, fast switching on/off capability and low switching/on-state losses, the adoption of high power

fast recovery thyristors is expected to be able to achieve a better compromise on its total semiconductor losses and the output voltage wave quality for the proposed hybrid device based solution. Also, the footprint of the overall converter station can be reduced drastically. Nevertheless, at present, the current capability of commercial SiC thyristors are still not high enough to be applied for high power applications [22].

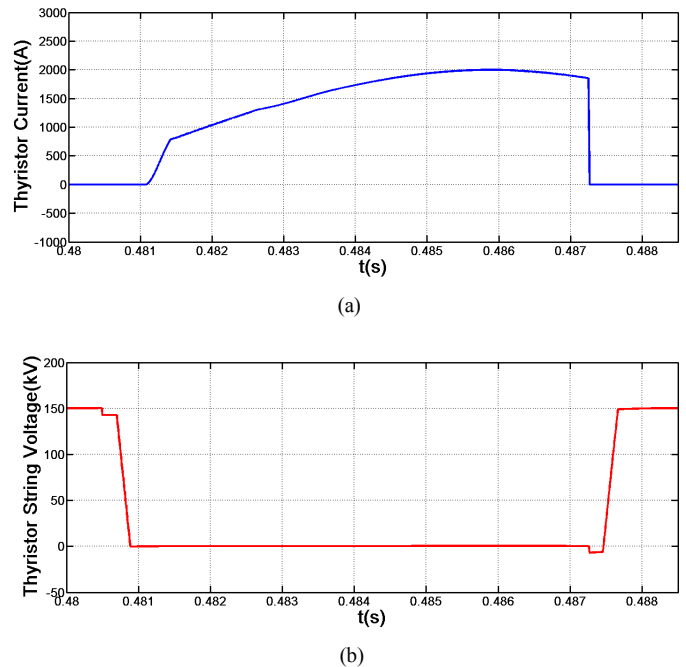


Fig. 4. Zoomed-in version of the thyristor key waveforms: (a) thyristor current waveform during commutation; (b) thyristor voltage during commutation.

V. CONCLUSIONS

In this paper, the active forced commutation (AFC) cell is proposed for modular multilevel converter (MMC) to enhance its power capacity and conversion efficiency by the use of the thyristors for dealing with the main power of the converter. Also, the full-bridge chain-link (FB-CL) with self-commutated devices is employed to operate in short period to implement the forced commutation and transition of the main power switches in each cell.

With the main current carried by the thyristor-bridge and the short period operation of the IGBT part in the AFC cell, reduced conduction losses are obtained due to the lower on-state forward voltage drop of thyristor compared with that in IGBT based MMC.

Compared to the line-commutated-converter LCC, the turn-off of thyristors in the AFC cell can be decoupled from the external power circuit condition thanks to the use of inner auxiliary FB-CL. In this manner, the independent control of active and reactive power in the proposed converter can be implemented, offering the equivalent system level functionally as in a conventional VSC station such as bidirectional power flow without voltage reversal and improved compatibility with weak ac grids.

To conclude, the hybrid use of thyristor and IGBT in the proposed approach combines the advantages of conventional MMC and LCC. It is able to achieve a compromise between the converter efficiency and control flexibility, fulfilling a wide range of practical requirements for high power high efficiency applications.

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