Improved Control Strategy of Full-Bridge Modular Multilevel Converter

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Abstract—This paper describes a control approach that allows the cell capacitors of the full-bridge modular multilevel converter (FB-MMC) to be controlled independent of dc link voltage. Also the control approach offers the possibility of operating the FB-MMC from bi-polar dc link voltages; thus, creating new possibilities for building generic hybrid dc grids with reversible dc link voltage, where conventional line commutated current source converters can operate in conjunction with voltage source converters. Additionally the control approach improves dc fault ride-through of the FB-MMC compared with existing approaches. This is achieved by active control of the arm currents and cell capacitor voltages, and exploitation of the FB-MMC redundant switch states. FB-MMC operation with reversible DC link voltage and decoupled control of the cell capacitor voltages from the dc link voltage are demonstrated using simulations.

Key words—dc fault ride-through capability; dc short circuit proof; High-voltage dc transmission systems; half and full bridge modular multilevel converters; and line commutated converter.

I. INTRODUCTION

The growing demand for low carbon technologies to mitigate the effect of global warming has accelerated the development of renewable power generation that relies increasingly on the use of power electronics. Voltage source converter high-voltage dc (VSC-HVDC) transmission is seen as a key facilitator for the integration of renewable power plants into ac grids. Early generation VSC-HVDC links were built around two-level and neutral-point clamped (NPC) converters. But these converters suffer from high semiconductor losses and expose interfacing transformers to intolerable voltage stresses, *dv/dt*. These stresses are acerbated should the link dc operating voltage be raised to increase their power capacity. Additionally, the use of concentrated dc link capacitors makes VSC-HVDC links vulnerable to dc faults as converter switching devices are exposed to high current stresses due to discharge of the dc link capacitors, and uncontrolled ac in-feed current to the dc side during dc side faults.

Half and full-bridge modular multilevel converters (HB/FB-MMC) have emerged as attractive topologies for high-voltage applications. They offer the following features: scalable to high voltage without the need for series device connection; modular structure with internal fault management (while the system remains operational); and relatively low semiconductor losses[1]. The use of distributed cell capacitors in the HB-MMC improves its dc fault ride capability as the magnitude of the uncontrolled ac in-feed currents that may flow in the converter switches during dc fault are significantly reduced (as cell capacitors do not contribute to the fault current). FB-MMC switching device blocking during a dc fault is sufficient to eliminate any ac grid contribution to the dc fault current. Although this feature is attractive, the FB-MMC has higher semiconductor losses than the HB-MMC (2.35 times according to reference [1]). Although there are several alternative converter topologies offering dc fault short-circuit proof ability with relatively low semiconductor losses, half and full bridge MMCs remain the industry preferred topologies.

Different aspects of the HB and FB-MMCs have been studied. For example, the basic operational principle, modulation and capacitor voltage balancing of the MMC are discussed in [2-6]. The authors in [5, 7, 8] adopted the use of a single reference per phase for both sinusoidal pulse width modulation and staircase modulation with the nearest voltage levels. These references demonstrated the possibility of using output phase currents rather than the arm currents for control and capacitor voltage balancing. However, the use of a single reference increases the number of switching combinations that can be used to maintain cell capacitor voltage balancing, which make generalization of this approach challenging.

The use of two reference signals per phase (one per arm) for controlling the MMC using pulse width (level shifted phase disposition) and staircase modulation is proposed in [9]. This approach is widely used because it makes MMC modulation generalisation simpler than that in [5, 7, 8].

Reference [10] presented fundamental switching frequency modulation and capacitor voltage balancing for the MMC, which is claimed to be suitable for HVDC applications. The approach ensures each switching devices operates at the fundamental frequency, with cell capacitor voltages maintained. It main deficiency is that it increases the energy requirement per cell capacitor several fold compared to pulse width and staircase modulations in order to ensure cell capacitor voltage ripple remains within an acceptable range (233kJ/MVA compared to (30 to 40)kJ/MVA, given [11]).

The use of phase-shifted carriers pulse width modulation (PS-PWM) for the MMC, where each cell is controlled independently, including regulation of the cell capacitor voltages, is discussed in [12, 13]. The approach generates high quality output voltage at a reduced switching frequency per cell, and simplifies overall MMC control as the time consumed for cell capacitor voltage sorting is not needed. However, its main drawbacks are: switching of more than one voltage level is unavoidable, and cell capacitor voltages tend to diverge from

the desired set-point when the system is subjected to minor transients[14-16].

References [13, 17-19] present an improved control strategy which is applicable to HB and FB-MMCs that uses PS-carrier PWM with a number of control loops for the cell capacitor voltages, arm current balancing, circulating current suppression, and individual cell capacitor voltage balancing, to ensure stable system operation, independent of operating conditions. The validity of the control approach in [13, 17-19] was confirmed using simulation and experimentation. However, the increased control reliance in order to maintain cell capacitor voltage balancing may lead to system collapse from any control system malfunction, which is not the case with the traditional approaches. This approach is therefore less likely to be adopted in HVDC applications.

Reference [20] presented comprehensive review of HB and FB-MMCs, including their open and closed loop control strategies. Some control strategies highlighted are traditional control of the modular multilevel converter that estimate the modulating signals of the upper and lower arms based on the output phase current loop as for the two-level voltage source converter, with feed forward terms for disturbance rejection as shown in [21]. Although this approach is stable and popular, as stated in [20], it suffers from relatively slow dynamic response compared to those with regulated arm currents as in [22-32]. Most of the approaches that regulate arm currents use some form of average cell capacitor voltage regulation, originally suggested by Akagi and others in [13, 17-19, 25]. However, increased reliance of these methods on the use of control within the modulator or in the main control path may raise several concerns regarding their robustness during ac and dc network faults, and malfunction of control systems.

This paper presents a control approach that uses the unexploited possibilities within the FB-MMC power circuit to decouple its cell capacitor voltage regulation from the dc link voltage; thus, realizing operation with variable and bi-polar DC link voltage. The viability of the presented control scheme is demonstrated in an illustrative HVDC station based FB-MMC, with positive and negative dc link voltage operation. A detailed discussion is presented of the different FB-MMC operating modes and their potential uses in HVDC transmission systems. Aspects related to dc fault survival can found in [33].

II. MODULATION AND CONTROL OF THE FULL-BRIDGE MODULAR MULTILEVEL CONVERTER

Figure 1 shows a three-phase modular multilevel converter with N full-bridge cells per arm. Cell capacitors and switching devices of each cell must be able to block V_{dc}/N during normal operation. Therefore, each arm must block the full dc link voltage V_{dc}. Unlike the unipolar cells of the half-bridge MMC, each bipolar cell of the full-bridge MMC can generate three voltage levels $\pm V_{dc}/N$ and 0. This allows the FB-MMC cell capacitors to be inserted as additive or subtractive polarities (added or subtracted from the dc link voltage V_{dc}) to generate different voltage levels at the converter output poles '*a*', '*b*' and '*c*' relative to the supply artificial mid-point. Figure 2 illustrates the pulse width modulation strategy use in this paper for controlling the full-bridge MMC, assuming a fixed modulation index (M) and adjustable dc offset (m_d), where the upper and lower arm modulation functions of phase '*a*' are described as $v_{a1}=½V_{dc}(m_d+m_a)$ and $v_{a2}=½V_{dc}(m_d-m_a)$, and $m_a=M\sin\omega t$ and $-1\leq m_d\leq 1$. During normal operation, the FB-MMC dc link voltage is regulated around the rated voltage, so $0\leq v_{a1}/V_{dc}\leq 1$ and $0\leq v_{a2}/V_{dc}\leq 1$ as $m_d\approx 1$. In this operating mode, the FB-MMC operates in the buck mode; thus, voltage levels at the converter output poles (a, b and c) are generated by insertion of the FB cell capacitors with opposing polarities to that of the dc link voltage (only subtractive states are utilized). In this mode, cell capacitor insertion with the same polarity as the dc link (additive states) is allowed only during the intermediate voltage levels to accelerate cell capacitor voltage balancing. When the dc link voltage is reduced below the peak of the line-to-line voltage, the FB-MMC must be operated in a boost mode in order to retain full control over active and reactive power exchange with the ac grid. In this mode, insertion of the FB cell capacitors with the same polarity as the dc link voltage (additive states) can be utilized to allow these cell capacitors of each converter arm appear as virtual dc links, provided the sum of the cell capacitor voltages of each arm is regulated around the rated dc operating voltage (even when the dc link is suppressed to zero as during a pole-to-pole dc short-circuit fault). With the modulation strategy depicted in Figure 2, the full-bridge MMC can exchange both active and reactive powers with the ac grid in buck and boost modes. But when the dc link voltage is suppressed to zero, any injection of active power into the grid leads to cell capacitor discharge; therefore, the active power command must be reduced to zero (allowing the full-bridge MMC to operate as a double-star static synchronous compensator). As the dc link voltage reduces, the modulation function dc component m_d must be decreased proportionally. This allows normalized versions of the modulation functions of the upper and lower arms to cross the time axis into a negative region. The proportion of the modulating function crosses into the negative region represents the number of cell capacitors with reverse polarities to be added to dc link voltage. For practical considerations related to the type of dc cable being used with voltage source converter based HVDC links, the usable range of m_d at present is limited to $0\leq m_d\leq 1$. However, $-1\leq m_d\leq 0$ represents a new operating region, where the FB-MMC operates normally with reversed dc link voltage polarity, while the voltage stresses across its cell capacitors and switching devices are fully controlled. This new operating region is expected to create possibility for hybrid dc grids, where line commutating current source converters (LCC) and voltage source converters based on the FB-MMC can operate harmoniously. Figure 2 shows the main per phase control loop that adjusts m_d, and regulates cell capacitor voltages of the

upper and lower arms and the common-mode current i_d. This control loop has an important function during a dc side fault, as it restraints the fault current magnitude each converter arm experiences as demonstrated in [33].

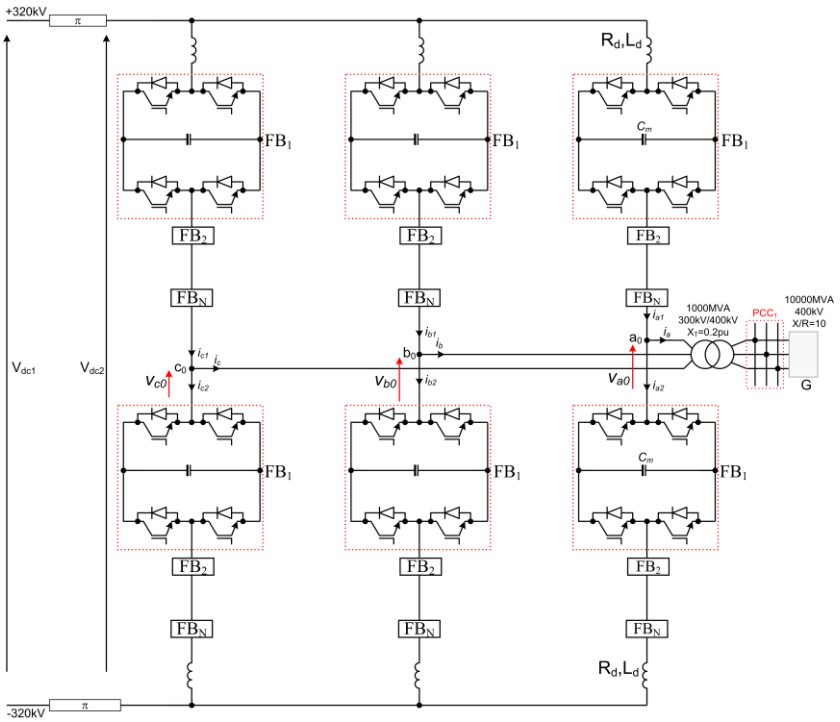


Figure 1: H-bridge MMC based HVDC converter station (Number of cells per arm $N=21$, cell capacitance C_m=1mF, and arm inductance L_d=50mH).

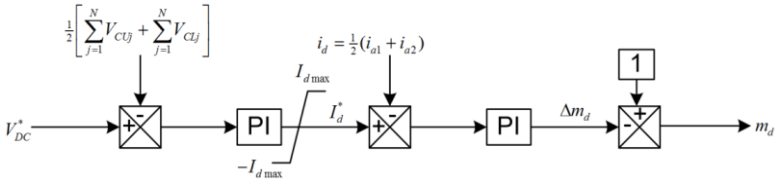


Figure 2: Per phase control for m_d adjustment.

III. SIMULATIONS

To substantiate the discussion presented in section II regarding manipulation of the modulation function dc component (m_d) and its suitability for typical HVDC converters, this section presents simulation results from a 21-cell FB-MMC with parameters listed in Figure 1. In this example, the FB-MMC is modelled by electromagnetic transient simulation, and controlled as illustrated in Figure 2 is used. More modelling and control system details can be found in references [21, 33].

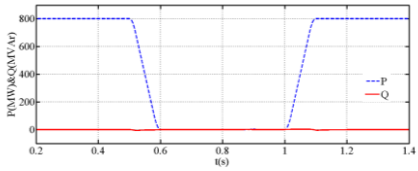
A) DC link voltage reversal

As stated, adjustment of the modulation index dc component (m_d) and full exploitation of the FB-MMC redundant switch states offer new features for modern VSC-HVDC links. To demonstrate of some of these features, the converter station in Figure 1 is fed from a controlled voltage source with an initial dc link voltage of 640kV. At time t=0.6s, the dc link voltage is reversed -640kV, with a slope of 4pu/s (based on a dc link voltage of 640kV). The reference active power is 800MW at unity power factor, and reduced to zero during the dc link voltage reversal, and then restored to 800MW, and the results are displayed in Figure 3. Figure 3 (a) shows the active and reactive power the converter station exchanges with the ac grid over the simulation period. Figure 3 (b) shows the converter station output currents measured at the PCC, zoomed around dc link voltage reversal event and active power restoration. Figure 3(c) shows the upper and lower arm currents for phase 'a' are regulated during operation with positive and negative dc link voltages, with limited transients in the regions when the dc link voltage is near zero. Figure 3 (d) shows a pre-filter phase voltage (v_{a0}) FB-MMC presents to the low-voltage side of the interfacing transformer. The cell capacitor voltages in Figure 3(e) shows that the cell capacitor voltages are regulated around 640kV/21≈30.47kV, independent of the dc link voltage polarity. The plots for the voltages developed across the upper and lower arms displayed in Figure 3 (f) and its snapshot in Figure 3 (g)

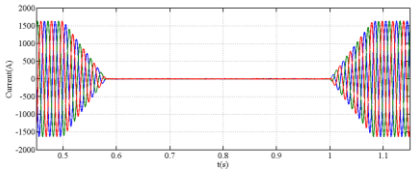
show that the dc components of the upper and lower arm voltages follow that of the modulation functions, which are adjusted by the proposed control scheme as previously claimed. Figure 3 (i) presents the dc link voltage (V_{dc1}) measured at the terminal of converter station VSC_1 in Figure 1. The results in Figure 3 show that the FB-MMC being studied remains controllable, whether its input dc link voltage is positive or negative, including when much lower than the peak of the ac grid voltage (this means the peak fundamental voltage the FB-MMC can generator is no longer coupled to the dc link voltage as in the HB-MMC and conventional VSCs).

B) Decoupling of cell capacitor voltages from converter DC link voltage

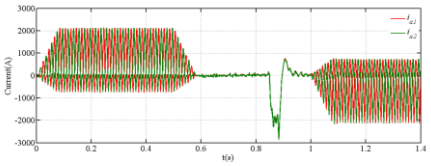
Figure 4 shows waveforms that illustrate the usefulness of m_d manipulation for decoupling FB-MMC cell capacitor voltage regulation from the converter dc link voltage. In this illustration, the FB-MMC dc link voltage in Figure 1 is maintained at 640kV and its cell capacitor voltages are initially regulated at 30.48kV, and at t=0.6s, the cell capacitor reference voltage is increased by 10% (33.52kV). In an attempt to minimize any transients from energy level change of these cell capacitors, the active power the converter station exchanges with the ac grid is temporary reduced from 800MW to 400MW at t=0.5s, and then restored to 800MW at t=0.8s, see Figure 4 (a). The inverter output phase current waveforms at the PCC in Figure 4 (b) show no undesirable transients during the cell capacitor voltage set-point change. Figure 4 (c) shows the upper and lower arm currents exhibit limited transients as the cell capacitor reference voltage is increased from 30.48kV to 33.52kV (this means the total voltage across each converter arm is increased from 640kV to 704kV). Figure 4 (d) shows that the cell capacitor voltages of the FB-MMC follow their reference voltage and are regulated over the entire simulation period. The measured input dc voltage (V_{dc1}) is independent of the cell capacitor voltages, and the dc link current magnitude remains determined by the active power the converter exchanges with the ac grid and input dc link voltage, see Figure 4 (e) and (f). However, the dc link current shows a transient when the reference cell capacitor voltage is increased, and returns to its expected settling point. The results presented in Figure 3 and Figure 4 show that the proposed control scheme is able to decoupling cell capacitor voltage regulation from converter dc link voltage, including during dc link voltage reversal.



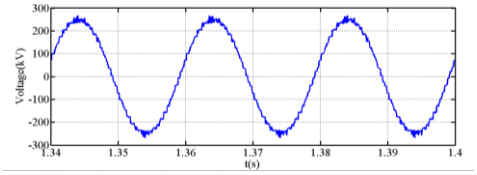
(a) Active and reactive power the converter station exchanges with the AC grid at the PCC, with unity power factor



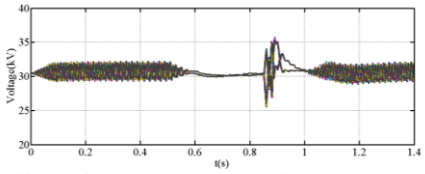
(b) Current waveforms the converter station injects into the AC grid at the PCC



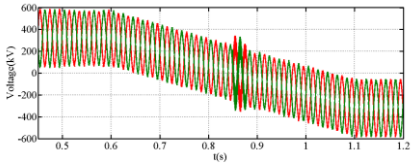
(c) Upper and lower arm currents (phase *a*)



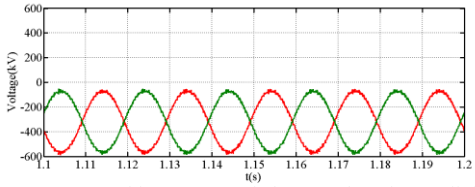
(d) Pre-filter phase voltage the converter presents to the interfacing transformer low-voltage side



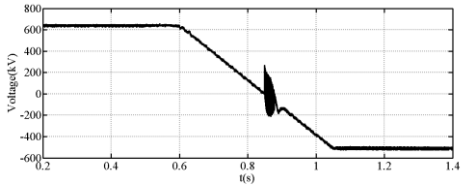
(e) Cell capacitor voltages (upper and lower arms of phase *a*)



(f) Phase *a* voltage waveforms across upper and lower arms during DC link voltage reversal

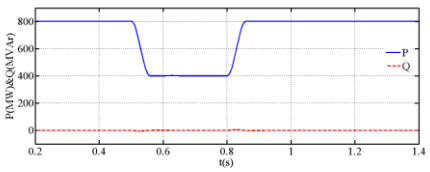


(g) Voltages across upper and lower arms of phase *a* when the DC link voltage is reversed to -640kV

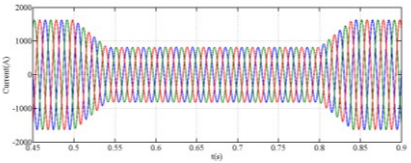


(h) DC voltage at the terminal of the H-bridge MMC (V_{dc2})

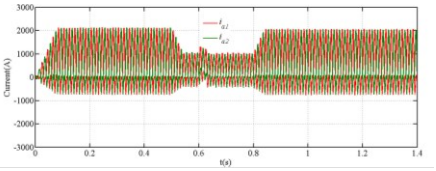
Figure 3: Waveforms illustrates closed loop performance of a H-bridge MMC during DC link voltage reversal.



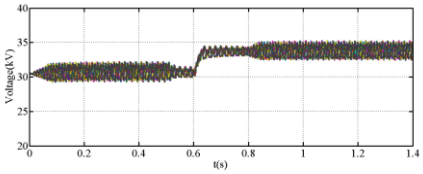
(a) Active and reactive power the converter station exchanges with theAC grid



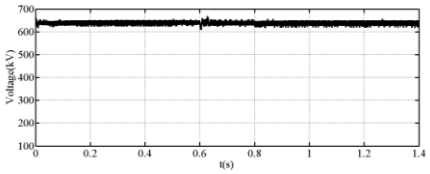
(b) Current waveforms the converter injects into the AC grid at PCC_1



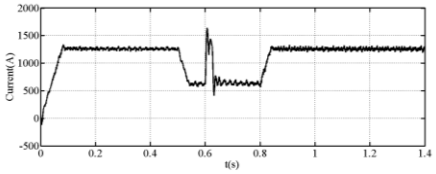
(c) Upper and lower arm currents (phase *a*)



(d) Voltage across cell capacitors of the upper and lower arms of phase *a*



(e) DC link voltage measured at the terminal of the converter station (V_{dc2})



(f) DC link current

Figure 4: Waveforms when cell capacitor voltage balancing of the H-bridge MMC HVDC converter is decoupled from the DC link voltage and AC grid voltage.

IV. Conclusions

This paper explored new operating regions of the FB-MMC that can be exploited to enable HVDC transmission links to ride through DC faults with and without converter blocking, with controlled recharge of the DC link cables after a DC fault is cleared. Also, FB-MMC operation with a variable DC link voltage ranging from V_{dc} to $-V_{dc}$, was demonstrated. The usefulness of the new operating regions was validated by simulations, where the generic nature of the proposed control scheme for a HVDC converter station, was highlighted using a FB-MMC with 21 cells per arm, with staircase modulation.

V. References

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