AC Voltage Sag-Swell Compensator based on Unified Non-Inverting and Inverting Output Voltage AC Chopper

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Abstract

This paper proposes a unified AC chopper topology that can generate both non-inverting and inverting AC voltages. It is therefore suitable for compensating utility voltage sag-swell in domestic consumer and industry infeeds. The proposed converter is able to save on the passive device footprint and improve dynamic performance compared to other similar candidates. The topology derivation, operating principle and performance evaluation are analysed in this paper. Simulation results are presented to assess the proposed scheme with in-phase and out-phase AC voltages generated from a fixed grid input to compensate the voltage sag-swell disturbances in the utility.

1 Introduction

With developments in the power industry, the increasing diversity and unbalanced disturbances of the load conditions necessitate the use of local voltage stabilisers, called dynamic voltage restorers (DVR), at the critical grid buses to ensure reliable power supply [1, 2].

A DVR is a type of series-connected flexible AC transmission system (FACTS) device mainly used at distribution level to compensate voltage quality problems including voltage amplitude sag-swell, voltage flicker, unbalanced voltage disturbances, etc. The DC-AC conversion based DVR device can functionally meet all of these requirements, and can also deal with harmonic distortion as long as the switching frequency is sufficiently high. However, this kind of device is usually expensive and heavy due to the DC energy source and DC-link capacitors. The DC-link energy storage component, consisting of electrolytic capacitors, also suffers from short service life due to the frequent charging and discharging processes. These cost and reliability issues are now the main constraints for DC-AC prototype FACTS devices [3, 4].

Motivated by cost-effective designs for DVR solutions, small-footprint AC choppers are of interest to be employed as voltage amplitude controllers, although they are not suitable for voltage harmonic compensation. Compared to the conventional DC-AC scheme, this approach can avoid the bulky DC-link stage and can be easily coupled with the main grid via either auto-transformers or isolated transformers. However, the normal buck or boost type AC chopper can only compensate the voltage in a fixed direction, meaning that either voltage sag or swell can be managed but not both unless complex winding structures are used in the transformers [5, 6].

The Z-source direct AC-AC converter [7] offers bipolar voltage generation ability by means of the additional impedance network. However, in this configuration, there is discontinuity in its output voltage gain curve, and the input and output terminals are floating with respect to each other. A variety of quasi-Z-source based AC-AC converters have been presented with common ground between the input and output [8, 9]. However, they still suffer from sharply changing output voltage gain around a certain operation point, which is challenging for the adaptive adjustment of the controller.

The bipolar AC chopper with inner voltage boosting cell and smooth bidirectional output voltage gain curve has been presented, as shown in Figure 1 [10]. It is also able to maintain a common ground for input and output ports. However, the extra passive devices in the voltage boosting cell are still necessary to achieve bipolar voltage gain, which causes a large footprint (low power density), high voltage stress on semiconductor devices, slow dynamic response and complex control design.

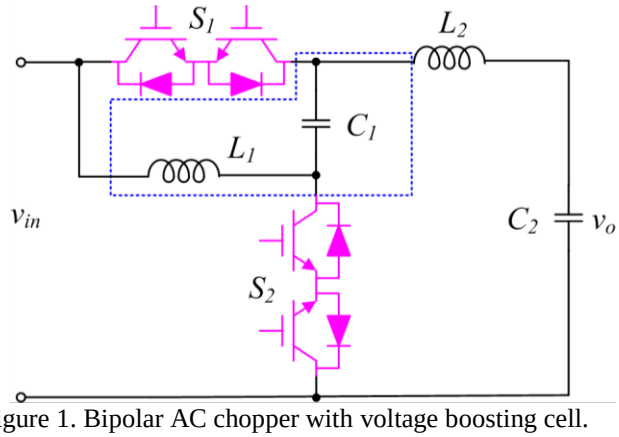

Figure 1. Bipolar AC chopper with voltage boosting cell.

In an attempt to optimise this aspect whilst maintaining other advantages, this paper proposes a unified non-inverting and inverting AC chopper (UNI-AC) topology with bipolar voltage gain, reduced power switch voltage stress, and small footprint. It employs more silicon devices but saves on the passive components, reducing the order of the converter

model. The operating principle and performance analysis of the proposed converter are described in this paper.

2 Operational Principle of the UNI-AC

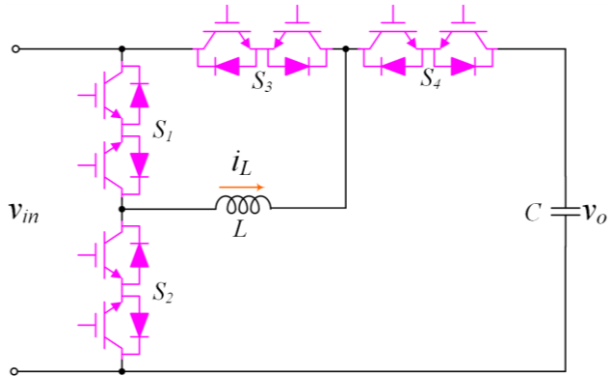

Figure 2. The unified non-inverting and inverting AC chopper (UNI-AC).

The schematic of the proposed UNI-AC is shown in Figure 2, where four bidirectional power switches using back-to-back insulated gate bipolar transistors (IGBTs) are employed, and an inner inductor L and output capacitor C are used as energy storage elements to extend the voltage output range. A solid connection between the input and output reference terminals is facilitated in the UNI-AC. The active switches S_1 and S_2 (S_3 and S_4) are not allowed to conduct simultaneously to avoid short-circuit in the proposed converter. To regulate the output voltage, the switch combination of {S_1, S_4} and {S_2, S_3} are modulated in a complementary manner, allowing the periodic charging and discharging of L and C.

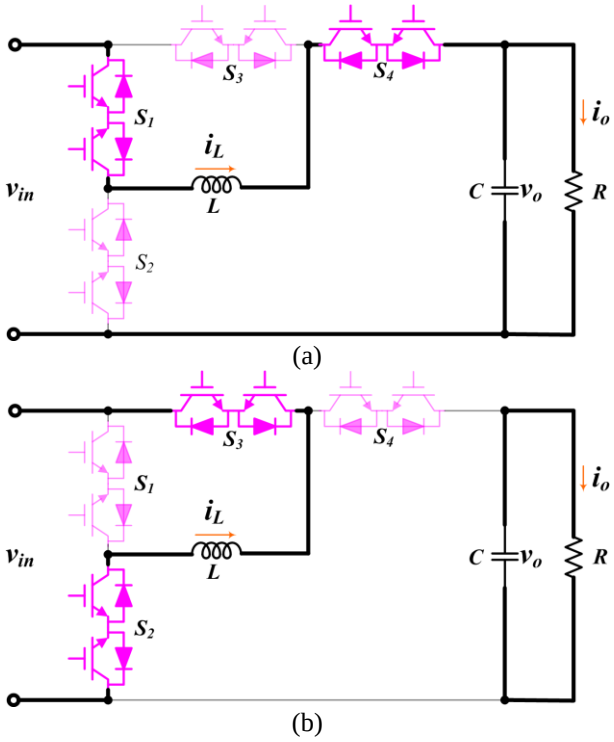

Figure 3. UNI-AC operating modes: (a) stage 1, (b) stage 2.

As shown in Figure 3, the operating principle of the UNI-AC is summarised in two stages:

Stage 1: according to Figure 3(a), when S_1 and S_4 are on and S_2 and S_3 are off, output voltage is generated from the input. The inner inductor L is discharged to supply energy to the output.

Stage 2: according to Figure 3(b), when S_1 and S_4 are off while S_2 and S_3 are on, L can be charged by the input and the stored energy is prepared for the subsequent Stage 1.

If the switching frequency is sufficiently high compared to the AC voltage fundamental frequency, the state variables can be viewed as constant during each switching cycle. Assuming that d is the duty cycle of {S_1, S_4}, i_o and i_L are the load current and inner inductance current, and that v_{in} and v_o represent the input and output voltages respectively, the principles of volt-second and ampere-second balance in the UNI-AC can be expressed by (1). After algebraic manipulation of the first equation in (1), the voltage transfer ratio M of the proposed converter is expressed as (2).

$$\begin{cases} d(v_{in}-v_o)-(1-d)v_{in}\approx 0 \\ d\cdot(i_L-i_o)-(1-d)i_o\approx 0 \end{cases} \quad (1)$$

$$M=\frac{v_o}{v_{in}}=2-\frac{1}{d} \quad (2)$$

Figure 4 shows the plot of M versus d for the proposed UNI-AC, where a bidirectional voltage output is achieved when the duty cycle varies around 0.5. This means the UNI-AC is able to generate AC voltage both in-phase and out-phase with the input voltage. Therefore, both voltage sag and swell can be compensated adaptively when the proposed converter is applied as a DVR in the utility.

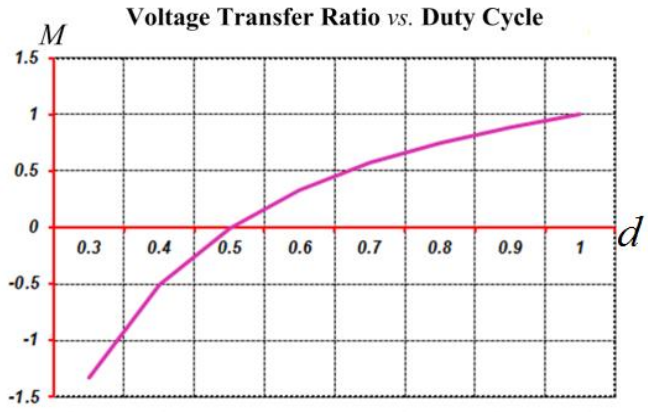

Figure 4. UNI-AC voltage transfer ratio varying with duty cycle.

The UNI-AC topology is expected to have a reduced footprint (higher power density) and a more compact design than the solution in [10].

3 Performance Analysis

In this section, the parameter selection and design guidelines of the UNI-AC are analysed and described.

Based on Figure 3, the blocking voltages of S_1 and S_2 in the UNI-AC are both equal to the input voltage v_{in}, whilst the sustained voltage applied across S_3 and S_4 is the difference between v_{in} and v_o. According to (1), the output capacitor voltage v_o can be calculated from (3) and, thus, the voltage stress on S_3 and S_4 is expressed in (4). It is found that the extended output voltage range is maintained and that lower voltage stresses for the power switches are achieved compared to those in [8-10], especially when the duty cycle is small to generate out-phase voltage. Despite the proposed UNI-AC having twice the number of switches, this does not increase the total semiconductor device cost, due to the reduced voltage stress per device.

$$v_o = v_{in} \cdot (2 - 1/d) \tag{3}$$

$$v_{sw} = v_{in} \cdot (1/d - 1) \tag{4}$$

Using the second equation in (1), the relationship between the current state variables can be approximately expressed in (5). Then, the current flowing through all of the UNI-AC power switches is equal to the inductor current as in (6).

$$i_L = i_o / d \tag{5}$$

$$i_{sw} = i_L = i_o / d \tag{6}$$

The output capacitor C can be designed as a filter considering the voltage ripple demand and the reactive power rating, etc., which are expressed in (7), where f_0 is the fundamental frequency and f_{sw} is the switching frequency. Based on these constraints, the value of C can be chosen to achieve optimised performance. In Figure 2, the inductor L acts as an energy buffer to link the input source and output capacitor C. Also, it determines the current ripple flowing through the power switches. A large inductance can reduce the output voltage range due to the inductive voltage drop, but is able to limit the magnitude of high-frequency current ripple. This indicates that the value of L should be selected based on the trade-off between current ripple and the total reactive power rating of the inductor as in (8) [11]. It is noticed that the real voltage and current stresses used for selecting the power switches are estimated by the summation of the average component and the maximum ripple value.

$$\begin{cases} \Delta v_o = \dfrac{i_o \cdot (1-d)}{f_{sw} \cdot C} \\ Q_c = 2\pi \cdot f_o \cdot C \cdot v_o^2 \end{cases} \tag{7}$$

$$\begin{cases} \Delta i_L = \dfrac{v_{in}(1-d)}{f_{sw} \cdot L} \\ Q_L = 2\pi \cdot f_o \cdot L \cdot i_L^2 \end{cases} \tag{8}$$

4 Simulation Results

The performance of the proposed UNI-AC in Figure 2 has been assessed by simulation with the following specifications: input AC voltage v_{in}=240V (RMS), L=0.75mH, C=63μF, switching frequency f_{sw}=10kHz and load resistance R_L=12Ω.

In practise, the duty cycle variation range of the UNI-AC can be selected to 0.3-1. This can ensure a voltage output range of -1pu to 1pu of the input voltage. According to (3) and (6), the voltage and current stresses on the switches, as well as the ripple voltage and current superimposed on the state variables, increase as duty cycle is decreased. Hence, the waveforms for the state variables v_o and i_L together with the voltage and current stresses on the power switches are displayed in Figure 5 when duty cycle is set to be 0.3. It is observed that the voltage stresses for switches S_1 and S_2 are equal to the input voltage, whilst S_3 and S_4 experience approximately twice the input voltage as in (4). Hence, the voltage stresses of the proposed UNI-AC are reduced compared to the schemes in [8-10], where the voltage stresses on power switches can reach more than three times the input voltage if duty cycle d=0.3.

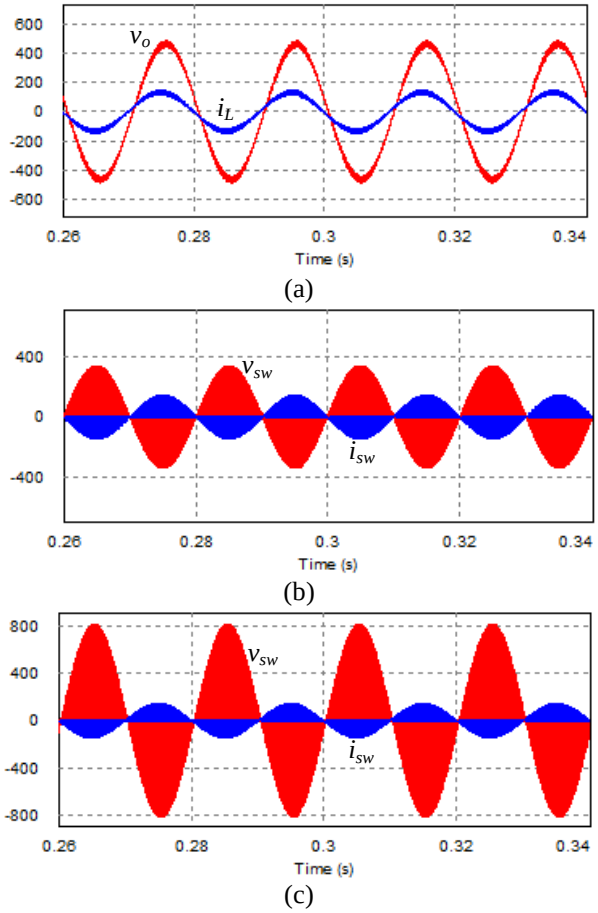

Figure 5. The key waveforms of the UNI-AC when d=0.3
(a) the state variables on output capacitor and inner inductor
(b) the voltage and current waveforms for switches S_1 and S_2
(c) the voltage and current waveforms for switches S_3 and S_4;.

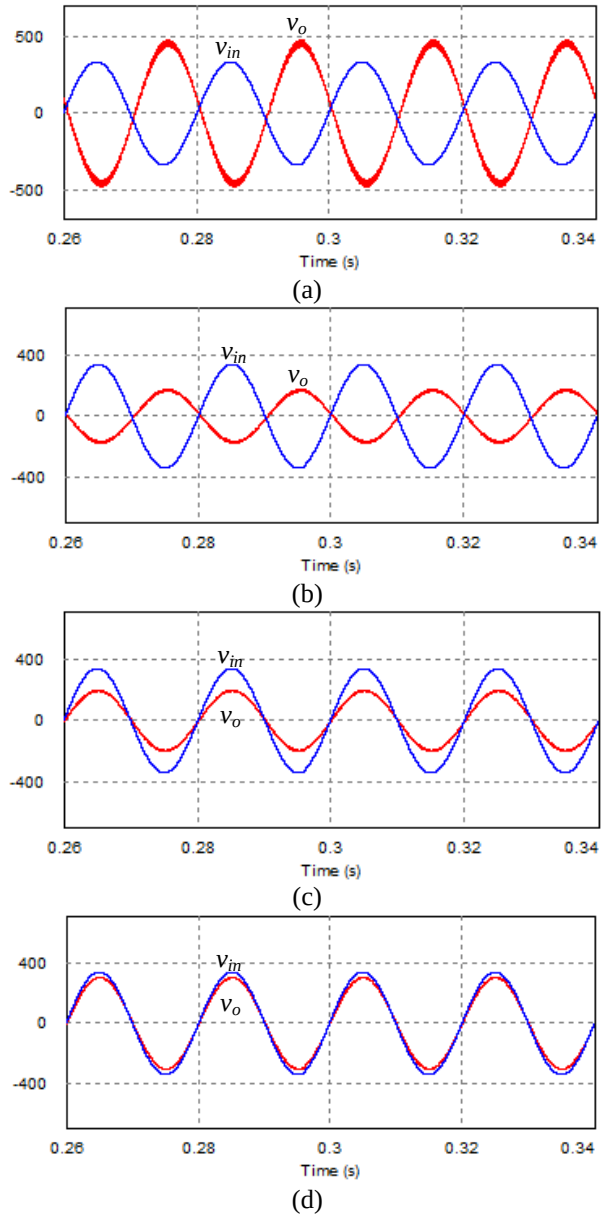

Figure 6. UNI-AC voltage output variation with duty cycle (a) d=0.3 (b) d=0.4 (c) d=0.7 (d) d=0.9.

From Figure 6, it is concluded that the output voltage can be both in-phase and out-phase relative to the input voltage, according to duty cycle variation. In Figure 6(a), when the duty cycle d=0.3, the output voltage of the UNI-AC has approximately 180° phase-shift relative to the input voltage. If duty cycle increases to 0.4, the output reverse direction AC voltage will decrease as in Figure 6(b). Duty cycle d=0.5 is theoretically the boundary between positive and negative voltage generation, hence with the duty cycle d increasing to 0.7, the output voltage becomes in-phase with v_{in}, as shown in Figure 6(c). The continuous increase of d can push the output voltage close to v_{in} as shown by Figure 6(d).

The results of Figure 6 verify that the UNI-AC shown in Figure 2 can act as a utility voltage sag-swell compensator based on direct AC-AC conversion, which is low-cost and compact.

5 Conclusion

This paper describes the application of a unified non-inverting and inverting AC chopper as a DVR. This kind of converter is capable of generating bidirectional AC voltage, both in-phase and out-phase with the input voltage. This feature facilitates the use of the DVR to be a cost-effective solution to stabilise the voltage in a critical grid bus, overcoming the challenge of voltage sag-swell. Compared with a DC-AC configuration, this scheme saves on DC energy supply and storage requirements, making it compact and economical.

Acknowledgements

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