

ALUMINIUM OXIDE PREPARED BY ATOMIC LAYER DEPOSITION IN ORGANIC THIN-FILM TRANSISTORS OPERATING AT 2 V: COMPARISON WITH UV-OZONE OXIDATION

Stuart Hannah and Helena Gleskova

Department of Electronic and Electrical Engineering, University of Strathclyde, Glasgow, United Kingdom (stuart.hannah.2013@uni.strath.ac.uk)

INTRODUCTION

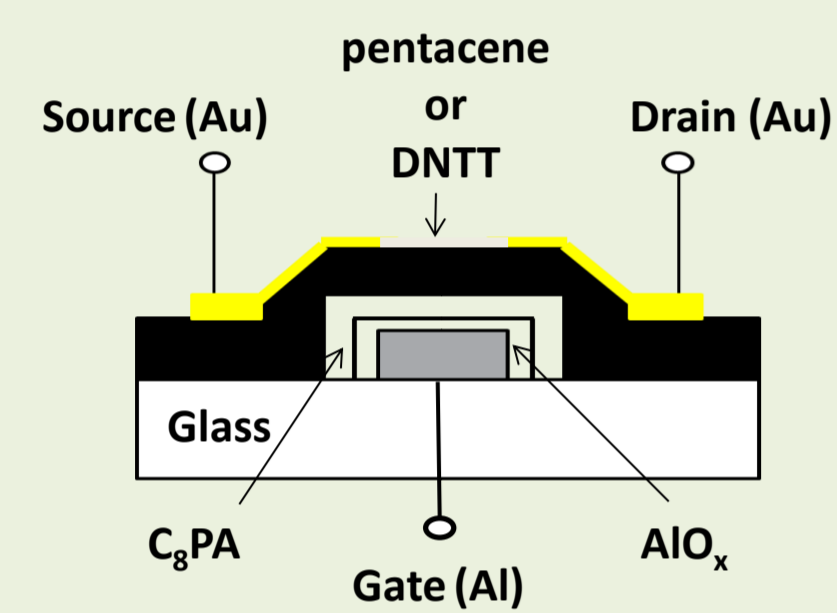
Large-area, roll-to-roll fabrication of thin-film circuits demands layer thickness uniformity over large areas. Previously, a 10-nm-thick dry bi-layer dielectric based on aluminium oxide (AlO_x) prepared by UV-ozone oxidation and n-octylphosphonic acid (C_8PA) monolayer prepared by vacuum evaporation has been developed for organic thin-film transistors (OTFTs) based on pentacene. Here we compare such OTFTs to similar transistors that incorporate ALD- $\text{AlO}_x/\text{C}_8\text{PA}$ bi-layer. In addition, a 12.9-nm-thick ALD- AlO_x exposed to UV-ozone for 60 minutes was incorporated into OTFTs based on dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT).

AIMS

- Use atomic layer deposition (ALD) to grow thin layers of AlO_x for low-voltage OTFTs.
- Compare Al/ALD- $\text{AlO}_x/\text{C}_8\text{PA}$ /pentacene/Au and Al/UV-ozone- $\text{AlO}_x/\text{C}_8\text{PA}$ /pentacene/Au transistors and metal-insulator-metal (MIM) structures.
- Fabricate Al/ALD- AlO_x /DNTT/Au and Al/ALD- $\text{AlO}_x/\text{C}_8\text{PA}$ /DNTT/Au OTFTs and compare them with pentacene OTFTs.

EXPERIMENT

- Two devices incorporated thin ALD- AlO_x (12.9 nm) and two used thicker (36.8 nm) ALD- AlO_x . ALD performed from H_2O and TMA at 160°C .
- Within each pairing, one sample underwent a 2-minute UV-ozone clean prior to C_8PA assembly and/or pentacene evaporation. All other transistor layers were identical to UV-ozone- AlO_x (9 nm) OTFTs. $W = 1000 \mu\text{m}$ and $L = 30, 50, 70$ and $90 \mu\text{m}$.
- In the DNTT OTFTs the ALD- AlO_x (12.9 nm) layer was exposed to UV-ozone for 60 minutes prior to C_8PA self-assembly. Source/drain and gate contacts are similar to pentacene transistors.



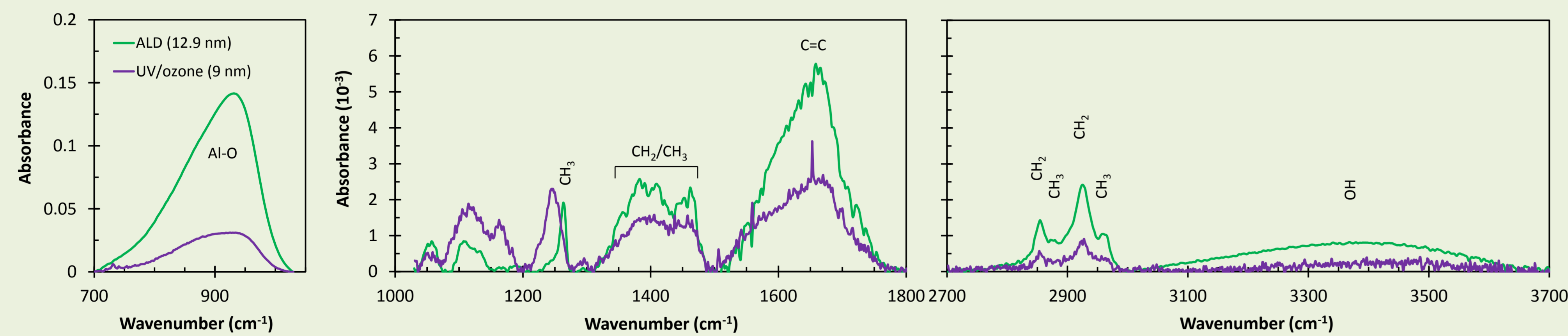
Linear regime ($|V_{DS}| < |V_{GS} - V_t|$):

$$I_D = \mu C \frac{W}{L} (V_{GS} - V_t) V_{DS} \quad \mu_{lin} = \frac{\partial I_D}{\partial V_{GS}} \cdot \frac{1}{C V_{DS}} \frac{W}{L}$$

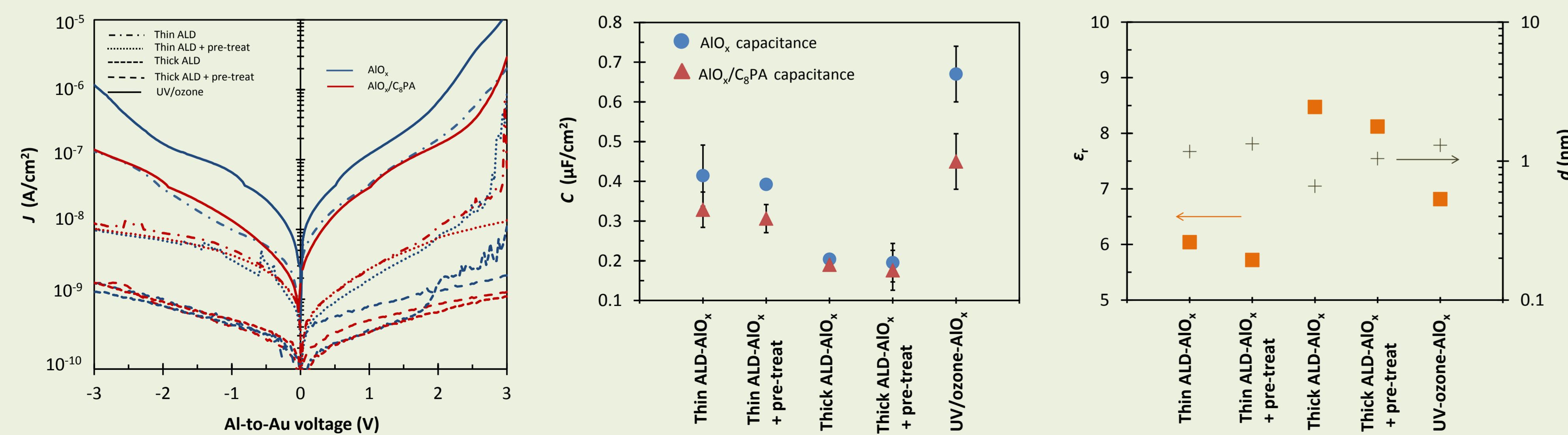
Saturation regime ($|V_{DS}| > |V_{GS} - V_t|$):

$$I_D = \mu C \frac{W}{2L} (V_{GS} - V_t)^2 \quad \mu_{sat} = \left(\frac{\partial \sqrt{I_D}}{\partial V_{GS}} \right)^2 \cdot \frac{1}{C} \frac{W}{2L}$$

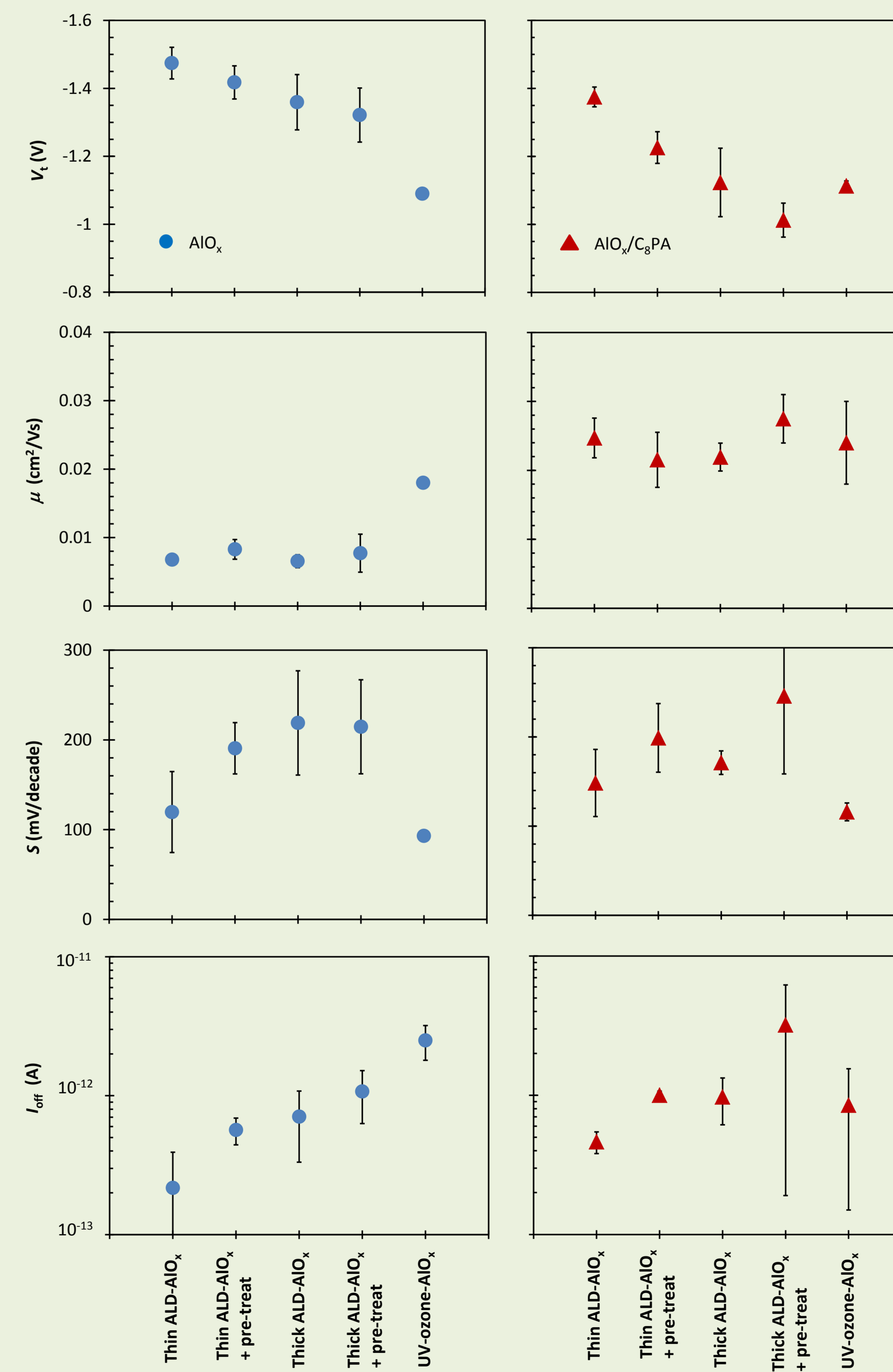
FTIR



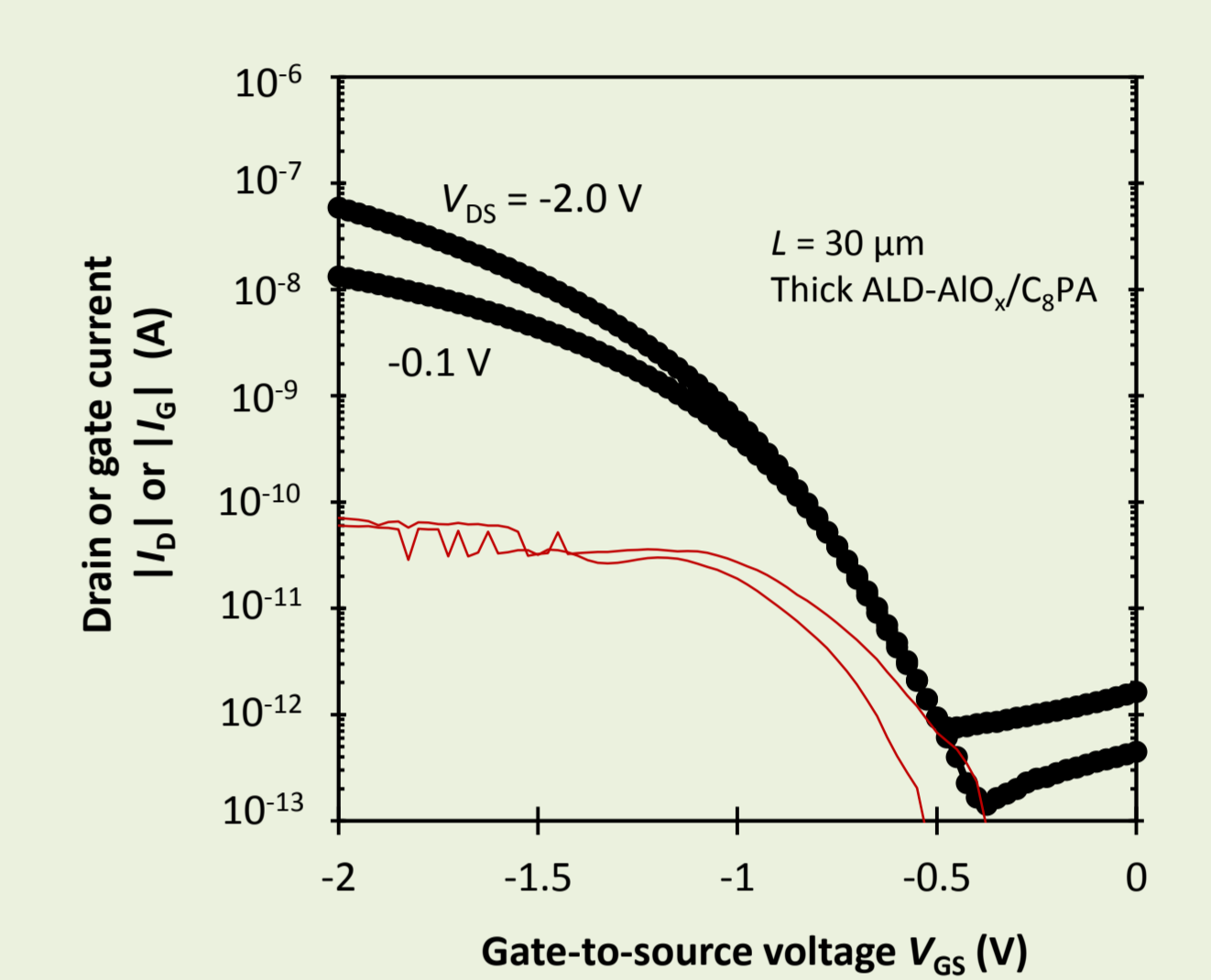
RESULTS: MIM STRUCTURES



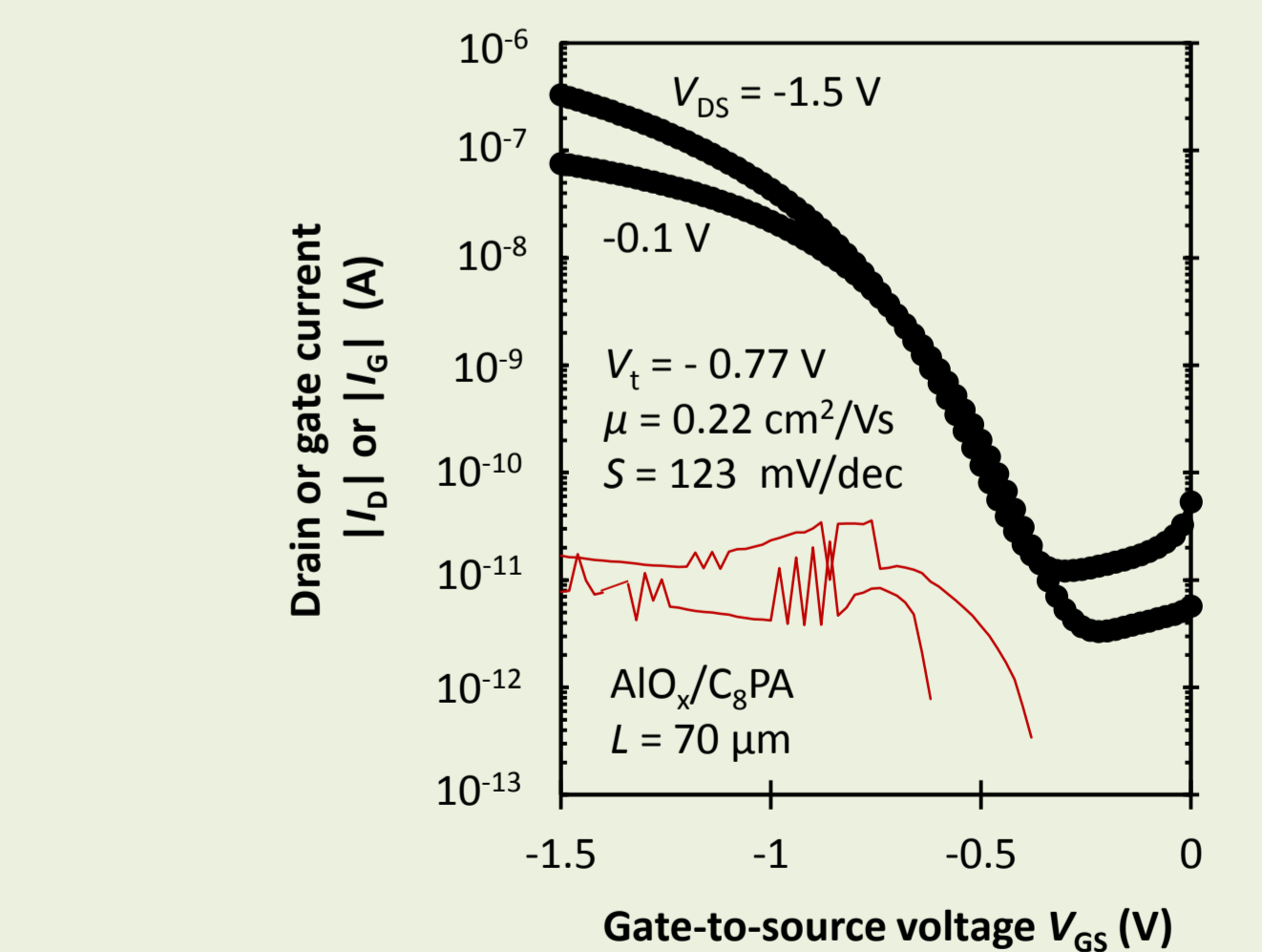
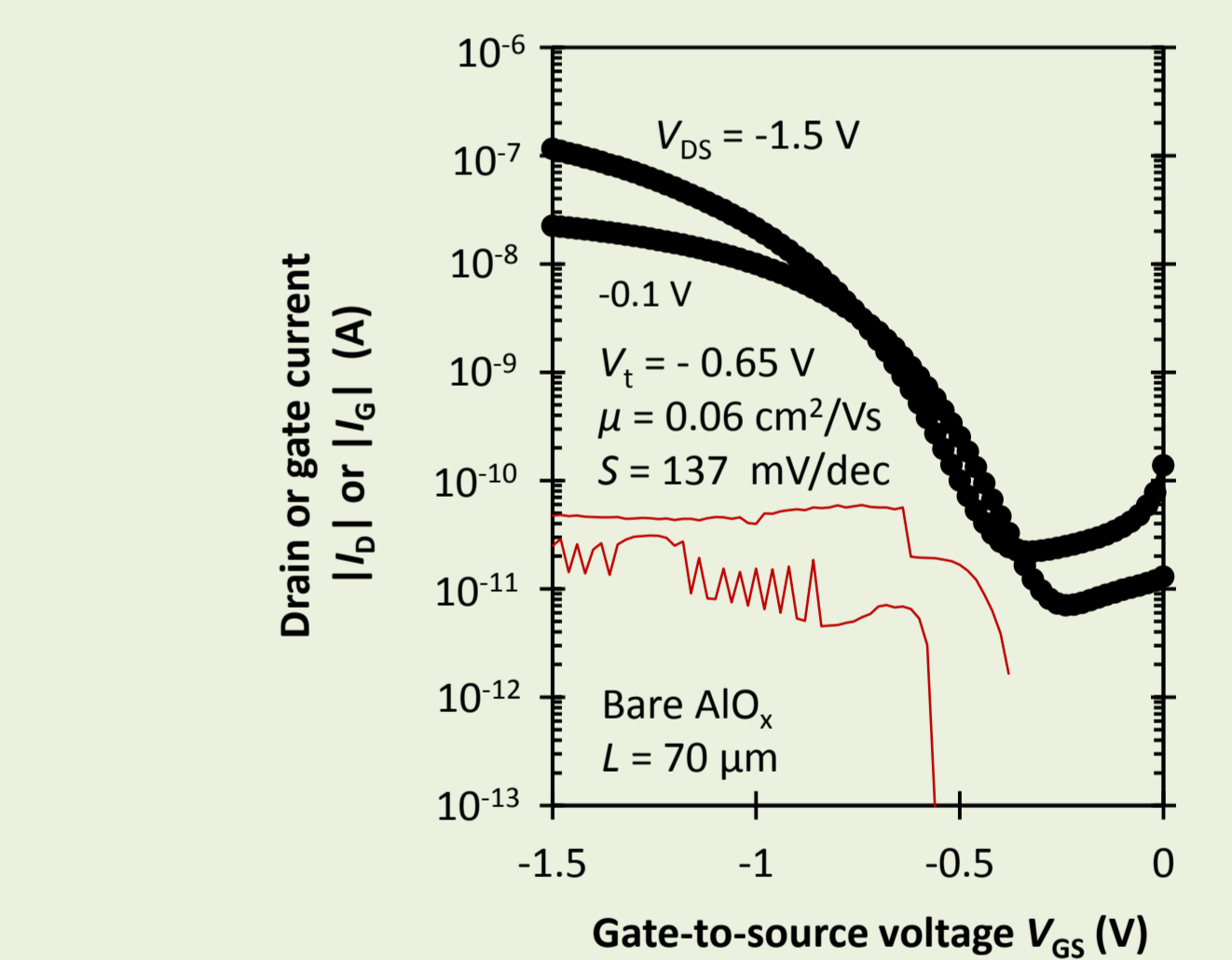
RESULTS: PENTACENE TRANSISTORS



PENTACENE TRANSISTORS



DNTT TRANSISTORS



CONCLUSIONS

- Leakage current density and capacitance are lower for ALD- AlO_x ; primarily as a result of the thicker layer.
- C_8PA self-assembly is not affected by the AlO_x layer or by its treatment.
- UV-ozone- AlO_x leads to the lowest threshold voltage. Other parameters are comparable to OTFTs with ALD- AlO_x .
- DNTT OTFTs show greatly improved transistor performance over pentacene devices; DNTT offers lower threshold voltage and substantially higher mobility.

ACKNOWLEDGEMENTS

Stuart Hannah is a recipient of a DTG Scholarship funded by Engineering and Physical Sciences Research Council (EPSRC). He would like to thank the School of Engineering of University of Glasgow for transistor fabrication support, the Micro/Nano Fabrication Laboratory of Princeton University for access to ALD system, New Technology Research Centre of University of West Bohemia for FTIR measurements, and C. Watson from School of Electronic Engineering of Bangor University for ellipsometry measurements.