Hardware accelerated image processing to enable real-time adaptive radiotherapy

The accuracy of radiotherapy is constrained by organ motion and deformation occurring between the acquisition of CT and MR images used to plan the treatment and the time at which the treatment is delivered. Adaptive radiotherapy uses image data acquired at the time of treatment to adapt the original treatment plan to match the current patient anatomy. Currently, the image processing and dose calculation algorithms required to perform this plan adaptation cannot be executed in a clinically acceptable timeframe. Hardware acceleration has the potential to speedup these algorithms, making real-time adaptive radiotherapy a clinical possibility[1].

Hardware acceleration is a technique where an algorithm is implemented using hardware that is better suited to the specific algorithm than more general purpose processors in order to reduce the execution time of the algorithm. This can be achieved using field programmable gate arrays (FPGA), which are devices consisting of reconfigurable hardware, allowing their function to be customised for a specific application. These devices have been shown to be able to accelerate image processing algorithms pertinent to adaptive radiotherapy[2].

In this study a global thresholding algorithm based on Otsu's method combined with a three dimensional mean filter was used to segment a series of CT images of a Modus QUASAR respiratory motion phantom into three unique classes. A Xilinx Zynq Z-7020 device consisting of a dual-core ARM Cortex-A9 central processing unit (CPU) coupled to an 85 000 logic cell FPGA was used to accelerate the algorithm by implementing sections of it in the reconfigurable hardware. The execution time of this implementation was compared to an implementation running on an ARM CPU and Intel Core-i5 CPU.

The execution times of the implementations are shown in table 1. The hardware accelerated implementation was found to execute nearly sixty times as fast as the un-accelerated algorithm. The hardware accelerated implementation was also found to run around 14% faster than on the more powerful Intel Core-i5 CPU. Figure 1 shows an example of the segmentation results where the blue contour represents the boundary between two of the classes.

Table 1: Algorithm execution times

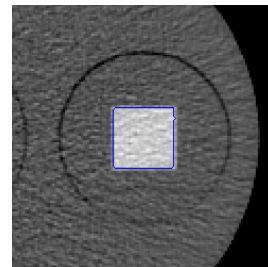| Implementation	Execution Time (ms)
Hardware Accelerated	14.8
ARM Cortex-A9	885.0
Intel Core-i5	17.0

Figure 1: CT slice of phantom with boundary between two classes marked in blue

In the algorithms presented here the overhead of transferring data to the hardware represents a significant proportion of the algorithm execution time. It is anticipated that greater acceleration will be possible for algorithms with greater computational complexity because the data transfer overhead will represent a smaller proportion of the overall execution time.

The requirement for fast processing in radiotherapy is likely to increase as the amount of data available to more accurately guide treatment increases through the use of techniques such as 4D CT and image-guided radiotherapy. FPGA have been shown to be effective at accelerating certain algorithms required for real-time adaptive radiotherapy, however, more research is required to establish which will execute faster on other types of hardware, such as CPU and graphical processing units (GPU). It is likely that heterogeneous computing platforms, composed of a mixture of hardware architectures, will be used in the future implementation of real-time adaptive radiotherapy.

References:

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