Active Control of DC Fault Currents in DC Solid-State Transformers during Ride-Through Operation of Multi-Terminal HVDC Systems

Rui Li, Lie Xu, *Senior Member, IEEE*, Liangzhong Yao, *Senior Member, IEEE*, and Barry W. Williams

***Abstract*—When a pole-to-pole dc fault occurs in a multi-terminal HVDC system, it is desirable that the stations and dc solid-state transformers on healthy cables continue contributing to power transfer, rather than blocking. To reduce the fault current of a modular multilevel converter based dc solid-state transformer, active fault current control is proposed, where the dc and ac components of fault arm currents are regulated independently. By dynamically regulating the dc offset of the arm voltage rather than being set at half the rated dc voltage, the dc component in the fault current is reduced significantly. Additionally, reduced ac voltage operation of the dc solid-state transformer during the fault is proposed, where the ac voltage of transformer is actively limited in the controllable range of both converters in the transformer to effectively suppress the ac component of the fault current. The fault arm current peak and the energy absorbed by the surge arrester in the dc circuit breakers are reduced by 31.8% and 4.9% respectively, thereby lowering the capacities of switching devices and circuit breakers. Alternatively, with the same fault current level, the dc-link node inductance can be halved by using the proposed control, yielding lowered cost and volume. The novel active fault current control mechanism and the necessary control strategy are presented and simulation results confirm its feasibility.**

***Index Terms*—Active fault current control, average model, dc fault protection, dc solid-state transformer, modular multilevel converter (MMC), multi-terminal HVDC system, ride-through operation.**

I. Introduction

DC fault protection is an issue to be resolved for the development of modular multilevel converter (MMC) based HVDC transmission systems. [1-4]. The dc circuit breakers (DCCBs), including mechanical DCCBs, solid-state DCCBs, and hybrid DCCBs, have the potential to isolate a dc fault and protect stations from damage. However, the response of conventional mechanical DCCBs is slow and converter semiconductors endure high current stress during the response time [5-7]. The solid-state DCCBs can rapidly isolate a fault but at high capital cost and significant on-state losses. Hybrid dc circuit breakers can clear a fault in milliseconds but have a large footprint and high capital cost [8, 9].

In [10], limiting reactors are series connected with the fast acting DCCBs (e.g. solid-state DCCBs, hybrid DCCBs) to limit the fault current *di/dt* and decrease the fault current peak. However, all the system stations are blocked during the fault to avoid overcurrents, causing shutdown of the entire multi-terminal HVDC system. The ride-through operation of a multi-terminal HVDC system is presented in [11, 12], where additional series dc inductors and slow DCCBs are used to limit the fault current increase rate and isolate the fault. For a dc fault applied at the dc-link node, the stations connected to the healthy branches of the HVDC system are far from the fault location so the fault has less influence.

Recently, the concept of the 'dc solid-state transformer' (DCT) has been proposed which uses active controlled power electronic components to optimize converter performance. By blocking all the converters of the dc solid-state transformer, dc faults can be isolated without significantly affecting the healthy system parts. Similar to the ac transformer, the dc solid-state transformer can adapt the dc voltage to any higher or lower voltage level. Due to the absence of common standards, current HVDC systems are built with different dc voltage levels [13-16]. Thus, the dc solid-state transformer appears the only approach to connect and interconnect existing HVDC links with different dc voltages. Additionally, the solid-state transformer can contribute to the power flow and dc voltage control which are required to operate the dc grid properly and efficiently. Moreover, the solid-state transformer can provide galvanic isolation for safety reasons and for the normal operation of converters connected in the multi-terminal HVDC system [9].

Solid-state transformers include the thyristor based solid-state transformer [17, 18], the dual-active bridge (DAB) transformer [19], and the MMC based transformer [20]. Due to extremely low switching losses and improved harmonic characteristics, the MMC based dc solid-state transformer is an attractive approach [21-23], so is considered in this paper. In [9], a terminal station with a different dc voltage rating is connected to the main HVDC link through a dc solid-state transformer. When a dc fault is applied at a dc cable, the solid-state transformer on the faulty cable can be blocked quickly to

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isolate the fault from the healthy main HVDC link. Thus the stations on main HVDC link can be operated continuously. However, a fault on the main HVDC link is not considered.

The aim of this study is to use active control of the dc fault currents to reduce current stresses on solid-state transformer and DCCBs during ride-through operation of the healthy parts of a multi-terminal HVDC system under a dc fault. The paper is organized as follows. In Section II, the radial three-terminal HVDC system incorporating a solid-state front-to-front dc transformer is presented. The fault current of a dc solid-state transformer during ride-through operation is analyzed in Section III. In Section IV, novel active control of the fault current is proposed, where the dc and ac components of fault currents are regulated independently. The active fault current control is assessed in Section V, considering a pole-to-pole dc fault at the dc-link node of a three-terminal HVDC system. Finally Section VI draws the conclusions.

II. Radial Three-Terminal HVDC System Incorporating A DC Solid-State Transformer

A. System Configuration

Fig. 1 shows the radial three-terminal HVDC system being studied, where dc inductances and DCCBs are at the both ends of Cables 1 and 2 and one end of Cable 3 (T_3) to limit the fault current increase rate and isolate the fault. The other end of Cable 3 (O_3) is connected to the dc-link node through a dc solid-state transformer to isolate the fault on Cable 3 from the main HVDC link and to match the dc voltage of station S_3 (±300kV) to that of the main HVDC link (±400kV).

As shown in Fig. 2, the dc solid-state transformer is composed of two MMCs (MMC_1 and MMC_2) which are front-to-front connected through a three-phase ac transformer. Both MMCs in the dc transformer, as well as the stations S_1, S_2, and S_3, employ the generic MMC topology with half-bridge (HB) submodules (SMs). The dc transformer operates with sinusoidal waveforms on the ac side for controllability and good harmonic characteristics, compared to the quasi two-level control in [9].

Stations S_1 and S_3 regulate the dc voltages of the dc network, while S_2 injects rated active power P_2 into ac grid G_2. In the solid-state transformer, MMC_1 regulates the ac voltage while MMC_2 operates in an active power control mode and exports rated power P_3 from the main dc-link to the ac side. A modified average model of the generic MMC is used for all the converters in Fig. 1 to reduce computation time and accelerate the simulation, as will be detailed in Section II C.

The parameter details of the test system are listed in Table I. The ac side voltages of the DCT are set to produce an approximate modulation index of 0.7, when sinusoidal modulation is used [24-26]. Each cable is modeled with 10 pi sections to simulate high frequency behavior during a fault and obtain satisfactory simulation accuracy [27, 28].

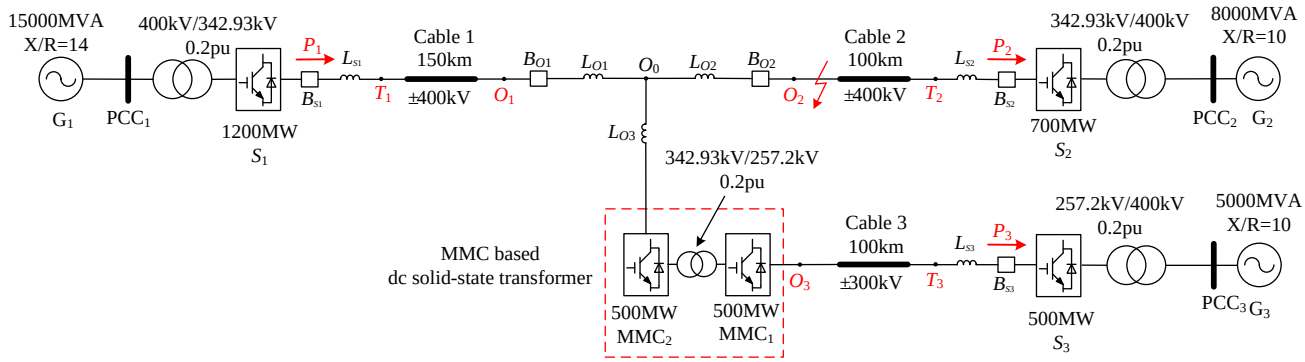

Fig. 1. Radial three-terminal HVDC transmission system using average models of half-bridge based MMCs, incorporating a solid-state front-to-front dc transformer.

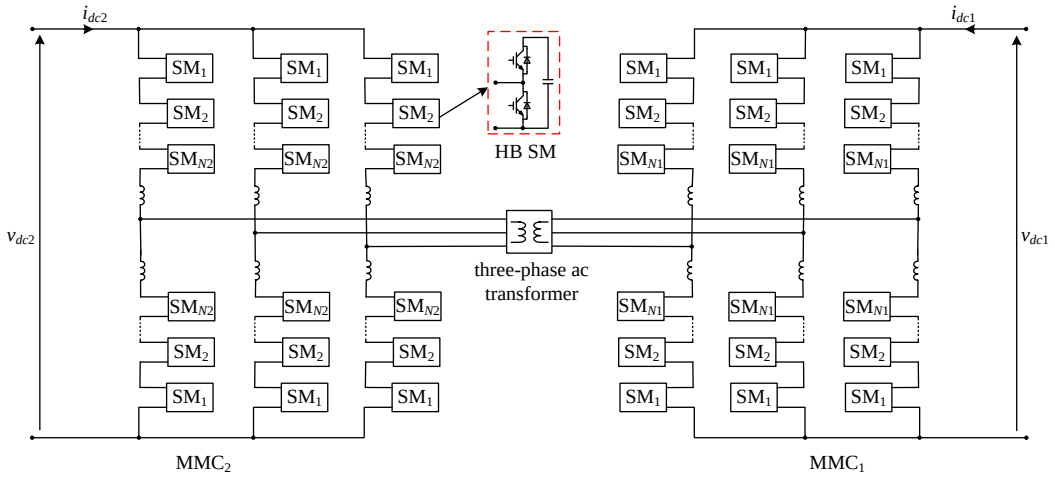

Fig. 2. DC solid-state transformer based on the generic MMC topology with half-bridge submodules.

As the active fault current control to be proposed does not depend on the fundamental operating frequency of the dc transformer, the DCT MMCs are operated at 50Hz for simulation simplicity. With a higher operating frequency, for example, 500Hz, the SM capacitance, arm inductance, and three-phase ac transformer sizes can be reduced significantly, but at the expense of higher switching losses [29, 30].

TABLE I
Nominal Parameters of Modeled Test System.

PARAMETER	Nominal value
rated dc voltages of DCT MMC_1 and station S_3: V_{dc1}	±300kV
rated dc voltages of DCT MMC_2 and stations S_1 & S_2: V_{dc2}	±400kV
power rating of stations S_1: P_1	1200MW
power rating of stations S_2: P_2	700MW
power rating of station S_3 and MMC_1 & MMC_2 in transformer: P_3	500MW
SM number per arm of DCT MMC_1 and station S_3	285
SM number per arm of DCT MMC_2 and stations S_1 & S_2	380
SM capacitor voltage: V_{SM}	2.105kV
SM capacitance of DCT MMC_1 and station S_3	4.59mF
SM capacitance of DCT MMC_2	3.46mF
SM capacitance of stations S_1	8.3mF
SM capacitance of stations S_2	4.84mF
fundamental operating frequency of DCT	50Hz
arm inductance	5%pu
station terminal inductance	100mH
dc-link node inductance	300mH
pi section number in the dc cable	10
R, L, and C of dc cable	9mΩ/km, 1.4mH/km, 0.23μF/km

B. Consideration of DC Fault Ride-Through Operation

As the HB SMs do not have dc fault blocking capability, the high fault current flows through the SM freewheel diode, from the ac grid into the fault on the dc side, even if the MMC station is blocked. Thus, dc fault ride-through operation is a challenge for the development of HB based MMCs.

When a pole-to-pole dc fault occurs at Cable 3, MMC_1 and MMC_2 in the transformer are both blocked to isolate the fault from healthy stations S_1 and S_2. As the blocking time of IGBTs is only several microseconds, the fault can be rapidly isolated by the solid-state transformer. Thus, a fault at Cable 3 does not expose the ride-through operation of stations S_1 and S_2 to significant risk [9], and thus it is unnecessary to use the scheme to be proposed.

However, if a dc fault occurs at O_2 as shown in Fig. 1, it is desirable that stations S_1 and S_3 continue operating without disrupting power transfer between S_1 and S_3 through the solid-state transformer. This requires that there are no overcurrents in S_1, S_3 and the solid-state transformer during the fault period, while the DCCBs isolate the fault from the rest of the dc network. If slow DCCBs with 10ms opening time are used [12, 31, 32], it is necessary to limit the fault current increase, especially in MMC_2 of the transformer. As the fault is near MMC_2, its SM capacitors are rapidly discharged through node inductors L_{O2} and L_{O3} (MMC_2 cannot be blocked if dc fault ride-through is to be achieved) and high ac currents are likely due to the transformer ac voltages, via freewheel diodes. Thus the pole-to-pole dc fault at O_2 is the most serious fault case for ride-through operation of S_1, S_3 and the solid-state transformer, thus is considered in this paper.

The arm current peak threshold is set at 2pu and the DCCBs are modeled with an opening time of 10ms, which is a typical time that can be achieved for the mechanical DCCBs [12, 31, 32].

C. Modified Average Model of Generic MMC

As MMCs typically use hundreds of SMs per arm in HVDC application, it is a burden to simulate the whole system using detailed switching models. To reduce computation time and accelerate the simulation, average models are used to evaluate MMC performance in normal operation and during a dc fault [33-35]. It is demonstrated in [33-35] that improved average models are applicable to pole-to-pole dc fault studies, with high accuracy.

However, the average model in [27] is only valid when the SM capacitance is large enough to maintain near constant SM capacitor voltage. One of the most important reasons is that only one equivalent capacitor is used in the MMC model. Thus the state equation that describes MMC behavior is significantly reduced, resulting in model inaccuracy [27].

But the modified average model adopted in this paper, Fig. 3, uses 6 capacitors for the MMC and can represent the MMC behavior accurately under various operating conditions, including a pole-to-pole dc fault. Its derivation is based on the average models presented in [34-37] and the reference voltage and current for the controllable voltage and current sources and the IGBT switching logic are detailed in [36, 37] and [34] respectively.

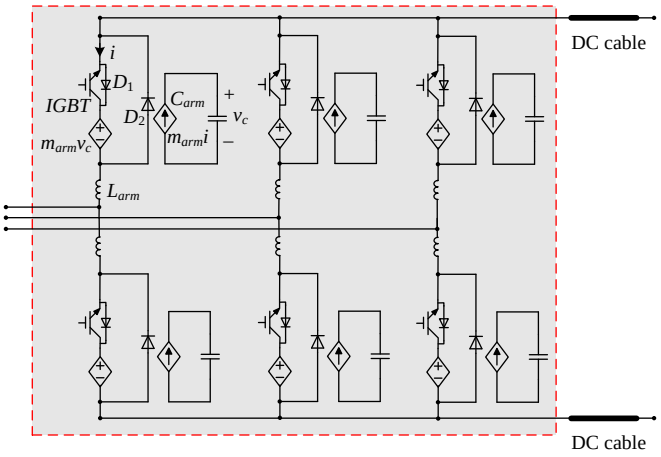

Fig. 3. Modified average model of generic MMC with half-bridge submodules.

The modified average model in Fig. 3 provides reliable representation of MMC behavior during dc fault ride-through operation. This is achieved with the typical SM capacitance requirement of 30-40kJ/MVA as suggested by ABB in [38], which yields a capacitor voltage ripple in the range of ±10%. Compared to the average model with only one equivalent capacitance in [27], the modified average model in Fig. 3 reproduces MMC behavior during dc fault ride-through

operation without compromising accuracy [34, 35] and is adopted in this paper.

As only one capacitor C_{arm} is used per arm in Fig. 3, SM capacitor voltage balancing is not considered in the average model [27, 34, 39, 40]. By using a sorting algorithm, SM capacitor voltages during dc fault ride-through operation can be balanced in a detailed switching model [41-43].

III. Fault Current Analysis of the DC Solid-State Transformer

This section discusses the current behavior of the dc solid-state transformer, with conventional control, during a pole-to-pole dc fault.

A. DC Component in the Fault Current with Conventional Control

When a dc fault is applied at a dc cable, the solid-state transformer connected on the healthy cable continues operating. The generated upper and lower arm voltages of the MMC in the transformer are

$$v_u = -v_{ref} + \tfrac{1}{2}V_{dc} \quad (1)$$

$$v_l = v_{ref} + \tfrac{1}{2}V_{dc} \quad (2)$$

where v_{ref} is the reference ac voltage of the MMC in the transformer; V_{dc} is the rated dc voltage; and u and l refer to the upper and lower arms, respectively.

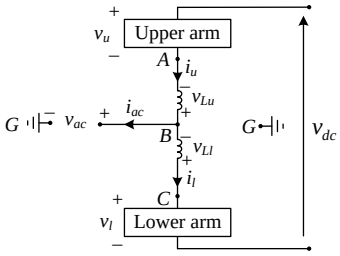

Fig. 4. Equivalent circuit for one phase during ride-through without blocking the converter.

Assuming the dc voltage drop of the DCT MMC is Δv_{dc} ($\Delta v_{dc} \geq 0$) after a dc fault, the converter actual dc voltage v_{dc} and the voltages between A and G (v_{AG}), and C and G (v_{CG}), as shown in Fig. 4, can be expressed as

$$v_{dc} = V_{dc} - \Delta v_{dc} \quad (3)$$

$$v_{AG} = \tfrac{1}{2}v_{dc} - v_u = v_{ref} - \tfrac{1}{2}\Delta v_{dc} \quad (4)$$

$$v_{CG} = -\tfrac{1}{2}v_{dc} + v_l = v_{ref} + \tfrac{1}{2}\Delta v_{dc}. \quad (5)$$

Under normal operation, the dc voltage drop Δv_{dc} is zero, thus the voltages v_{AG} and v_{CG} in Fig. 4 both equal the reference ac voltage v_{ref}, as depicted by (4) and (5). However, during the dc fault, v_{AG} and v_{CG} are not equal to v_{ref} due to the dc voltage drop Δv_{dc} and the voltages across the upper and lower arm inductors, from (4) and (5), can be approximated as

$$v_{Lu} = v_{Ll} = \tfrac{1}{2}\left(v_{CG} - v_{AG}\right) = \tfrac{1}{2}\Delta v_{dc}. \quad (6)$$

As a pole-to-pole dc fault results in significant dc voltage drop Δv_{dc}, a large dc voltage of $\tfrac{1}{2}\Delta v_{dc}$ is generated across the arm inductors. Consequently, high dc fault current results in the converter arms with conventional control.

To further analyze the behavior of the dc component in the fault arm current, each MMC phase can be represented by the phase capacitor C_p in series with inductance L_p and resistance R_p, as shown in Fig. 5, where C_p, L_p and R_p are expressed as

$$C_p = 2C_{SM}/N, \qquad L_p = 2L_{arm}, \qquad R_p = 2R_{arm}. \quad (7)$$

N is the number of SMs per arm; C_{SM} is the SM capacitance; and L_{arm} and R_{arm} are the inductance and resistance of the arm reactor.

As the initial voltage of C_p is the rated dc voltage V_{dc}, the fault arm current flowing through the switching devices can be derived from the equivalent circuit in Fig. 5 [33]:

$$i_f(t) = \frac{\Delta v_{dc}}{2\omega_f L_{arm}} e^{-t/\tau_1} \sin\omega_f t + I_0 \sqrt{1 + \frac{1}{\tau_1^2 \omega_f^2}}\, e^{-t/\tau_1} \sin(\omega_f t + \alpha) \quad (8)$$

where I_0 is the initial current flowing through the switching devices; $\tau_1 = \dfrac{2L_{arm}}{R_{arm}}$; $\omega_f = \sqrt{\omega_0^2 - 1/\tau_1^2}$; $\omega_0 = \dfrac{1}{2}\sqrt{\dfrac{N}{L_{arm}C_{SM}}}$; and $\alpha = \arctan\tau_1\omega_f$.

Assuming the SM capacitor voltages are balanced in the fault mode, they are depicted by

$$v_C(t) = \frac{\Delta v_{dc}}{N}\sqrt{1 + \frac{1}{\tau_1^2\omega_f^2}}\, e^{-t/\tau_1} \sin(\omega_f t + \alpha) + \frac{V_{dc} - \Delta v_{dc}}{N}. \quad (9)$$

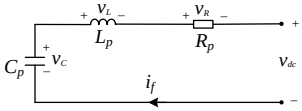

Fig. 5. Equivalent phase capacitor discharging circuit.

Conventionally, the dc components of the arm voltages are controlled at half the rated dc voltage, even during a dc fault, to support the dc-link voltage. However, high dc components are generated in the fault arm currents due to the large dc voltage drop Δv_{dc} during a dc fault and the dc components dominate the fault arm currents, as shown in (8). To reduce the dc component in the fault currents during a dc fault, the dc offsets of the arm voltages can be reduced, rather than being set at half the rated dc voltage. Based on this observation, active dc component control of the fault current is proposed, as detailed in Section IV A and C.

B. AC Component in the Fault Current

To regulate the ac current (i_{ac}, Fig. 4), the peak of ac phase voltage (v_{ac} in Fig. 4, referenced to the dc-link mid-point G) should be less than $\tfrac{1}{2}v_{dc}$, when sinusoidal modulation is adopted [24-26]. Initially following a remote dc fault, the actual dc voltage v_{dc} of the DCT converter (MMC_1 and MMC_2, Fig. 2) is higher than the threshold of v_{dcth} defined by

$$v_{dcth} = 2V_m \quad (10)$$

where V_m is the peak (amplitude) of the ac phase voltage v_{ac} in Fig. 4. Thus, the DCT converter can control ac current (i_{ac}, Fig. 4) and dc components dominate in the fault arm currents, as mentioned. After the MMC actual dc voltage v_{dc} falls below the threshold voltage v_{dcth}, the DCT converter loses control of ac currents and high currents are forced by the ac side voltage into the dc side.

The ac side voltages of stations S_1, S_2, and S_3, Fig. 1, are fixed and are determined by the grid voltage and the

transformer ratio. For a solid-state transformer, the ac voltage is set by one MMC in the transformer and is conventionally constant to guarantee maximum power transfer capability. In order to reduce the ac components in the fault arm currents, reduced ac voltage operation of the dc solid-state transformer is proposed and detailed in Section IV B and C.

IV. Active Control of the Fault Current

The fault arm current during a pole-to-pole dc fault is composed of dc and ac components. In this section, active fault current control is proposed where the dc and ac fault current components are independently controlled to suppress the fault arm currents.

A. Active DC Component Control of the Fault Arm Current

In order to reduce the dc component in the fault current, active dc component control of the fault current is proposed, where the dc offsets of the arm voltages are dynamically regulated. As the HB submodules cannot generate a negative voltage, the upper and lower arm voltages are depicted by

$$v_u = \begin{cases} \tfrac{1}{2}\left(V_{dc} - \text{PID.out}\right) - v_{ref}, & V_{dc} - \text{PID.out} \geq 2v_{ref} \\ 0, & V_{dc} - \text{PID.out} < 2v_{ref} \end{cases} \quad (11)$$

$$v_l = \begin{cases} v_{ref} + \tfrac{1}{2}\left(V_{dc} - \text{PID.out}\right), & V_{dc} - \text{PID.out} \geq -2v_{ref} \\ 0, & V_{dc} - \text{PID.out} < -2v_{ref} \end{cases} \quad (12)$$

where PID.out is the output of the proposed active dc component control of the fault current and meets the requirement described by (13):

$$\begin{cases} \text{PID.out} = 0, & \text{in normal operation} \\ \text{PID.out} \geq 0, & \text{during a dc fault} \end{cases}. \quad (13)$$

According to (11) and (12), the voltages v_{AG} and v_{CG} can be expressed as

$$v_{AG} = \begin{cases} \tfrac{1}{2}\left(\text{PID.out} - \Delta v_{dc}\right) + v_{ref}, & V_{dc} - \text{PID.out} \geq 2v_{ref} \\ \tfrac{1}{2}\left(V_{dc} - \Delta v_{dc}\right), & V_{dc} - \text{PID.out} < 2v_{ref} \end{cases} \quad (14)$$

$$v_{CG} = \begin{cases} \tfrac{1}{2}\left(\Delta v_{dc} - \text{PID.out}\right) + v_{ref}, & V_{dc} - \text{PID.out} \geq -2v_{ref} \\ -\tfrac{1}{2}\left(V_{dc} - \Delta v_{dc}\right), & V_{dc} - \text{PID.out} < -2v_{ref} \end{cases}. \quad (15)$$

As a result, the voltages across the upper and lower arm inductors can be approximated as

$$v_{Lu} = v_{Ll} = \begin{cases} \tfrac{1}{2}\left(\Delta v_{dc} - \text{PID.out}\right), & V_{dc} - \text{PID.out} \geq 2\left|v_{ref}\right| \\ \tfrac{1}{4}\left(2\Delta v_{dc} - V_{dc} - \text{PID.out} - 2v_{ref}\right), & V_{dc} - \text{PID.out} < -2v_{ref} \\ \tfrac{1}{4}\left(2\Delta v_{dc} - V_{dc} - \text{PID.out} + 2v_{ref}\right), & V_{dc} - \text{PID.out} < 2v_{ref} \end{cases}. \quad (16)$$

Comparing (16) to (6), the following equation can be derived when $V_{dc} - \text{PID.out} \geq 2\left|v_{ref}\right|$:

$$\tfrac{1}{2}\left(\Delta v_{dc} - \text{PID.out}\right) \leq \tfrac{1}{2}\Delta v_{dc}. \quad (17)$$

This equation indicates that the voltages across the arm inductors are reduced by the output of the PID controller in the active dc component control, and thus, the fault currents are lowered by actively regulating the dc components of the arm voltages. As the HB SMs cannot generate negative voltages, the converter controllability of the dc components in the fault currents is limited in the conditions $V_{dc} - \text{PID.out} < -2v_{ref}$ and $V_{dc} - \text{PID.out} < 2v_{ref}$. However, benefitting from the proposed reduced ac voltage operation of the solid-state transformer, as detailed in Section IV B and C, the DCT ac voltage is always limited to the converter controllable range. This not only reduces the fault current ac component, but also improves controllability of the fault current dc component.

B. Reduced AC Voltage Operation of the DC Solid-State Transformer

To reduce the fault current ac component, solid-state transformer operation with reduced ac voltages is proposed, where the amplitude of the ac phase voltage (v_{ac}, Fig. 4) is actively limited in the controllable range of both transformer converters. Thus, the ac voltage contribution to the fault current is reduced. Fig. 6 illustrates the ac phase voltage in the ac component fault current control. During normal operation (t=0 to 0.03s), the peak of ac phase voltage (v_{ac}, Fig. 4) is lower than half the rated dc voltage (600kV) and the ac currents can be regulated. Assume the actual dc voltage of the DCT MMC (v_{dc}, Fig. 4) drops below the original peak of phase voltage v_{ac}, after the dc fault is applied at a dc cable at t=0.03s. By using active fault current ac component control, the ac voltage peak is limited to half the reduced dc voltage to avoid inrush currents forced by the ac voltage. Due to the reduced ac voltage, the power transfer capability of the solid-state transformer is correspondingly lowered. But this reduces the fault current significantly and thus the solid-state transformer can be operated continuously rather than having to be blocked. Additionally, the dc circuit breaker capacity is reduced by the active control.

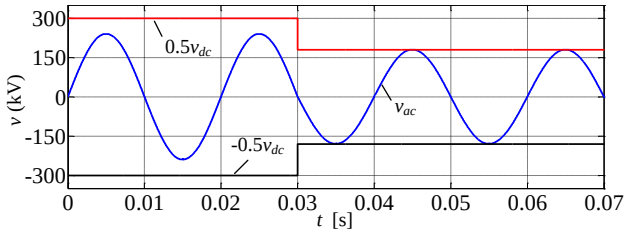

Fig. 6. AC phase voltage in the proposed reduced ac voltage operation of dc solid-state transformer.

C. Active Fault Current Control Strategy

The proposed active fault current control is shown in Fig. 7. MMC_1 in the solid-state transformer operates in an ac voltage control mode and its control strategy is shown in Fig. 7 (a). MMC_2 is assigned to control the active power with a control strategy illustrated in Fig. 7 (b), where only active dc component control for the fault current is required and the reference voltage v'_{ref2} is set by the current control loop [44, 45].

After the fault occurs, the arm inductors suffer a high fault short-circuit voltage, as depicted by (6), which causes a rapid increase of fault currents. Thus, the active dc component control of fault current is required to have a fast response and the ability to predict the future error of the system response. PID control is thus used to effectively limit the dc component of the fault current, as shown in Fig. 7. The fault current dc

component is obtained by subtracting the rated dc current I_{dc} (I_{dc1} and I_{dc2}, Fig. 7) from the actual dc current i_{dc} (i_{dc1} and i_{dc2}, Fig. 7) and is used as the feedback for the PID controller. During normal operation, the PID controller input is limited to zero by the dead zone block such that the arm voltage dc offsets are at their rated value. If the fault current is outside the predefined dead band, the PID controller output starts to increase from zero and regulates the arm voltage dc offsets continuously. The fault current band needs to be set such that active dc component control can quickly be enabled after the fault but avoid false activation under normal operation.

The ac voltage of the dc transformer needs to be controlled and coordinated between MMC_1 and MMC_2 to ensure controllability of both MMC ac currents. As demonstrated in Fig. 7 (a), PI control sets the ac side voltage of the transformer. Compared with open loop control, PI control suppresses the dc voltage variation disturbance and thus the ac voltage can be accurately set to the reference value.

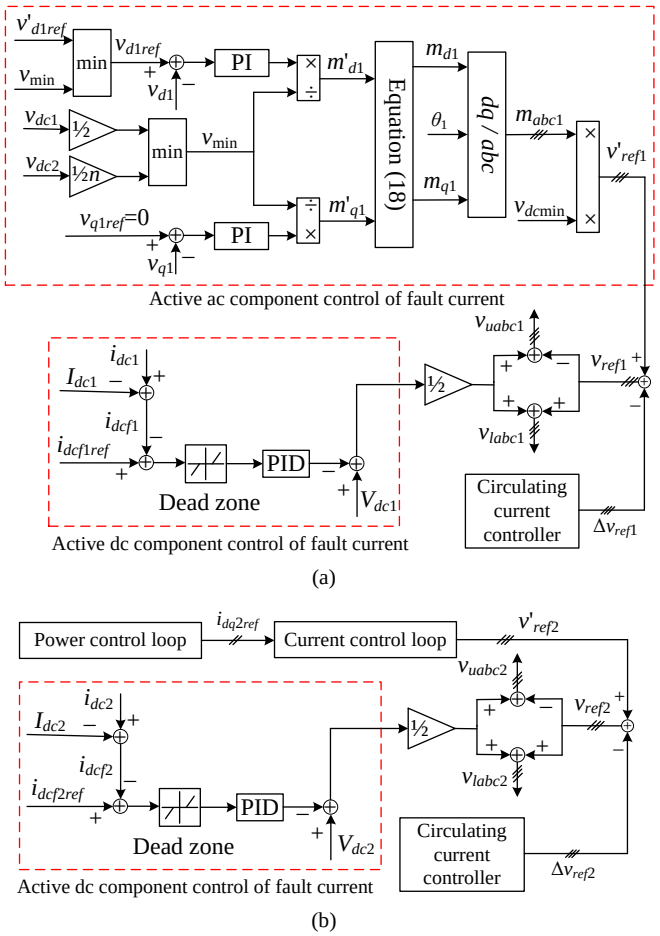

Fig. 7. Active control strategy of the dc solid-state transformer: (a) ac voltage control mode and (b) power control mode.

The reference voltages v_{d1ref} and v_{q1ref}, Fig. 7 (a), need to be set to limit the ac phase voltage to less than half the actual dc voltage. To achieve this, the *d*-axis reference voltage v_{d1ref} is obtained as $v_{d1ref} = \min\left(v'_{d1ref}, v_{\min}\right)$ while the *q*-axis reference voltage v_{q1ref} is set at 0. v'_{d1ref} is the original *d*-axis reference voltage and $v_{\min}$ is obtained from the minimum value of the two dc voltages of the dc transformer: $v_{\min} = \min\left(\tfrac{1}{2}v_{dc1}, \tfrac{1}{2}nv_{dc2}\right)$, where n is the ac transformer ratio. Thus, the ac voltages of the dc transformer are always within the control range of both MMC_1 and MMC_2 when the actual dc voltage is lower than the rated value. The inrush currents forced by the ac voltage are thus avoided by the proposed active ac component control of the fault current.

The minimum voltage $v_{\min}$ is the base voltage for the pu values of the PI outputs m'_{d1} and m'_{q1}, which are then limited by (18) to avoid over-modulation and further limit the ac voltages within the converter control range:

$$m_{d1} = \frac{m'_{d1}}{\sqrt{m'^{\,2}_{d1} + m'^{\,2}_{q1}}}, \qquad m_{q1} = \frac{m'_{q1}}{\sqrt{m'^{\,2}_{d1} + m'^{\,2}_{q1}}}. \tag{18}$$

The dc transformer operates with reduced ac voltage during the fault to lower the fault current and restores the rated value after the fault is isolated, in order to transfer rated power.

By independently regulating the dc and ac components in the fault currents, the proposed active control significantly reduces the fault currents. This implies the submodule capacitors are discharged by a smaller fault current and their voltages can be maintained higher during a dc fault. This characteristic improves converter controllability of the dc transformer and reduces oscillation during restoration after the fault is isolated. As the SM capacitors and the ac voltage provide less energy to the dc side fault, the converter actual dc voltage v_{dc} under active control is lower than that with conventional control. Nevertheless, even with a lower converter dc voltage, the proposed active control still reduces the fault currents.

The proposed fault current control is achieved by actively regulating the reference waveforms for the upper and lower arms, rather than carrier waveforms. This makes it independent on the carrier waveform arrangement and is thus valid for both of the N+1 and 2N+1 modulations [46, 47].

As shown in Fig. 8 (b), even under the most severe pole-to-pole dc fault, the dc solid-state transformer with active control regulates the ac current as well as during normal operation. Additionally, by using active control, the maximum arm current peak is reduced from 2.2kA (2.6pu) to 1.5kA (1.8pu), that is, lowered by 31.8%, Fig. 8 (c) and (d). Alternatively, with 600mH inductances at the dc-link node as recommended in [12], the arm current peak is limited to 1.9pu without active fault current control. In other words, the dc-link node inductance can be halved by using the proposed active control, with the same fault current level (less than 2pu). This significantly lowers the cost and volume of dc-link node inductances.

Once a fault is detected (generally any dc fault is detected by monitoring the voltage across link inductors $L_{S1,2,3}$ and $L_{O1,2,3}$), the circuit breaker B_{O2} is commanded to open with a 10ms opening time to isolate the fault from the healthy parts of the multi-terminal HVDC system. Due to the reduced fault current resulting from the proposed active control, the energy absorbed by surge arrestor in B_{O2} is reduced from 26.5MJ to 25.2MJ, a 4.9% reduction.

V. Performance Evaluation during Ride-Through Operation

The active fault current control during ride-through operation is assessed using the model in Fig. 1 with the parameters listed in Table I. The simulated scenario assumes the system in Fig. 1 is subjected to a permanent pole-to-pole dc fault at O_2 at t=0.7s. As mentioned, the DCCBs isolate the fault after 10ms from the fault initiation. Station S_2 is blocked after the detection of dc fault while S_1, S_3, and the dc solid-state transformer remain operational.

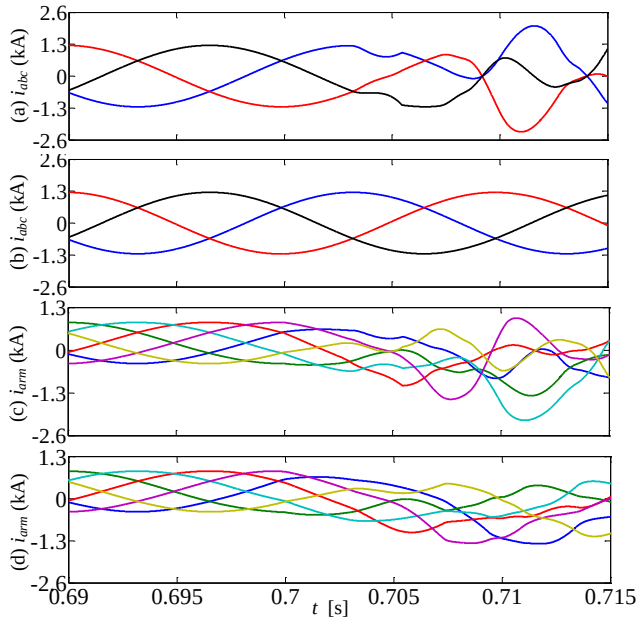

Fig. 8. Comparison between conventional control and the proposed active control: (a) three-phase ac currents with conventional control, (b) three-phase ac currents with active control, (c) arm currents with conventional control, and (d) arm currents with active control.

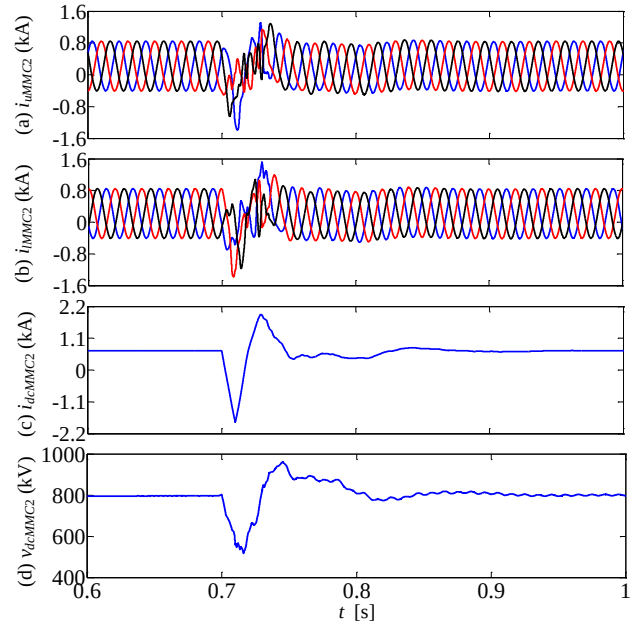

Fig. 9. Waveforms of MMC_2 in the dc solid-state transformer: (a-b) upper and lower arm currents, (c) dc current, and (d) dc voltage.

A. DC Solid-State Transformer Performance

By virtue of the proposed active fault current control, the fault arm current peak of MMC_2 in the transformer is reduced to 1.8pu, lower than the current threshold (2pu), Fig. 9 (a) and (b). After the fault, the dc current of MMC_2 changes direction and reaches a maximum value of 1.9kA during the restoration period, Fig. 9 (c).

As MMC_1 is decoupled from the fault by MMC_2, the dc fault influence on MMC_1 is less than that on MMC_2. The arm currents, dc current and dc voltage of MMC_1 present less disturbance during the fault, as observed in Fig. 10.

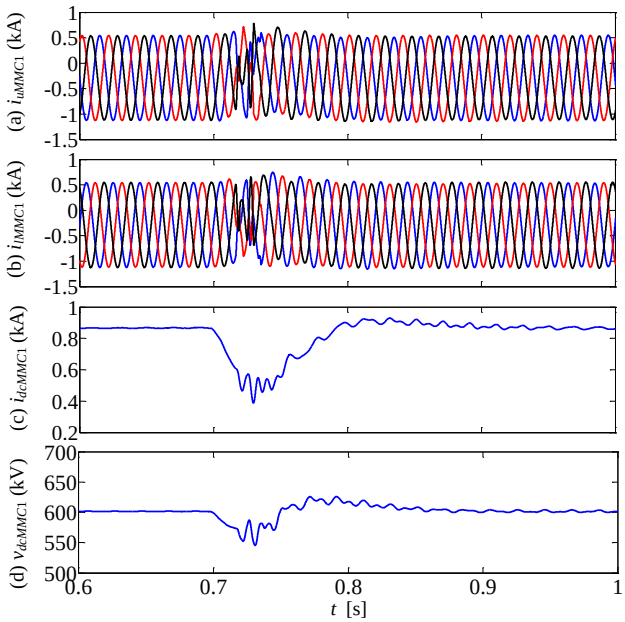

Fig. 10. Waveforms of MMC_1 in the dc solid-state transformer: (a-b) upper and lower arm currents, (c) dc current, and (d) dc voltage.

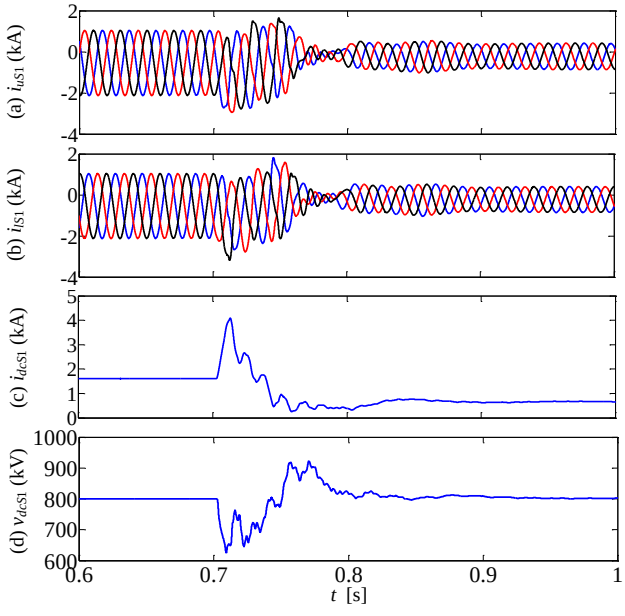

Fig. 11. Waveforms at station S_1: (a-b) upper and lower arm currents, (c) dc current, and (d) dc voltage.

B. Performance of Station Converters

The solid-state transformer is robust to dc faults, benefiting

from the new active fault current control. This makes it possible to continuously operate the healthy stations (S_1 and S_3) in the dc network, even though the test system is subjected to the most severe type of dc fault (pole-to-pole dc fault) and typical slow DCCBs (10ms) are used to isolate the fault.

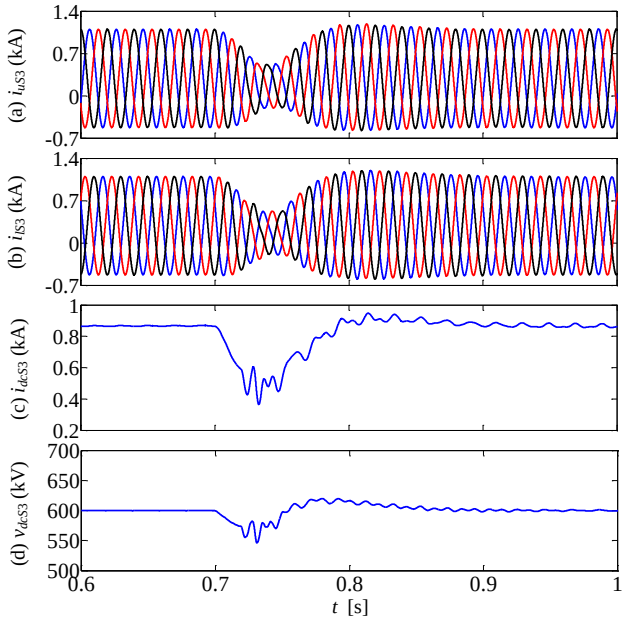

Fig. 12. Waveforms at station S_3: (a-b) upper and lower arm currents, (c) dc current, and (d) dc voltage.

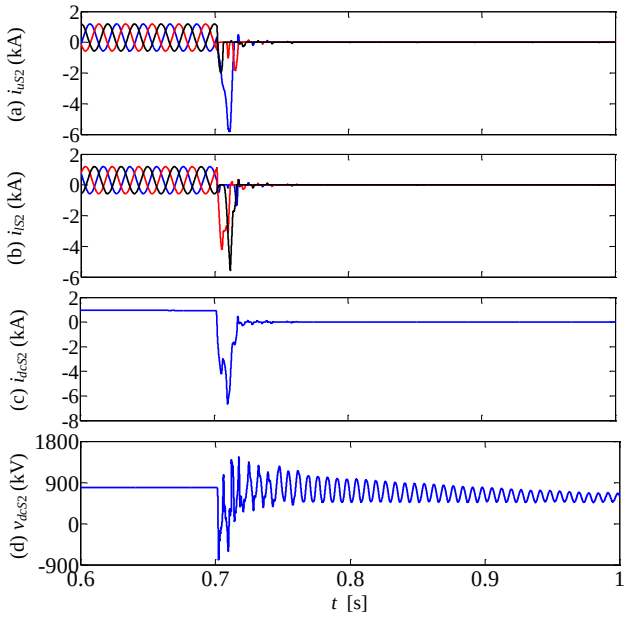

Fig. 13. Waveforms at station S_2 on the faulty branch: (a-b) upper and lower arm currents, (c) dc current, and (d) dc voltage.

The arm currents of station S_1 are lower than 1.5pu, Fig. 11 (a) and (b). As station S_3 is connected to the fault via the dc transformer, which is robust to the dc fault, the fault disturbance on station S_3 is much lower than that experienced by station S_1. S_3 does not experience excessive overcurrents during the fault, Fig. 12. The dc current of S_1 increases after the fault and reaches a peak of 4.1kA. Due to the different power direction and the robustness of the dc transformer to dc faults, the dc current of S_3 decreases and does not change direction. As station S_2 is isolated from the healthy parts, the steady-state dc current of S_1 is reduced from 1.5kA to 0.6kA after the fault, which is identical to that of MMC_2 in the transformer, Fig. 11 (c).

Station S_2 is immediately blocked after fault detection and circuit breaker B_{S2} is commanded to open with a 10ms delay, in order to isolate the fault from S_2 and protect the active switches. In Fig. 13 and Fig. 14, the freewheel diodes suffer the fault currents due to the long opening time of the circuit breaker (10ms) and the maximum diode $\int i^2(t)dt$ is 154kA^{2}s.

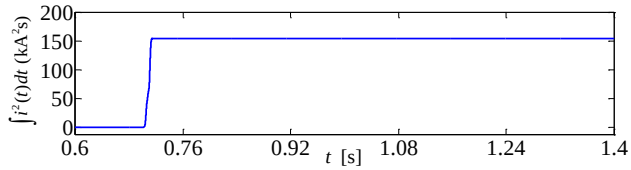

Fig. 14. Maximum diode $\int i^2(t)dt$ at station S_2.

C. DC Circuit Breaker Stresses

Fig. 15 shows the waveforms of breaker B_{O2} which is connected on the faulty branch at the dc-link node. The fault current flows through the mechanical switch until the switch opens at around t=0.71s. Then the current through the switch is commutated into the surge arrestor to limit the voltage across the circuit breaker, without exposing it to significant overvoltage. In Fig. 15 (b), the voltage across the circuit breaker is lower than 600kV (1.5pu). Only circuit breaker B_{O2} opens after detecting the fault at the dc-link node while B_{O1} and the dc transformer continue to transfer power between stations S_1 and S_3. As a result, the voltage across the surge arrestor in B_{O1} is always around zero, so does not absorb energy during the fault. All the opening energy is absorbed by the surge arrestor in B_{O2} and this energy is almost 25MJ, as shown in Fig. 15 (c).

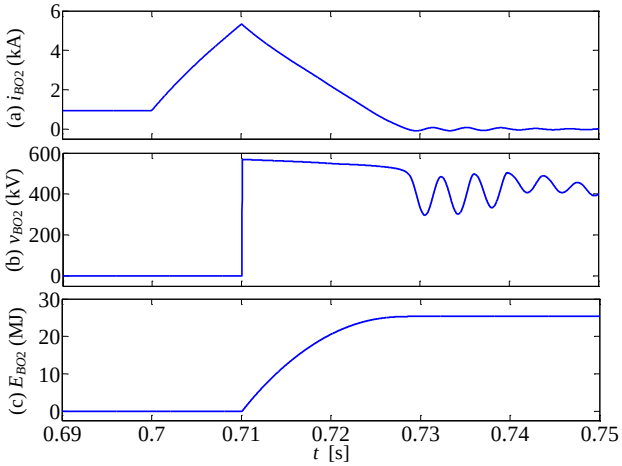

Fig. 15. Waveforms of dc circuit breaker B_{O2} at dc-link node: (a) current, (b) voltage, and (c) DCCB absorbed energy.

Besides B_{O2} (connected on the faulty branch at the dc-link node) opening, breaker B_{S2} at the terminals of station S_2 also needs to open to protect station S_2 converter. As shown in Fig. 16, circuit breaker overvoltage is avoided and the energy absorbed by the surge arrestor in DCCB B_{S2} is less than 7MJ.

The simulated pole-to-pole dc fault, which is the most

serious fault case for ride-through operation of the dc transformer, causes disturbance for the converters on the healthy branches, especially for DCT MMC_2, as it is close to the fault location. However, benefitting from the proposed active fault current control, the fault currents are significantly reduced and the submodule capacitor voltages are maintained higher during a dc fault, which improves dc transformer converter controllability and reduces oscillation during restoration, after the fault is isolated. All the fault currents are lower than the threshold (2pu) and the healthy parts are gradually restored to normal operation. DC fault ride-through operation of multi-terminal HVDC systems is thus achieved.

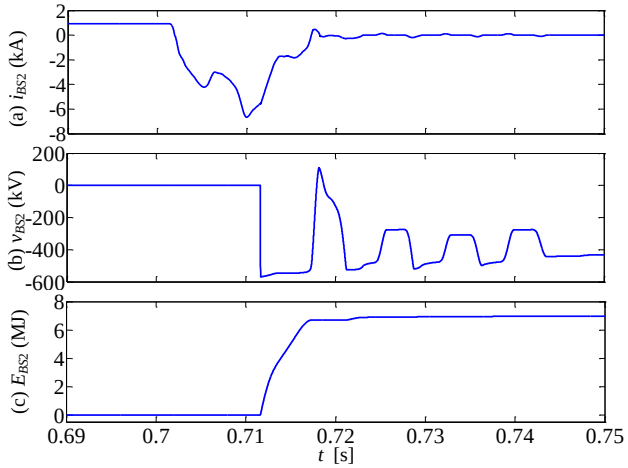

Fig. 16. Waveforms of dc circuit breaker B_{S2} at terminal of station S_2: (a) current, (b) voltage, and (c) DCCB absorbed energy.

VI. Conclusion

This paper proposes active fault current control of the dc solid-state transformer during a pole-to-pole dc fault, where the dc and ac components of the fault currents are independently suppressed. The mechanism of the novel active control was analyzed and a control strategy was presented. By dynamically regulating the dc offsets in the arm voltages rather than being set at half the rated dc voltage, the dc component in fault current is reduced by the proposed active control. The ac component in the fault current is also effectively lowered with the proposed reduced ac voltage operation of the dc transformer where the ac side voltage of transformer is actively limited in the controllable range of both transformer converters. The maximum arm current peak and the energy absorbed by surge arrestor in the dc circuit breaker are reduced by 31.8% and 4.9% respectively, and thus devices with low power capacity can be potentially used, yielding reduced losses and capital cost. The dc-link inductance can be halved that recommended in [12] by using active control thus the cost and volume of the dc-link inductors are decreased. System ride-through operation with a dc fault on the main HVDC link is achieved without exposing the dc transformer or station converters to significant fault currents and overvoltages.

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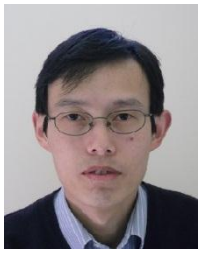

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