**OCDMA, Electronic Bottleneck, and Challenges for Fiber-Optic Communications**

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Optical fibre links have a great capacity potential for the point-to-point data transport. This aggregate data throughput has been further improved by implementation of data multiplexing techniques such as DWDM, OTDM, and OCDM. However these fibre link capabilities becomes severely limited at the fiber links end points where the routing and switching takes place by the electronic serial data processing abilities of current CMOS electronics. Any possible speed-ups by using electronic parallel processing is confounded by the fundamental limits of Amdahl's Law which states that 'If a computation has a serial component *f %* and a parallel component *p %*, then the maximum speed-up for given an infinite number of processors is *(f+p)/f.'* Clearly, the greater the parallel portion *p*, the higher the speed-up. [1] However, there is a fundamental maximum improvement in computational speed. As the number of parallel processors *n* increases the maximum speed-up value is achieved, beyond which adding more processors will provide diminishing additional computational advantage and will manly increase power consumption.

This scenario just described will soon hinder the ability of data networks to scale up to meet exponentially increasing demand for capacity. While all-optical wavelength routing can improve data network throughput, ultimately at network endpoints any such improvement will be choked by fundamentally limited CMOS electronic signal processing capabilities within routers. Therefore there is a need for overcoming this electronic bottleneck. It is believed that all-optical signal processing would help. In recent years good progress has been made in the development of photonic devices necessary to achieve the above. Any further leap will require development of an ultrafast all-optical switch as the key bases for future photonic logic gates.

Given a future where networks will need to perform ultra-high speed serial data processing all optically there will be basic requirements for all optical devices capable of performing at data rates well beyond is possible electronically today. To overcome this electronic bottleneck we have developed an ultrafast all optical photonic switch [2] which does not suffer from the currier recovery time limitations affecting all optical switches based on Semiconductor Optical Amplifiers demonstrated previously. [3] The schematic of this novel device is shown in Fig 3a) with its sub-picosecond switching capabilities illustrated in Fig 2b).

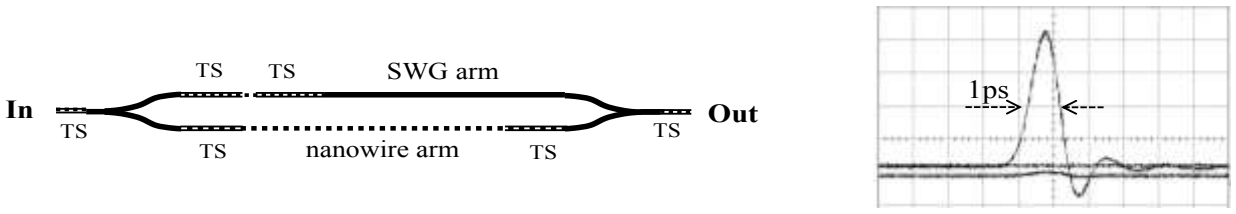


Fig 2. a) Schematic diagram of self-switching all-optical gate; b) demonstration of its terabit/sec switching capabilities. TS – tapered waveguide section, SWG – subwavelength waveguide gating.

The all-optical gate has a Mach-Zehnder interferometric structure with one arm composed of a Si nanowire. The second arm is a subwavelength waveguide grating structure. Tapered sections marked TS are added to properly balance optical device properties and its loss to help achieve complete interferometric switching.

1. T. Brian, http://www.embedded.com/design/mcus-processors-and-socs/4006507/Putting-multicore-processing-in-context-Part-One, Jan 9, 2006.
2. I. Glesk, P. J. Bock, P. Cheben, J. H. Schmid, J. Lapointe, and S. Janz, *Optics Express* **19** 14031 (2011).
3. J. P. Sokoloff, P. R. Prucnal, I. Glesk, and M. Kane, *IEEE Photonics Technology Letters* **5** 787 (1993).

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