

# Optical CMDA in light of current IT challenges

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With growing demands for ultra high speed connectivity the end user expects instantaneous broadband network access. It is becoming very clear that for current technologies based on well-established CMOS will be increasingly difficult to sustain the needed scalability of future electronic switches. However, the limitation of CMOS based electronics can be mitigated by a targeted use of photonic switching. Optical code division multiple access (OCDMA) based interconnects can provide very high spectral utilization, flexible rates while delivering simplified control and management. Higher channel count per the number of used wavelengths when compare to other approaches makes OCDMA a technology to be considered for the use in a number of targeted applications. By understanding challenges IT faces today we can utilize all optical switching to overcome bottlenecks imposed by the electronic switching.

**Key words:** OCDMA, ICT, electronic bottleneck, photonic devices, time gate.

## 1 Introduction

Overall Information and Communications Technology (ICT) energy consumption has been estimated to be around 1.5 PWh and equals to the total annual electricity generation by Japan and Germany. This number amounts to nearly 10% of global energy consumption. In addition, the volume of data passing through communication networks is expected to more than double by 2018. The majority of this rise can be attributed to growth in smart phone, portable and machine to machine (M2M) devices. Smart phones alone generate up to 20 times more data traffic than conventional mobile phones [1,2]. This growing demand for high speed, low latency data transmission has generated a need for substantially increased capacity and improved connectivity within data centers. Current data centers process all data by using electronic technology for switching and routing. They use conventional electronic interconnects, each limited to a maximum throughput of 10 Gb/s. As a result data centres with the technology available today are becoming less and less able to fulfil projected demand into the near future [3]; issues of increased latency and reduced bandwidth to the user are likely to become apparent. In fact Google report shows that an additional latency of 400 ms costs 0.44% in lost search sessions; while Amazon have reported that an additional latency of 100 ms costs them 1% in lost sales.

It is therefore apparent that new technological approaches are required to tackle the growing electronic

bottleneck issues in optical networks and within data centers to ensure sustainable data network growth with minimal latency.

It has been suggested that the fundamental limits of data center switching abilities which relies on bandwidth limited CMOS electronics has now been reached [4]. On the other hand it is becoming evident that all-optical systems using photonic integrated circuits and highly scalable optical interconnects may provide an answer to tackle not only power consumption issues but also deliver data rates well exceeding Terabits per second. However, while the transmission and wavelength routing in dense wavelength division multiplexed (DWDM) based long haul and metro transport systems look set to continue to deliver even higher transmission throughputs, the electronic signal processing, serial MUX/DEMUX and buffering which is necessary at their end points can currently only be achieved using conventional electronic hardware systems. As will be highlighted, electronics based processing cannot continue to scale to sustain the ever increasing serial data throughputs that DWDM backbones, metro networks and data centers demand and as a consequence the electronic bottleneck will result.

## 2 Limitations of electronic signal processing – the electronic bottleneck

The CMOS scaling rules was first described by Dennard in 1974. It states if transistor footprint can be reduced then at the same time switching speed will increase and

power consumption reduce [5]. An important observation of Dennard scaling is that over the years power density (Watts/unit chip area) has remained approximately constant as transistor density has increased. During this period the density of transistors has been increasing by a factor of two every 18 months for over 40 years. In 1965 Gordon Moore suggested an exponential improvement in transistor density. He predicting a doubling of transistor density every two years [6] what became known as ‘Moore’s law’. This trend according to Intel should continue until around 2020 [7].

However, despite the continuing validity of Moore’s law, Dennard scaling came to an end in 2005 with the development of 90nm lithography. At this level, transistor gates become too thin to prevent current from leaking into the substrate.

### 3 Towards all optical signal processing

It is clear from this discussion that the fundamental limits on electronic switching speeds will in the near future severely affect the ability of data networks to satisfy, both quantitatively and qualitatively. While the introduction of all-optical switching schemes [32-35] and advanced optical interconnects can improve latency, contention and overall capacity, a new solution is required to improve data serial processing speeds in order to take full advantage of enormous aggregate throughputs delivered by DWDM systems. The requirement for a new disruptive technology is therefore inevitable. Ideally, development of a photonic transistor allowing faster switching which is compatible with CMOS fabrication techniques would allow cheaper to market solutions than developing an all new ground-up fabrication technology. Silicon photonics devices can be fabricated using present CMOS fabrication techniques and therefore this technology is being widely investigated for the development of future optical signal processing systems [32]. Research in this area is still in its infancy, however some progress in the development of the optical transistor has been reported and several research groups have been successful in demonstrating what may become possible future solutions to this problem.

Chen has demonstrated an optical transistor where a single stored gate photon can control the transmission of applied source photons [36]. However, this transistor is not compatible with CMOS fabrication and since it requires three lasers it is unlikely to provide a practical solution in the foreseeable future.

Another approach by Varghese is the development of a silicon optical transistor which uses an asymmetric coupled add/drop filter consisting of a micro-ring resonator next to an optical waveguide representing the source [37]. Normally light will pass through the source waveguide and exit unaffected since weak source coupling with the micro-ring ensures that nonlinear effects are negligible. Its resonance will therefore remain unaffected. However, at a specific resonant frequency the

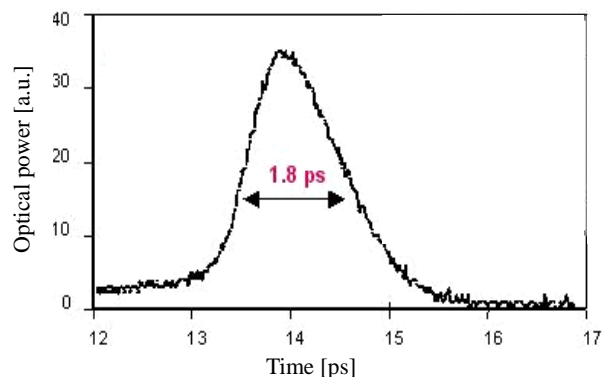
light will interact with the micro-ring resonator greatly reducing the output and changing the state to off. This change in resonant frequency is achieved using another optical waveguide representing the gate. The device is reported to operate at 10GHz. A notable advantage of this technology is compatibility with current state of the art CMOS fabrication techniques allowing scalability and avoiding the need to develop new fabrication techniques from the ground up.

### 4 Optical CDMA

Optical CDMA is a flexible technology for efficient and scalable multiple access. It also offers increased physical layer privacy and on-demand bandwidth sharing management. Recent improvements in fiber photonic technologies have led to several proof-of-concept demonstrations of encoding/decoding hardware for use in OCDMA.

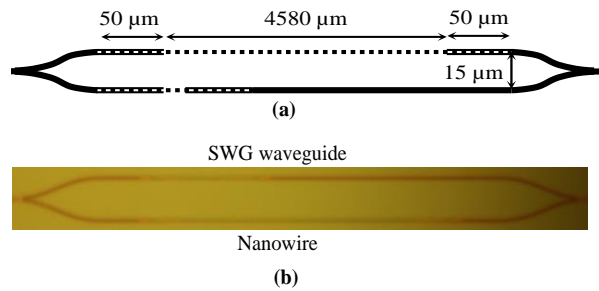
Recently we have developed and demonstrated an advanced highly flexible OCDMA system [38,39] with the aim to increase the number of simultaneous users. The superior scalability was achieved by means of all optical signal processing through elimination of the Multi Access Interference (MAI) by introduction of ultra-fast all optical time gating and a self-clocked receiver based on all optical clock recovery. As shown the MAI noise can be removed if a picosecond (ps) time gating is used immediately after the decoding process of the self-clocked receiver.

Given the future where networks will need to perform at ultra-high serial data rates there will be strong requirements for ultra-fast all optical gating devices capable to perform switching and gating at Terra Hertz (THz) serial data rates. To overcome the existing electronic bottleneck and achieve THz switching speeds we have developed an ultra-fast all optical photonic switch [40-41] which does not suffer from carrier recovery time limitations which can be seen in Fig. 1 and affect all optical switches based on Semiconductor Optical Amplifiers (SOA) demonstrated previously [32-35].



**Figure 1:** Illustration of a switching window distortion due to the SOA recovery time limitations in time gating devices [34].

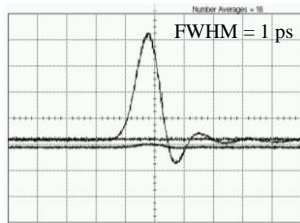
The conceptual schematic of this novel device called Time Gate (TG) is shown in Fig. 1(a) while Fig. 2(b) is



**Figure 2:** (a) Schematic diagram of the time gate; (b) SEM image of the manufactured device. SWG is subwavelength waveguide grating.

its SEM image. The Time Gate has a Mach-Zehnder interferometric structure. TG's one arm is composed of a Si nanowire waveguide. The second arm of TG is a subwavelength waveguide grating (SWG) structure with added tapered sections to balance the coupling losses to and from Y waveguide couplers for achieving complete interferometric switching.

The sub picosecond switching capabilities of TG are demonstrated in Fig. 3. The novel photonic device can be used as a self-switched all-optical time gate.



**Figure 3:** Demonstration of sub picosecond switching capabilities of the time gate.

## 5 Conclusions

Optical fibre networks offer large capacity for data transport. However this tremendous advantage is becoming severely undermined by the insufficient serial data processing speed ability of the currently available CMOS based electronic switching. This will soon hinder the ability of data networks to scale up in order to meet exponentially increasing IT demands.

While all optical wavelength routing can help to improve network data throughputs, ultimately at network endpoints this approach is not sufficient and networks will suffer data processing bottlenecks due to CMOS limited switching capabilities. As the consequence, there

is a great deal of need for development of disruptive switching technologies which will help to overcome the current electronic bottleneck.

On other hand, Optical CDMA with its superior all optical switching and soft blocking capabilities has a potential for implementation at network end points or as optical interconnects in targeted IT applications. Despite the fact that some progress has been made in advancing this technology, any further progression will depend on availability of ultrafast all optical switching devices.

## References

- [1] "Cisco Global Cloud Index: Forecast and Methodology, 2014-2019 White paper," Cisco. (12 March 2016) ([www.cisco.com/c/en/us/solutions/collateral/serviceprovider/global-cloud-index-gci/Cloud\\_Index\\_White\\_Paper.html](http://www.cisco.com/c/en/us/solutions/collateral/serviceprovider/global-cloud-index-gci/Cloud_Index_White_Paper.html))
- [2] "Explosive Growth in Data Traffic and the future of Global Communications Infrastructure," NTT. (14 March 2016). ([www.ntt.com/resource-center/article/data/global-watch02.html](http://www.ntt.com/resource-center/article/data/global-watch02.html))
- [3] D. Barney, "The great cloud bottleneck: How capacity issues can kill your cloud project." (12 June 2011) (<https://redmondmag.com/articles/2011/12/01/cloud-bottleneck-issues.aspx>). (14 March 2016)
- [4] J. Hruska, "The death of CPU scaling: From one core to many and why we're still stuck," Extremetech, 1 Feb. 2012. ([www.extremetech.com/computing/116561-the-death-of-cpu-scaling-from-one-core-to-many-and-why-were-still-stuck](http://www.extremetech.com/computing/116561-the-death-of-cpu-scaling-from-one-core-to-many-and-why-were-still-stuck)).
- [5] R. H. Dennard, IEEE J. Solid-State Circ. **9**, 5 (1974).
- [6] G Moore, Electron. Mag. **38** 20 (1965).
- [7] J. Hruska. "Intel's former chief architect: Moore's law will be dead within a decade," Extremetech, 30 August, 2013, ([www.extremetech.com/computing/165331-intels-former-chief-architect-moores-law-will-be-dead-within-a-decade](http://www.extremetech.com/computing/165331-intels-former-chief-architect-moores-law-will-be-dead-within-a-decade))
- [32] J. P. Sokoloff, P. R. Prucnal, I. Glesk, and M. Kane, IEEE Phot. Technol. Lett. **5**, 787 (1993).
- [33] I. Glesk, J. P. Sokoloff, and P. R. Prucnal. Electron. Lett. **30**, 339 (1994).
- [34] I. Glesk, P. R. Prucnal, I. and Andonovic, IEEE J. Sel. Top. Quantum Electron. **14**, 861 (2008).
- [35] T. B. Osadola, S. K. Idris, and I. Glesk, Quantum Electronics, TELFOR Journal **5**, 48 (2013). Invited paper. ([www.journal.telfor.rs/Published/Vol5No1/Vol5No1.aspx](http://www.journal.telfor.rs/Published/Vol5No1/Vol5No1.aspx))
- [36] W. Chen, K. M. Beck, R. Bucker, M. Gullans, M. D. Lukin, H. Tanji-Suzuki, and V. Vuletić, Science **341**, 68 (2013).
- [37] L. Varghese, L. Fan, J. Wang, F. Gan, X. Wang, J. Wirth, B. Niu, C. Tansarawiput, Y. Xuan, A Weiner, and M. Qi, "A Silicon Optical Transistor," in Frontiers in Optics 2012/Laser Science XXVIII, OSA Technical Digest (online) (Optical Society of America, 2012), paper FW6C.6.
- [38] S. K. Idris, T. B. Osadola, and I. Glesk, J. Europ. Opt. Soc. Rap. Public. (JEOS:RP) **8**, 13013 (2013).
- [39] T. B. Osadola, S. K. Idris, I. Glesk, and W. C. Kwong, IEEE Photon. Tech. Lett. **24**, 395 (2012).
- [40] I. Glesk, P. J. Bock, P. Cheben, J. H. Schmid, J. Lapointe, and S. Janz, Opt. Exp. **19** 14031 (2011).
- [41] I. Glesk, P. J. Bock, P. Cheben, J. H. Schmid, J. Lapointe, and S. Janz, Optical and Quantum Electron. **44**, 613 (2012). Invited paper.