An atomistic simulation investigation on chip related phenomena in nanometric cutting of single crystal silicon at elevated temperatures

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Abstract

Nanometric cutting of single crystal silicon on the different crystal orientations and at a wide range of temperatures (300 K-1500 K) was studied through molecular dynamics (MD) simulations using two sorts of interatomic potentials, an analytical bond order potential (ABOP) and a modified version of Tersoff potential, so as to explore the cutting chip characteristics and chip formation mechanisms. Smaller released thermal energy and larger values of chip ratio (ratio of the uncut chip thickness to the cut chip thickness) as well as shear plane angle were obtained when cutting was performed at higher temperatures or on the (111) crystal plane, implying an enhancement in machinability of silicon. Nonetheless, the subsurface deformation depth was observed to become deeper under the aforementioned conditions. Further analysis revealed a higher number of atoms in the chip when cutting was implemented on the (110) crystal plane, attributable to the lower position of the stagnation region which triggered less ploughing action of the tool on the silicon substrate. Regardless of temperature of the substrate the minimum chip velocity angle was found while cutting the (111) crystal plane of silicon substrate whereas the maximum chip velocity angle appeared on the (110) surface. A discrepancy between the two potential functions in predicting the chip

velocity angle was observed at high temperature of 1500 K, resulting from the overestimated phase instability and entirely molten temperatures of silicon by the ABOP potential. Another key observation was that the resultant force exerted by the rake face of the tool on the chip was found to decrease by 24 % when cutting silicon on the (111) surface at 1173 K compared to that at room temperature. Besides, smaller resultant force, friction coefficient at the tool/chip interface and chip temperature was witnessed on the (111) orientation, as opposed to the other orientations.

Keywords: Molecular dynamics; Cutting chip; Single crystal silicon; Nanometric cutting; Elevated temperatures

1. Introduction

In nanometric cutting of single crystal silicon, the cutting edge of the tool penetrates into the substrate surfaces, which are therefore plastically deformed and slide off along the rake face of the cutting tool at a constant velocity in a stationary flow, resulting in chip formation. Hence, the relative movement of the cutting tool and substrate leads to removing a layer of atoms (chip) from the substrate. The processes in chip formation can be examined within the orthogonal plane, since essential parts of the material flow take place within this plane. The major portion of the plastic deformation during chip formation occurs in the primary shear zone. The substrate atoms are deformed under the action of high friction forces in the secondary shear zones in front of the rake face and the flank face [1]. As the nanometric cutting process involves removing few atomic layers from the surface, it is very difficult to observe the cutting process and measure the process parameters directly from the experiments. Consequently, investigation of atomistic processes occurring at such small

length scales is more amenable to molecular dynamics (MD) simulation [2-3]. Despite the great enthusiasm in exploring nanometric cutting of silicon using MD simulation [4], the current pool of knowledge on the nanometric cutting of silicon at elevated temperatures is still sparse. Single crystal silicon, as a highly anisotropic material in physical and mechanical properties, is a kind of brittle material at room temperature owing to its sp^3 bonding, relatively short bonding length and diamond cubic lattice structure, which make it a difficult-to-cut material. Under high temperature conditions, the yield strength, hardness and fracture toughness of the silicon substrate would reduce and the plastic deformation enhances, which will facilitate the machining process of such difficult-to-cut engineering material.

Chip related phenomena refer to the complex phenomena encountered in nanometric cutting such as behaviour of the work material, required specific energy and degree of interaction at the tool/chip interfaces. Appreciation of chip related phenomenon is thus indispensable to acquire a wide picture of nanometirc cutting of silicon at different temperatures and to clarify what occurs around the cutting edge when the chip is generated at high temperatures. This study therefore aims at applying MD simulation by using two types of interatomic potential functions, an analytical bond order potential (ABOP) [5] and a modified version of the Tersoff [6], to explore chip related phenomena on the tool/chip interface during nanometric cutting of single crystal silicon on three crystallographic orientations i.e. the (010), (110) and the (111) at a range of machining temperatures from 300 K to 1500 K. The unique application of the two potential functions was based on the fact that the modified Tersoff [6] was developed to overcome the shortcomings of the original Tersoff function [7-8] which overestimates the melting point of silicon while the ABOP [5] is more robust in accurately describing the bulk and dimer properties of silicon with a poor prediction of melting point. Indeed, the poor estimation of melting point is a common problem intrinsic to bond order potentials for semiconductors.

2. MD simulation methodology

The three-dimensional MD model used in this study is illustrated in Fig. 1. The geometrical details and process parameters are given in Table 1. The periodic boundary condition (PBC) is imposed along the *z* direction of the simulation domain for the sake of reducing the effects of simulation scale and to mimic the plane-stress condition. The silicon atoms in the substrate and carbon atoms in the cutting tool are divided into Newtonian atoms, thermostat atoms and boundary atoms. Two layers of atoms at the bottom and side of the silicon workpiece in the *y* and *x* directions are boundary atoms which are immovable to ensure structure stability and to prevent the substrate from moving. The two layers above the boundary atom layers are thermostat atoms, and are used to provide adequate outward heat conduction away from the control volume. To this end, a Berendsen thermostat is employed. The third category of atoms in silicon workpiece is called Newtonian atoms, which are allowed to follow the microcanonical (NVE) dynamics in accord with the routine MD principles. The velocity Verlet algorithm with the single time step of 1 fs was employed for the time-marching method in the simulations.

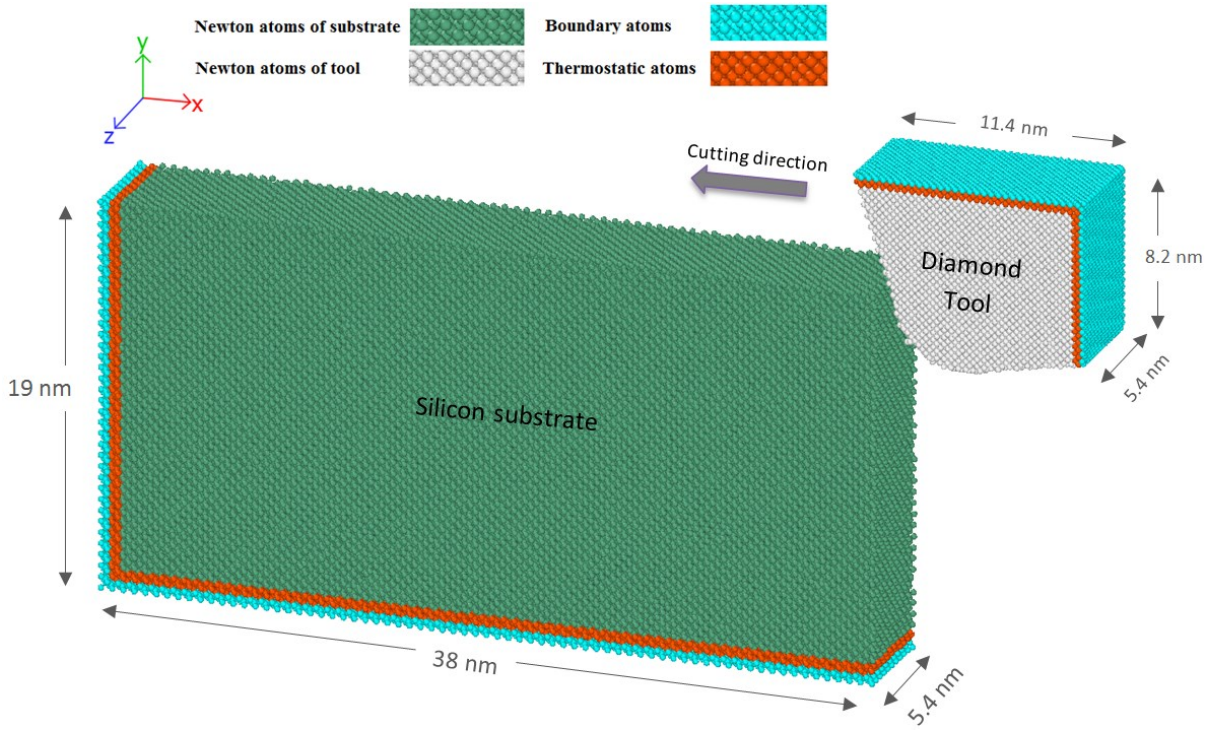


Fig. 1. Schematic MD simulation model for nanometric cutting

Table 1. Geometrical details and process parameters employed in the MD simulations

Workpiece material	Single crystal silicon
Workpiece dimensions	$38\times19\times5.4$ nm^3
Tool material	Single crystal diamond
Cutting edge radius (tip radius)	3.5 nm
Uncut chip thickness (cutting depth in 2D)	3 nm
Cutting orientation and cutting direction	Case 1: (010)<100> Case 2: (110)<00$\bar{1}$> Case 3: (111)<$\bar{1}$10>
Rake and clearance angle of the cutting tool	-25° and 10°

Workpiece temperature	300 K, 500 K, 750 K, 850 K, 1173 K and 1500 K
Cutting speed	50 m/s
Time step	1 fs
Potential energy function	ABOP [5] and modified Tersoff [6]

In MD simulation, interatomic interactions between atoms are commonly introduced by empirical potential functions selected properly for the atomic system. The choice of interatomic potential is crucial to the accuracy of MD simulation results. The most popular bond order potential function for predicting material behaviour of single crystal silicon is the Tersoff potential function [7-8]. Tersoff potential energy is a three-body potential function which is suitable for calculating covalent interactions of silicon and carbon atoms. However, Yoo *et al.* [9] and Cook and Clancy [10] revealed that the original Tersoff potential is not suitable for studying temperature sensitive phenomena as it overestimates the melting temperature of silicon by approximately 50% higher and underestimates the density of the liquid by nearly 14% lower than the experimental values. This motivated Agrawal *et al.* [6] to develop a modified version of the Tersoff potential to overcome the aforementioned shortcomings. Their modification made Tersoff potential a good choice to study elevated temperature processes such as thermal softening behaviour. Analytical bond order potential (ABOP) proposed by Erhart and Albe [5] is another popular potential function for describing the interactions between the atoms within the Si-Si, C-C and Si-C. It is more robust in describing the dimer and bulk properties of silicon over Tersoff potential [7-8] and is regarded as a potential function which can accurately describe the mechanical properties of silicon. Thus, in this study, both the modified Tersoff and ABOP interatomic potential functions are adopted to simulate the nanometric cutting at elevated temperatures and, more

importantly, to make a comparison between the simulation results obtained by both the potentials.

The total energy content of the system is affected by the lattice constant; hence, the lattice constant can influence the accuracy of the simulation results. The equilibrium lattice constant, which is defined as the length of unit cell at the equilibrium volume, ought to be calculated at different temperatures for the employed potential functions in order to attain reliable results. To this end, the minimum potential energy (cohesive energy) corresponding to the equilibrium lattice constant [11] of single crystal silicon and carbon was calculated at different temperatures, which is shown in Table 2. Note that the cohesive energy was time-averaged over 1 ns. The values for lattice constant of diamond shown here are only for the sake of information and were not used during the simulation, mainly because in all the studied cases, the tool was equilibrated at 300 K and then were allowed to follow the NVE dynamics, as mentioned earlier. Therefore the lattice constants of 3.563 Å and 3.568 Å, respectively, were used as the equilibrium lattice constants of carbon for modified Tersoff and ABOP potential functions.

Table 2. Variation of the lattice constant for silicon and carbon in diamond cubic structure obtained from the ABOP [5] and modified Tersoff [6] potential functions at various temperatures

Temperature (K)		Single crystal silicon			Carbon		
		Calculated lattice constant (Å)	Cohesive energy (eV)	Experimental lattice constant (Å) [12]	Calculated lattice constant (Å)	Cohesive energy (eV)	Experimental lattice constant (Å) [11]
300	Modified Tersoff	5.436	-4.628	5.431	3.563	-7.423	3.566
	ABOP	5.433	-4.627		3.568	-7.372	
	Modified	5.439	-4.627		3.564	-7.422	

500	Tersoff			5.434			-
	ABOP	5.436	-4.626		3.569	-7.371	
750	Modified Tersoff	5.443	-4.626	5.439	3.566	-7.421	-
	ABOP	5.439	-4.625		3.571	-7.37	
850	Modified Tersoff	5.444	-4.625	-	3.567	-7.420	-
	ABOP	5.441	-4.624		3.572	-7.369	
1173	Modified Tersoff	5.449	-4.623	5.449	3.569	-7.419	-
	ABOP	5.446	-4.623		3.574	-7.367	
1500	Modified Tersoff	5.454	-4.622	5.457	3.572	-7.416	-
	ABOP	5.451	4.620		3.576	-7.366	

In order to ensure that the atoms of the tool are far from the equilibrium cut-off range of the Si-C interaction, which is in the range of 2.2 to 2.6 Å [5-8], at the beginning of simulation, the diamond tool is set at a distance of 10 Å from the substrate. Then, the model is permitted to run for 30 ps so as to relax the system to the specified temperature. Although the role of environment particularly the oxygen is vital during nanometric cutting experiments, the simulations are still conducted in the vacuum and no chemical reaction and formation of oxide layer is considered here in order to simplify the MD model and purely explore the temperature influence on the chip related phenomena. This can be regarded as a limitation of the simulation studies carried out in this paper. Moreover, due to the limitation of computational power, cutting speed of 50 m/s is chosen in the simulation trials as it is

extremely computationally demanding to implement parametric investigations at real cutting speeds, i.e. 1 to 2 m/s. To perform the simulations, a public-domain computer code, known as "large-scale atomic/molecular massively parallel simulator" (LAMMPS) [13] was employed on a High Performance Computer (HPC) service which was coupled with Open Visualization Tool (OVITO) [14] to visualise and post-process the atomistic data.

3. Results and discussions

3.1. Chip formation process and mechanisms

In nanometric cutting, substrate atoms adjacent to the tool tip are subjected to the high compressive energy, resulting in forming highly displaced and disordered atoms. As the cutting tool advances, the plastically-deformed atoms near the tool tip pile up in front of the tool tip leading to the formation of cutting chips. The atoms above the stagnation region (shown in Fig. 2) are separated from the substrate, and flow upward on the rake face of the cutting tool and accumulate in front of the tool rake face, and consequently forming the cutting chips. The atoms below the stagnation region compress downward by the tool tip, leading to the creation of the freshly formed machined surface via the elastic recovery phenomenon. The position of this region can be identified through the measurement of the average displacement of workpiece atoms in the y direction in different layers. If the average displacement of one layer is positive whereas that of the layer underneath is negative, this range can be recognized as the stagnation region [15].

It is believed that the chips are formed based upon an extrusion-like process triggered by the effective rake angle of the cutting tool [16]. The extrusion-like mechanism might be a consequence of pressure drop (owing to a rise in the contact area) from the tool tip towards the region of the cutting edge [17]. Fig. 3 demonstrates the displacement vector of chip atoms in the XY plane on the different crystallographic orientations. The displacement vector of

each atom was calculated by subtracting its position in the reference configuration from the atom's position in the current configuration i.e. at a cutting distance of 20 nm. The chip formation mechanism in nanometric cutting of single crystal silicon on the (010) crystal plane comprises the extrusion of the workpiece atoms in the cutting direction, [100], and the transverse direction along the [110] direction. Other miller indices of direction during chip extrusion while cutting silicon on the (110) and (111) orientations can be traced from the Fig. 3.

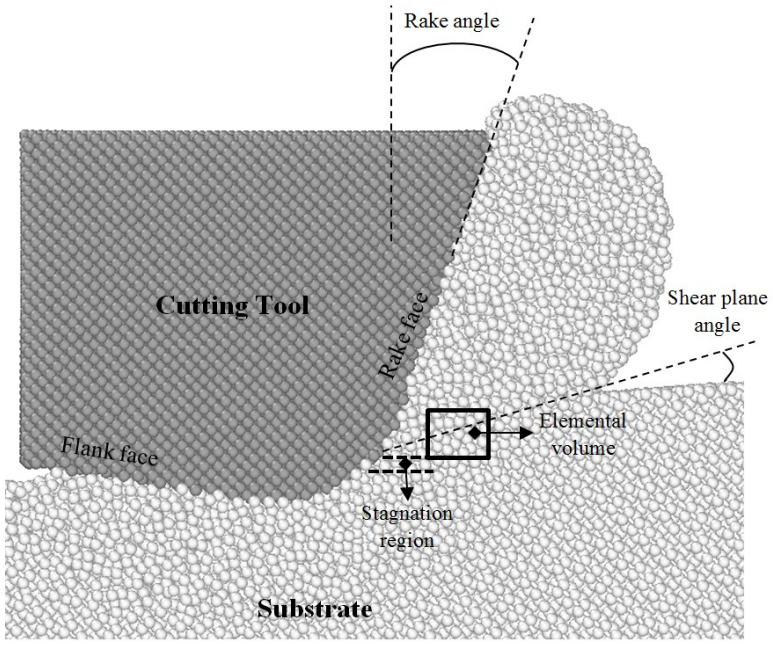


Fig. 2. A snapshot of MD simulation demonstrating stagnation region and shear plane angle. The elemental volume represents the volume of material ($1\times1.5\times3$ nm^3) considered for monitoring the variations of temperature during chip formation (only 2D representation is shown here).

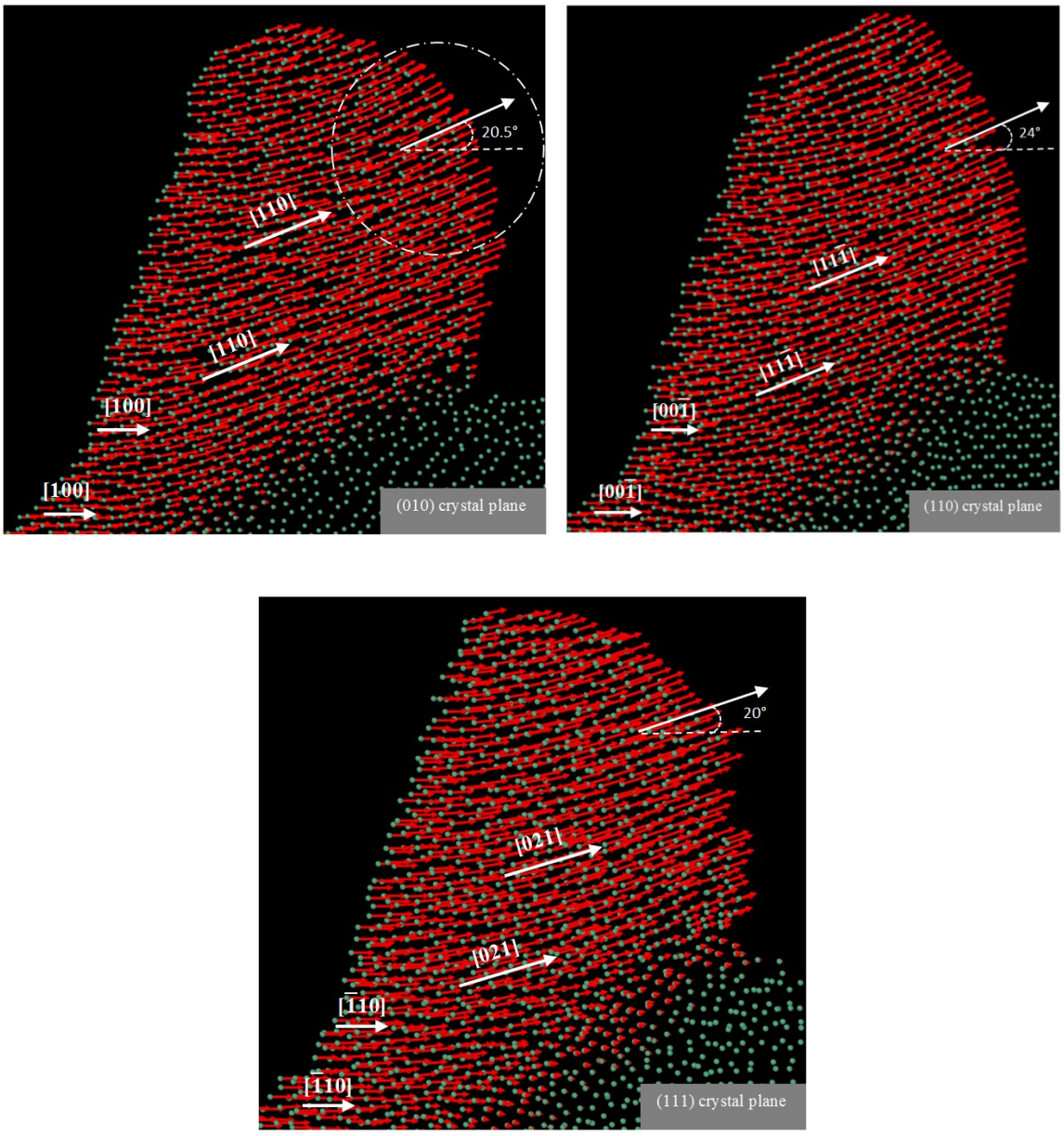


Fig. 3. Displacement vector of chip atoms and their corresponding angles in the *XY* plane. The chip velocity angle was calculated for the atoms located on the right side of the chip.

Fig. 3 also demonstrates the angle of displacement vectors of the chip atoms (chip velocity angle) with relative to the horizontal while cutting silicon on the different crystal planes. Note that the chip velocity angle was calculated on the right side of the cutting chip (shown in Fig. 3) for all the cases since the atoms on the left side of the cutting chip are profoundly affected by the rake face of the tool. Fig. 4 demonstrates the variations of the chip velocity angle with the temperature of the substrate while cutting silicon on the different crystallographic

orientations. It can be seen from Fig. 4 that regardless of temperature of the workpiece the minimum chip velocity angle appears while cutting the (111) crystal plane whereas it reaches the maximum while cutting the (110) surface. Comparing the chip velocity angle at different temperatures of the substrate, it can be found that, using the modified Tersoff potential, the chip velocity angle slightly increases (by ~3°) with the rise of the temperature of the substrate up to ~1200 K. However, a remarkable decrease in angle can be seen at higher temperature, i.e. 1500 K (0.88 T_m), which is near melting temperature of silicon, attributable to the very weak van der Waals interactions between the substrate atoms leading to the movement of chip atoms along the cutting direction rather than along the transvers direction. Nevertheless, such behaviour did not realize when the ABOP potential was employed; hence the chip velocity angle rose constantly with the increase of temperature of the substrate up to 1500 K. The reason for such observation could be traced at the melting point of silicon predicted by the ABOP potential. Since the ABOP potential energy function has not been parameterized to precisely reproduce the melting point of silicon, it is likely that it overestimates the melting temperature of silicon. As a consequence, satisfactory thermal softening which ought to be occurred at high temperature of 1500 K cannot be achieved. An attempt was made so as to calculate the phase instability and entirely molten temperatures of silicon using the one-phase method with reflective boundaries so as to diminish the hysteresis phenomenon. The phase instability and entirely molten temperatures of silicon given by ABOP were observed at 2481 K and 2549 K, respectively, which are far above the experimental value (1687 K). Hence at 1500 K, very weak interatomic interactions cannot be precisely described by ABOP. In the same way, the phase instability and entirely molten temperatures of silicon predicted by the modified Tersoff were calculated to be 1397 K and 1616 K, which are more close to the experimental values. More details on the calculations of the melting temperatures can be found in Appendix A.

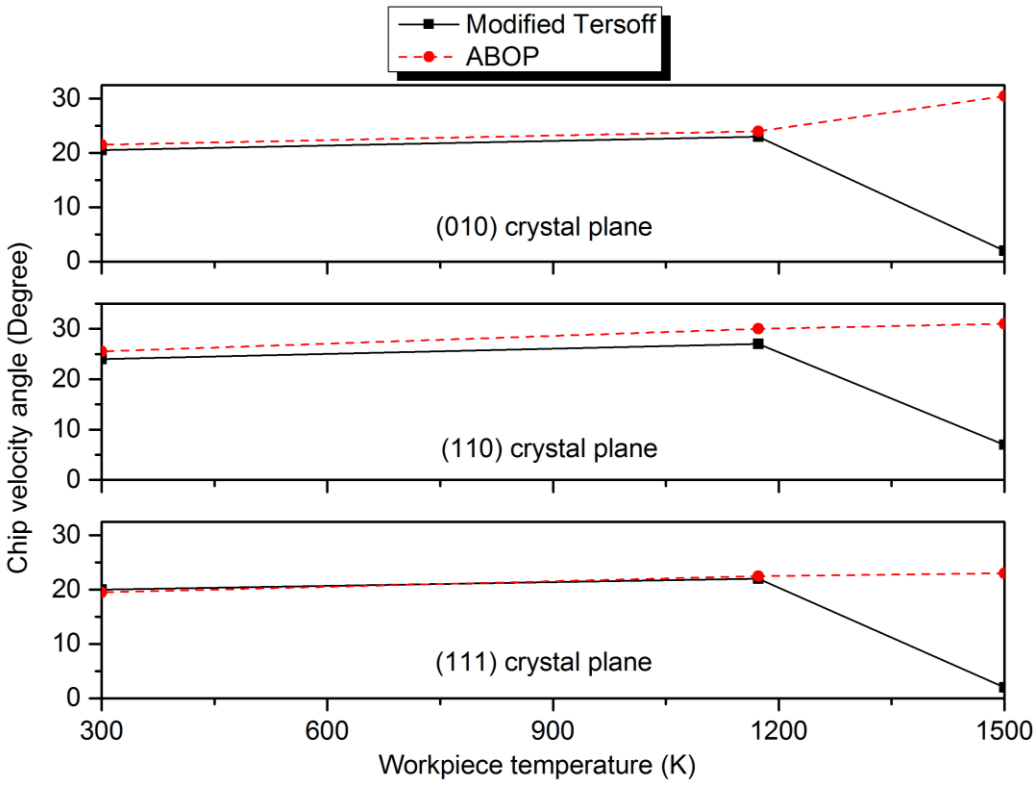
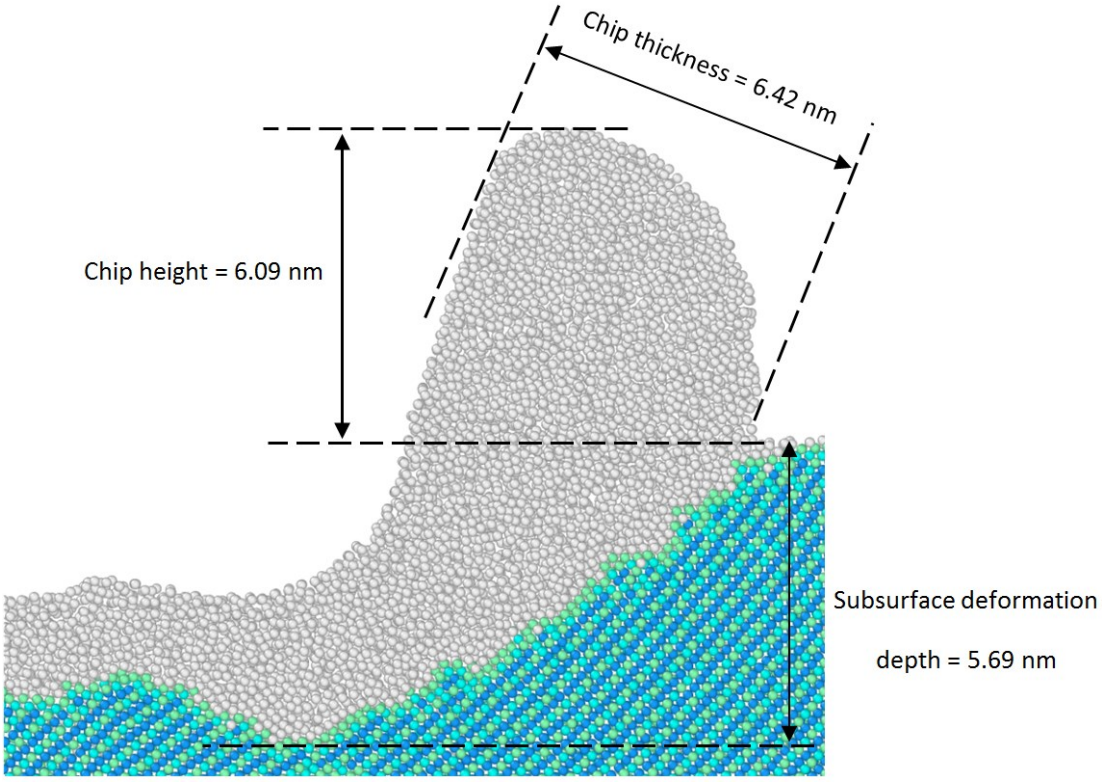


Fig. 4. Chip velocity angle as a function of temperature and crystal orientation obtained by the modified Tersoff and ABOP potential functions

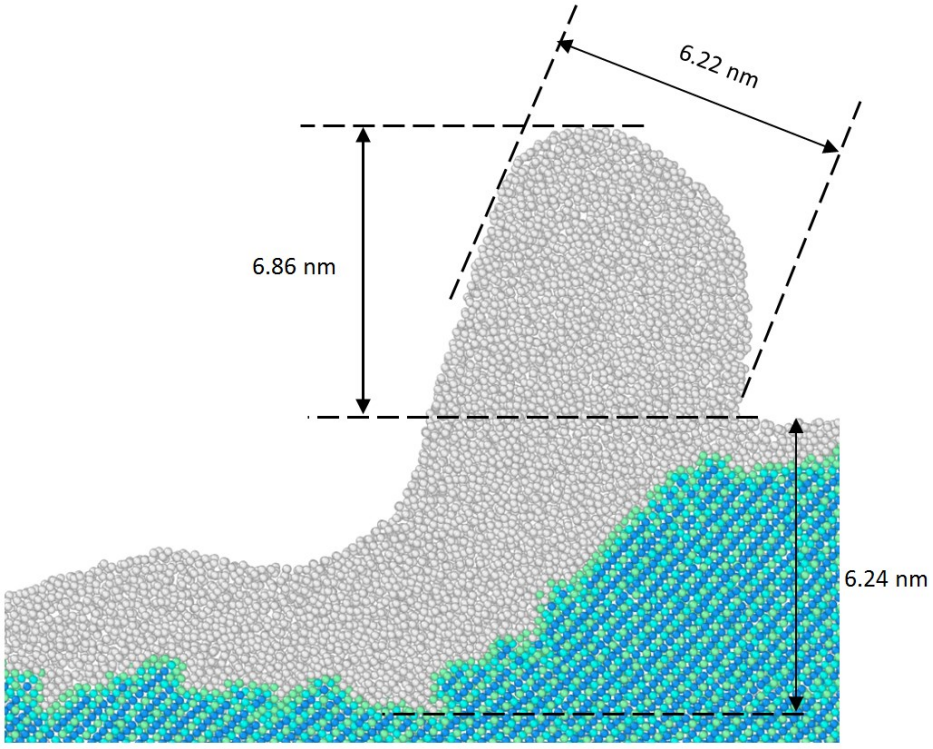
3.2. Geometry and characteristics of the chip

The chip form is a key index of the cutting as it would determine the behaviour of material under the cutting action. Fig. 5 demonstrates a representative cross-sectional morphology of the cutting chip and subsurface crystal deformation of single crystal silicon while cutting the (010) crystal surface at 300 K and 1173 K obtained by the modified Tersoff potential function. White atoms in the figure signify atoms which transformed from their pristine diamond cubic structure to the amorphous state. The subsurface deformation depth shown in Fig.5 was calculated through measuring the height of the lowest layer of the generated amorphous atoms (white atoms) underneath the tool. In addition, the distance between atoms

on up and bottom of the chip where the chip possesses the maximum radius of curvature was considered as the chip thickness.



(a) 300 K



(b) 1173 K

Fig. 5. Cross-sectional morphology of the cutting chip and subsurface crystal deformation of single crystal silicon while cutting the (010) crystal orientation. Atoms in white colour are amorphous atoms.

It can be clearly observed that thinner and taller chip is formed when nanometric cutting is implemented at 1173 K. In addition, when nanometric cutting is performed at room temperature, the depth of subsurface deformation layer is smaller than that of 1173 K. Thus, the deformation depth becomes deeper when the temperature of the substrate rises. As mentioned earlier, when the temperature of the substrate increases, the amplitude of atomic vibration of the substrate atoms increases, which is considered as an increase in the number of phonons. Consequently, atomic displacements are generated which leads to the increase of interatomic distances between atoms and thus weaker interatomic bonding. The weaker bonding between atoms at higher temperature causes more crystal deformation within subsurface atoms. Thus, the layer depth of deformation becomes greater. This particular behaviour apparently seems to be common in both single crystal silicon and 3C-SiC [18].

It can be observed from Fig. 6 that as the temperature of the substrate increases up to ~1200 K, thinner chips are produced, which indicates that lower cutting forces are needed to form the chip. Nevertheless, at temperatures higher than ~1200 K, the chip starts thickening owing to the more pile-up of atoms ahead of the cutting tool due to relatively easier flow of the substrate atoms at high temperatures. However, the cutting force and specific cutting energy keep decreasing as long as the temperature of the substrate is raised [19]. Similar trend was witnessed for the chip height, which has not been shown here. It is interesting to see that while cutting silicon on the (010) plane modelled by the modified Tersoff potential, the chip thickness decreases constantly even at high temperature of 1500 K.

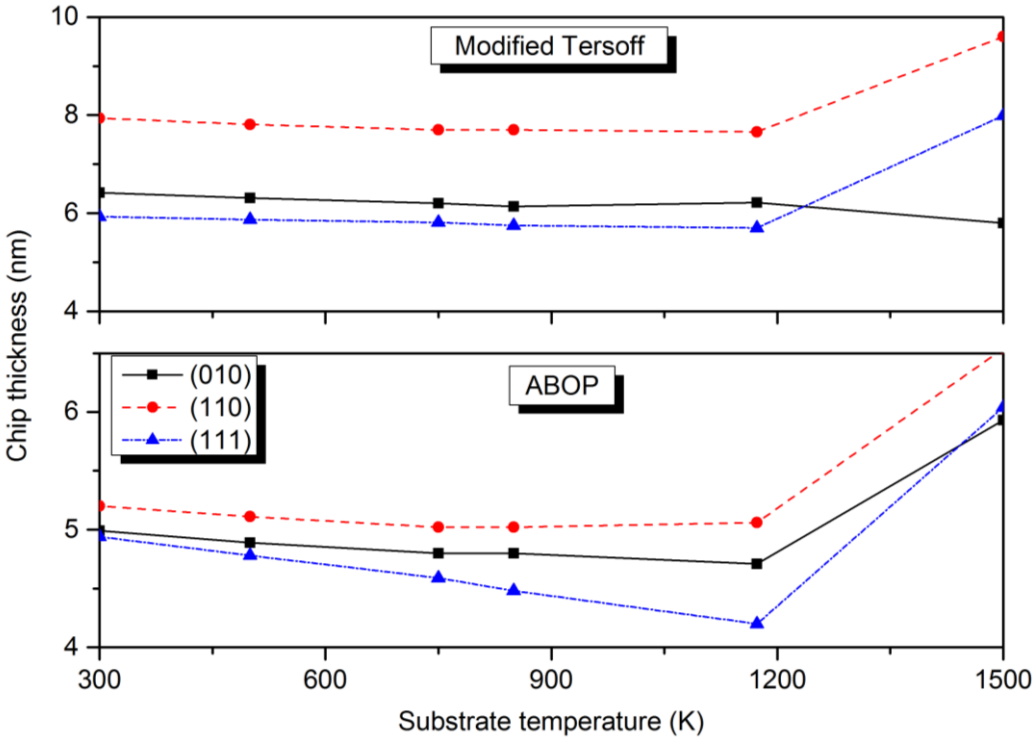


Fig. 6. Variations of the chip thickness while cutting silicon on different crystallographic planes at various temperatures obtained by modified Tersoff and ABOP potential functions

The chip ratio is regarded as a measure of plastic deformation and indeed it is a beneficial gauge to indicate machinability characteristics of the substrate, signifying energy consumed in nanometric cutting on plastic deformation. A large magnitude of chip ratio implies less thickening of the cutting chip thus smaller degree of deformation occurs during chip formation. This suggests that less force or energy is required to cut the substrate. It is observed from Fig. 7 that, in general, the chip ratio increases with the increase of temperature of the substrate, suggesting that the machinability of the substrate improves at higher temperatures. More apparent rise of the chip ratio is observed in Fig. 7 when the ABOP potential function is used. As mentioned before, due to more pile-up of atoms at higher temperatures, viz. 1500 K, the chip ratio decreases at these temperatures. The same scenario observed in the previous section is seen for the chip ratio modelled by the modified Tersoff potential.

The variation of number of the atoms in the chip with the temperature is demonstrated in Fig.

8, where the number of atoms in the chip increases up to ~1200 K while cutting silicon on the (010) and (110) planes. However, when nanometric cutting is performed on the (111) plane, the number of atoms in the chip increases constantly up to 1500 K. Such trend is observed for both employed potential functions. More importantly, using both potential functions, increase of the subsurface deformation layer depth is observed during cutting at higher temperatures, as demonstrated in Fig. 9. The key information from this analysis is that hot machining comes at an expense of relative increase in the subsurface deformation.

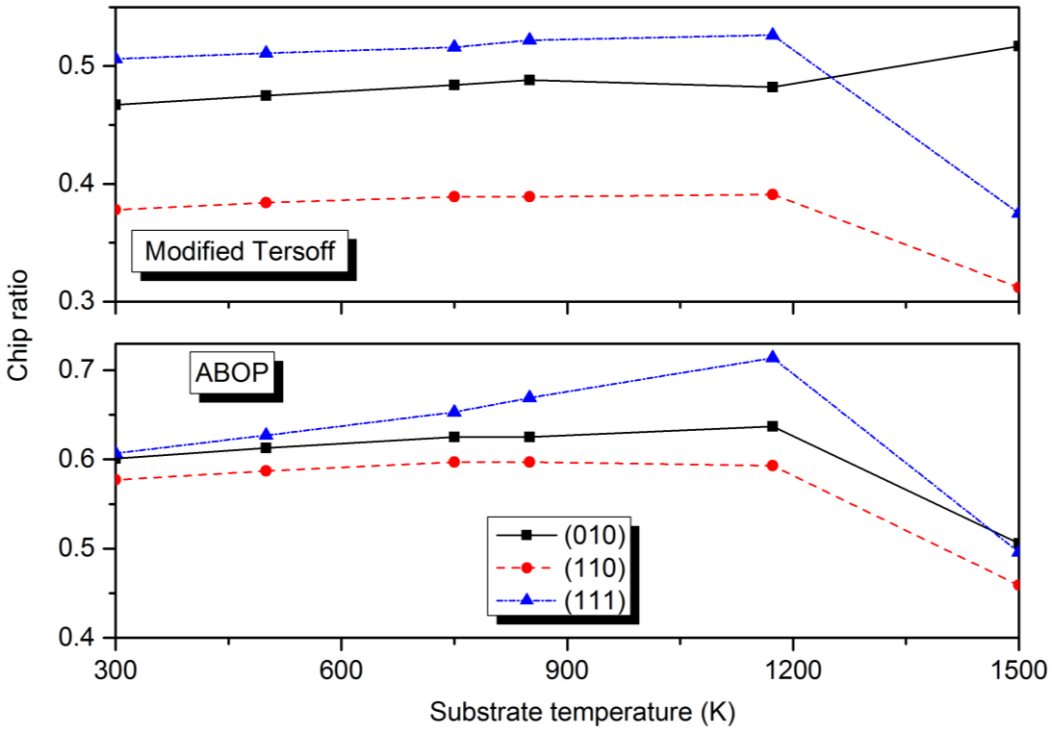


Fig. 7. Variations of the chip ratio while cutting silicon on different crystallographic planes at various temperatures obtained by the modified Tersoff and ABOP potential functions

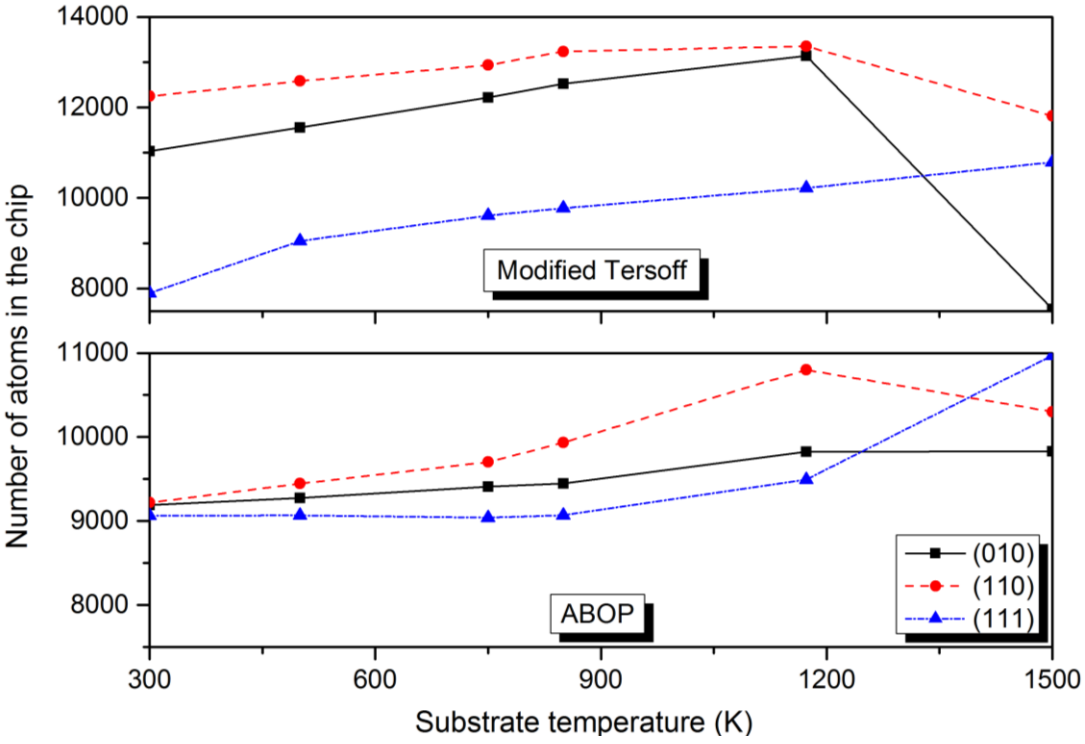


Fig. 8. Number of atoms in the cutting chip as a function of temperature and crystal orientation obtained by the modified Tersoff and ABOP potential functions

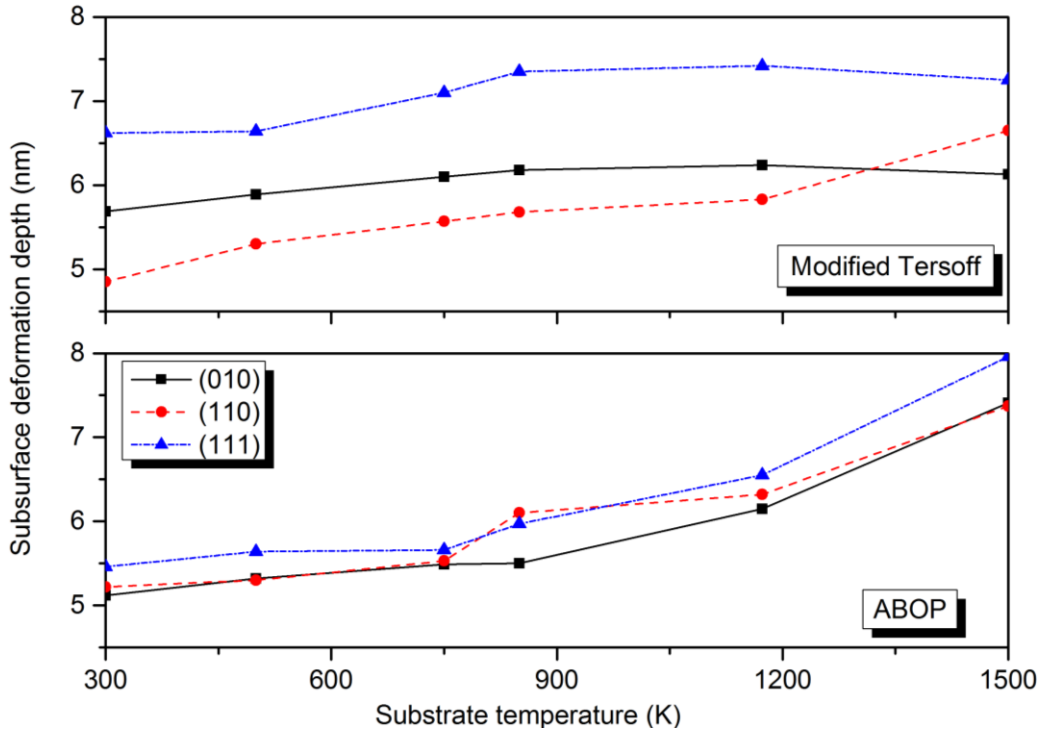


Fig. 9. Increase of the subsurface deformation layer depth with temperature on different crystal planes

Another light can be brought by the Figs. 6-9 is the variation of the aforementioned parameters on the different crystal planes. Single crystal silicon is highly anisotropic in its physical and mechanical properties. Hence, the aforementioned parameters are influenced by the crystallographic microstructure of the substrate. Irrespective to the machining temperature, the largest chip ratio is found on the (111) orientation while the smallest value appears on the (110) surface. It indicates that machinability is higher when nanometric cutting of silicon is performed on the (111) crystal plane. Thus, the (111) crystal plane can be considered as the easy cutting orientation whereas the (110) surface is the difficult to cut crystalline orientation. However, Fig. 7 shows some inconsistencies at temperatures higher than ~1200 K when the modified Tersoff potential is used.

Regardless of the temperature of the substrate, the maximum number of atoms in the chip was found while cutting silicon on the (110) surface, whereas the minimum number was observed on the (111) crystal plane. This observation may be closely related to the position of the stagnation region during cutting on different crystal planes. Our previous study [15] showed that when cutting of silicon is carried out on the (111) crystal plane, the stagnation region (shown in Fig. 2) is located upper (from the bottom of the tool) than those on the other crystal planes. For instance, when cutting was performed on the (111) crystal plane at 750 K, the stagnation region was positioned at 0.5-0.7 nm from the bottom of the tool as opposed to 0.2-0.4 nm for the (110) plane. This fact suggests that more atoms are compressed to the machined surface and less atoms flow upward on the rake face of the cutting tool to form the chips. This implies that ploughing due to compression is more pronounced on the (111) plane and thus a thicker subsurface deformation layer is generated, as demonstrated in Fig. 9. The converse scenario occurs when cutting is implemented on the (110) crystal plane of the substrate, where the stagnation region is placed at lower position leading to less ploughing action of the tool and, therefore, higher number of atoms in the cutting chip and reduced

subsurface deformation layer depth. However, there may be some other unidentified phenomena involved in the chip extrusion during nanometric cutting of silicon at room and at high temperatures since this process encompasses complex interplay among a multitude of various variables such as adhesive forces, interfacial energies, anisotropy, contact areas, number of dangling bonds dictating the nanoscale friction, etc.

3.3. Variation of forces and associates parameters exerted by the tool rake face on the chip

A quantitative analysis of the forces acting on the chip, rake face/chip friction, shear plane angle, chip velocity and temperature will help obtain better appreciation of the mechanism of chip formation and chip morphology in hot nanometric cutting of silicon. The tangential force (F_t), normal force (F_n) and resultant force (R) exerted by the rake face on the chip can be calculated by:

$$F_t = F_x \times \tan(\alpha) + F_y \tag{1}$$

$$F_n = F_x - F_y \times \tan(\alpha) \tag{2}$$

$$R = \sqrt{{F_t}^2 + {F_n}^2} \tag{3}$$

where F_x is the tangential cutting force, F_y is the thrust force and α is the tool rake angle (shown in Fig. 2). Accordingly, the tool rake face/chip friction coefficient can be obtained by:

$$\mu = \frac{F_t}{F_n} \tag{4}$$

In ductile mode cutting, the value of the shear plane angle characterizes the machinability of the substrate material. The shear plane angle describes the position of the primary shear zone with respect to the horizontal, as demonstrated in Fig. 2. Thus, it is beneficial to assess this parameter during nanometric cutting. Shear plane angle (φ) can be calculated using the following equation:

$$\varphi = tan^{-1}\left(\frac{r\times\cos(\alpha)}{1-r\times\sin(\alpha)}\right) \tag{5}$$

where r is the chip ratio [20]. Table 1B in Appendix B lists the magnitude of the above-mentioned parameters obtained from the simulation data in all the test cases at varying temperatures and crystallographic planes. As shown elsewhere [19] the ABOP potential energy function is robust in predicting forces and fracture stress of silicon. Therefore, the following analysis is carried out based on the results obtained by the ABOP potential. It should be noted here that the average values of the tangential cutting forces and thrust forces were calculated after the tool penetrated in the substrate by 15 to 25 nm. As a result of thermal softening, the magnitudes of the forces exerted by the tool rake face on the chip were observed to decrease with the increase of temperature of the substrate for all the crystallographic planes. Particularly, the resultant force was found to decrease by 24 % when cutting the (111) surface at 1173 K compared to that at room temperature. More importantly, as evidence in Fig. 10, the magnitudes of resultant force and friction coefficient at the rake face/chip interface were found to be smallest while cutting silicon on its (111) crystal plane, whereas they were largest on the (110) orientation. It is documented that the slip in diamond cubic lattice is analogous to FCC crystals and occurs preferentially on the (111) slip planes, meaning thereby that the (111) orientation should lead to low resultant force. A more detailed analysis, shown in Fig. 11, revealed that the minimum chip temperature is found on the (111) crystal plane while the maximum chip temperature appears on the (110) surface, which is in agreement with the above-mentioned results. It can be also inferred that lower values of friction could lead to lower chip temperature while cutting the (111) crystal plane. In addition, more friction at the tool rake face/chip interface may play a role in forming thicker chips on the (110) orientations, where the chip atoms cannot simply slide over the atoms of tool rake fake, resulting in more piling up of the cutting chip atoms. Accordingly, thicker cutting chips are observed while cutting silicon on the (110) plane, and contrarily, thinner ones on the (111) surface.

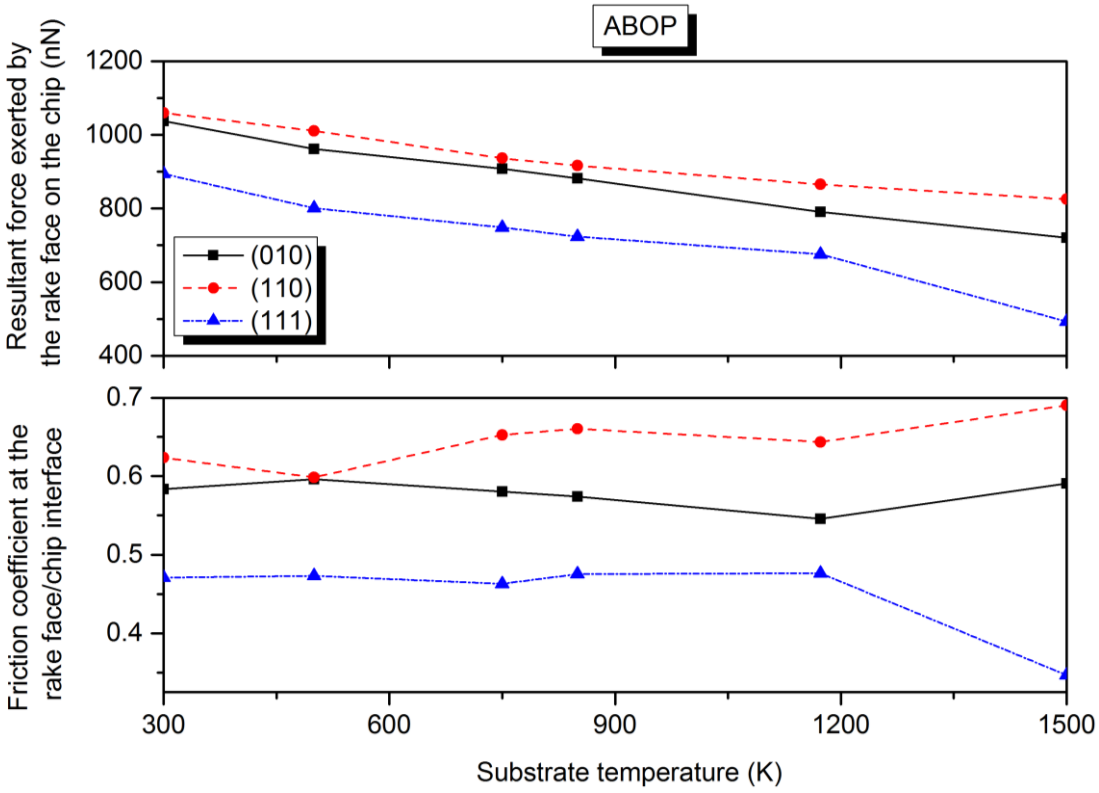


Fig. 10. Variations of the resultant force exerted by the tool rake face on the chip, and friction coefficient at the tool rake face/chip interface while cutting silicon on different crystallographic planes at various temperatures obtained by ABOP potential function

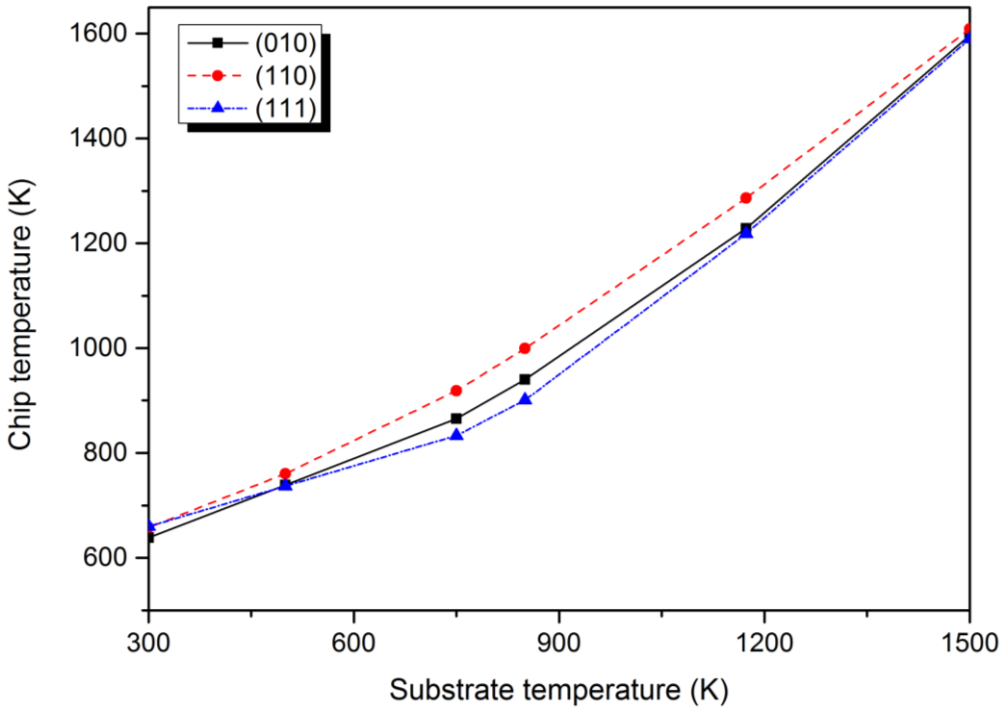


Fig. 11. Chip temperature as a function of substrate temperature and crystal surface

The chip velocity in nanometric cutting is defined as the velocity of the chip relative to the tool and directed along the tool rake face. As the chip velocity is a function of the chip ratio, r, ($V_{chip} = r \times V_{cutting}$), $V_{cutting}$ is the cutting speed, thus it increases with the increase of the temperature of the substrate, and follow the same trend observed in Fig. 7. In addition, the highest chip velocity is observed on the (111) crystal plane while the lowest chip velocity appears on the (110) surface. It is worth pointing out that less friction on the (111) surface could facilitate the sliding up motion of the atoms on the tool rake face, leading to higher chip velocity on this crystallographic plane.

As noted earlier, the shear plane angle is known as one of the important parameters to determine the machinability of materials. This angle can vary over a fairly wide range, depending on the conditions existing during cutting. Increase of the shear plane angle with the temperature of the substrate can be seen up to ~1200 K in Fig. 12. As observed before, the modified Tersoff shows almost the same trend like ABOP, yet the shear plane angle demonstrates slightly different pattern on the (010) plane. Higher magnitudes of shear plane angle correspond to the smaller shear plane area, implying that shear takes place in a more confined area culminating in lowering shear forces, and in turn, lowering the cutting forces. However, once again, some inconsistency can be seen at high temperature of 1500 K. Smaller shear plane angle is observed when hot nanometric cutting is carried out on the (110) crystal plane, signifying that higher shear forces are required to form the chip on this crystal surface. Hence, the (110) plane once again can be regarded as the difficult to cut orientation. On the contrary, larger shear plane angle is witnessed while cutting silicon on the (111) crystal plane, manifesting higher machinability which confirms that (111)<$\bar{1}$10> crystal setup is the easy cutting direction, in agreement with the experimental results [21-22].

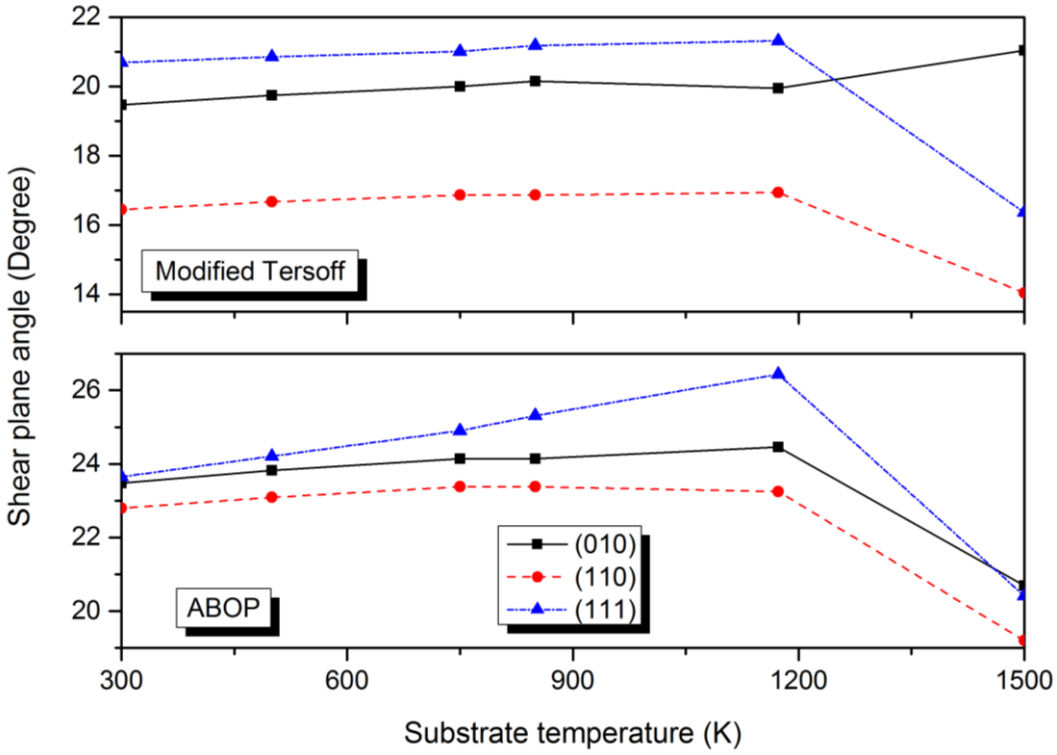


Fig. 12. Variations of the shear plane angle while cutting silicon on different crystallographic planes at various temperatures obtained by modified Tersoff and ABOP potential functions

3.4. Extent of temperature increase during the chip formation process

Chip formation process in nanometric cutting is driven by the plastic deformation mainly occurring in the primary deformation zone. Successive bond breaking and bond reforming will take place in the primary deformation zone leading to energy release and generation of thermal energy (heat). The bulk of the generated heat is dissipated into the chip thus the chip carries a great amount of heat during its separation from the substrate. In order to study the heat generated during the chip formation process and the extent of temperature increase (due to the generated heat) from the initial substrate temperature, a volume of material (1×1.5×3 nm^3 ~ 210 atoms), shown in Fig. 2, was considered in the deformation zone and the variations of the temperature were monitored on this volume. As seen in Fig. 13, the amount

of temperature increase from the initial substrate temperature decreases with the increase of the temperature of substrate, signifying less release of thermal energy during the deformation phase at higher temperatures due to weaker bonding between atoms. Also, the maximum and minimum thermal energy are found on the (110) and (111) crystal planes, respectively. The generated heat in the deformation zone during the chip formation process is transferred to the chip, leading to the higher and lower local temperatures on the (110) and (111) orientations, respectively, which is analogous to the already observed behaviour in the chip temperature shown in Fig. 11.

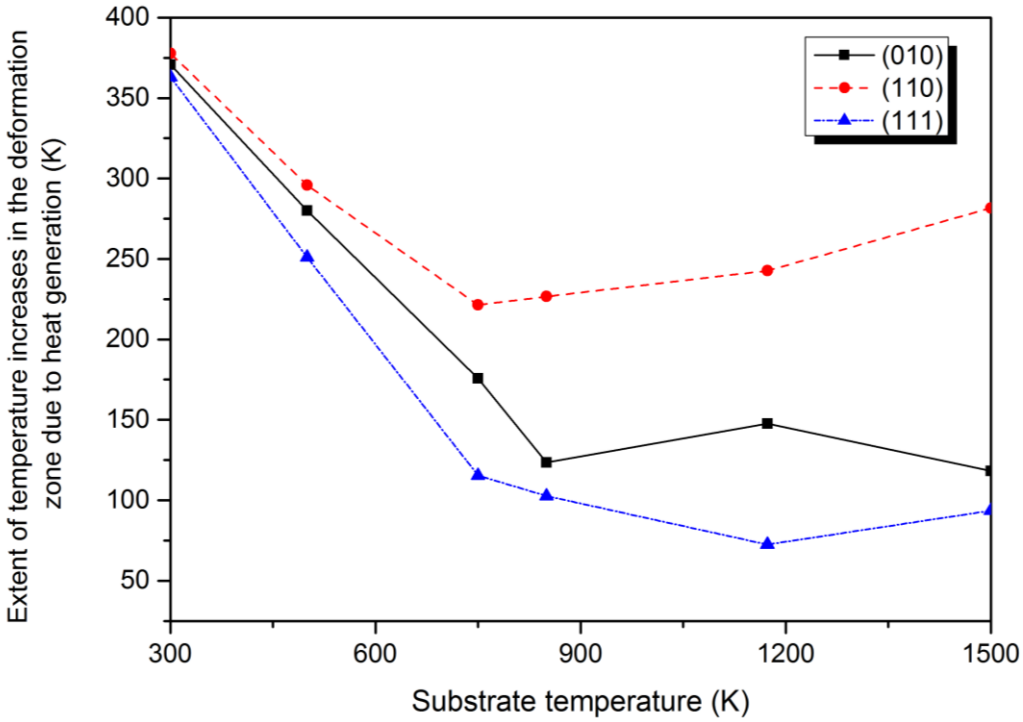


Fig. 13. Extent of temperature increase in the deformation zone during chip formation while cutting silicon on various crystal planes and at different temperatures

4. Conclusions

Nanometric cutting of silicon workpiece at a wide range of temperatures was investigated in

this paper using MD simulation with two potential energy functions namely the ABOP and the modified Tersoff, to provide a superior understanding of chip formation mechanism and chip morphology in this process. The findings are summarised as follows:

1. Thinner and taller chips, and greater chip ratio were observed to form when nanometric cutting is implemented at higher temperatures or on the (111) crystal plane of silicon substrate.
2. The depth of deformation layer in the silicon substrate was noticed to become greater under high temperature conditions.
3. More atoms in the cutting chip and reduced subsurface deformation layer depth was observed while cutting the (110) crystal plane, attributable to the lower position of stagnation region which causes less ploughing action of the cutting tool.
4. Using the modified Tersoff potential function, the chip velocity angle was observed to experience a sudden drop near the melting point temperature (1500 K) of silicon while the ABOP did not show such behavior. Further analysis through calculation of the phase instability and melting temperatures of silicon demonstrated that the ABOP predicts aforementioned parameters much higher than those of the modified Tersoff potential.
5. The magnitudes of the forces exerted by the tool rake face on the cutting chip decreased with the increase of the temperature of substrate for the crystallographic planes studied. Moreover, the minimum resultant force and friction coefficient at the tool rake face/chip interface were found when cutting the (111) crystal plane, whereas they reached their maximum value when cutting the (110) plane, which confirmed that the mentioned surfaces are the easy and difficult-to-cut surfaces, respectively. Also, the lowest chip velocity and chip temperature were observed when using the (111) surface.

6. Higher magnitudes of shear plane angle were observed while cutting the (111) plane of the silicon workpiece or at higher temperatures. It signifies a smaller shear plane area, implying that shear took place in a more confined area culminating in lower shear forces.
7. Lower thermal energy and in turn smaller extent of temperature increase (due to the generated heat) in the deformation zone were noticed while cutting silicon on the (111) plane or at high temperatures.

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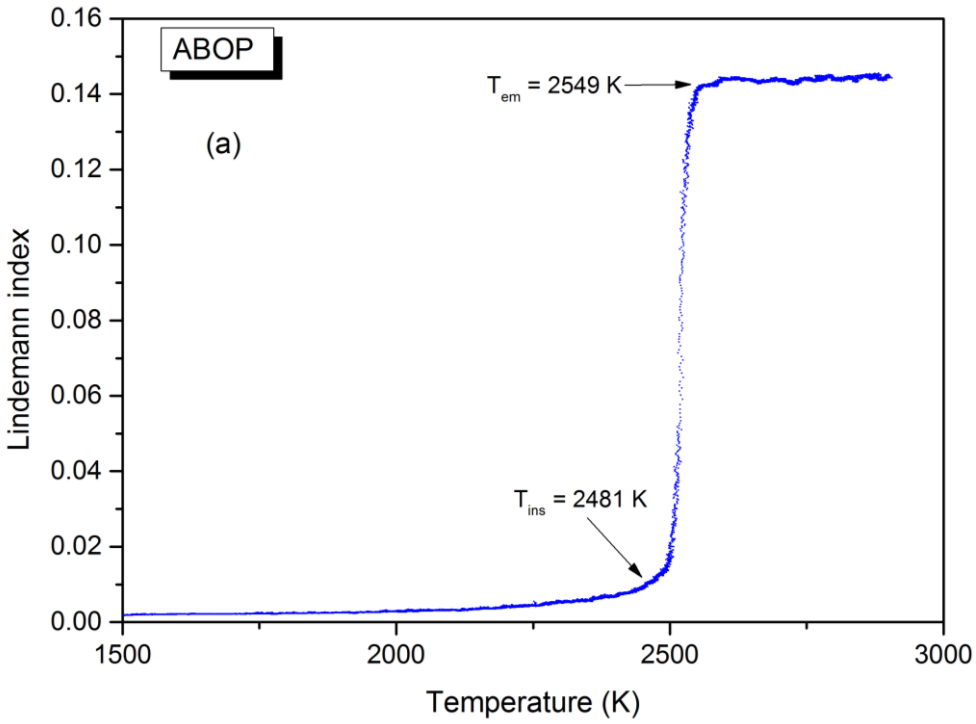
Appendix A

In order to calculate the melting point of silicon by the ABOP and modified Tersoff interatomic potentials, first, a rough estimation was carried out using the one-phase method. Accordingly, a $15 \times 15 \times 15$ supercell of silicon containing 27,000 atoms was heated up under the NVT ensemble. Reflective boundaries and low heating rate of $9 \times 10^9 K/s$ were adopted in order to avoid the hysteresis phenomenon and superheating [23-24]. The phase instability temperature (T_{inst}) was observed at 2481 K and 1397 K, respectively, for the ABOP and the modified Tersoff potentials, where the Lindemann index [25] experienced an upward

jump, as indicated in Fig. 1A. Due to the alteration of the atomic bonding of silicon from the covalent bond to metallic bond upon melting, atomic volume shrinkage (calculated using Voronoi tessellation [26]) equal to ~10.1% and ~9.2% was noticed when using the ABOP and the modified Tersoff potential functions, respectively, which are consistent with the reported experimental values [27-28]. The entirely molten temperature (T_{em}) was calculated to be 2549 K and 1616 K, when using the ABOP and modified Tersoff potential functions, respectively.



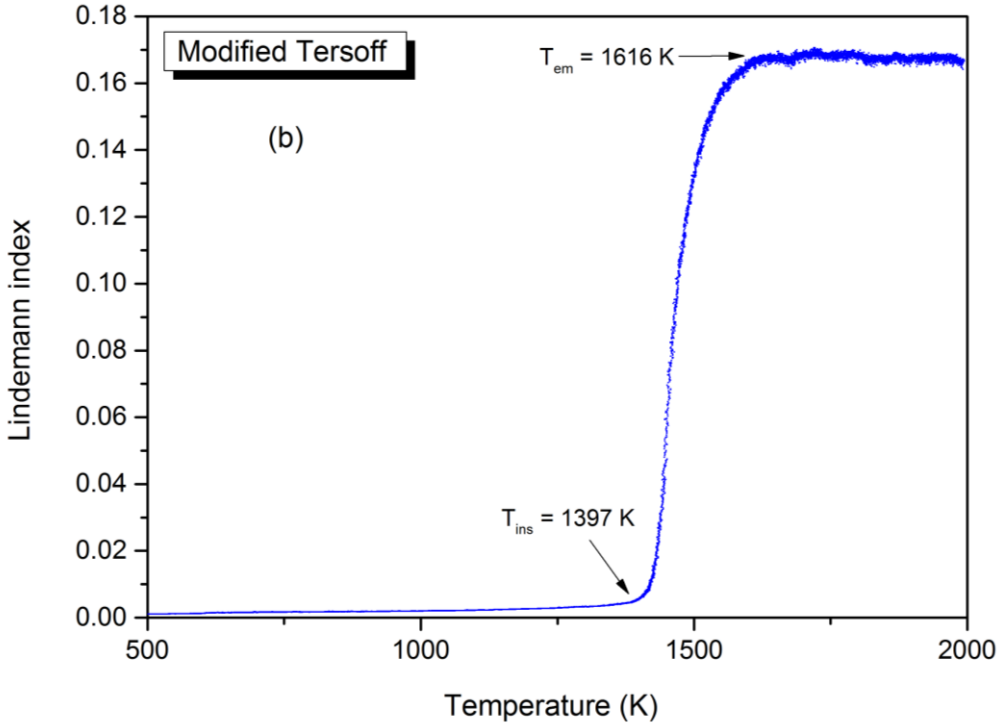


Fig. 1A. Variation of the Lindemann index upon incremental heating. T_{inst} corresponds to the phase instability temperature while T_{em} stands for the entirely molten temperature.

Appendix B

Table 1B. Forces, friction, shear plane angle, chip velocity and chip temperature while cutting silicon on different crystallographic orientations at various temperatures obtained by the ABOP potential function

Temperature of the substrate (K)	Crystal orientation	Tangential force (*F*) exerted by the rake face on chip (nN)	Normal force (*N*) exerted by the rake face on	Resultant force (R) exerted by the rake face on chip (nN)	Friction coefficient at the rake face/chip interface	Shear plane angle (°)	Chip velocity (m/s)	Chip temperature (K)

			chip (nN)					
300	(010)	523.01	896.37	1037.8	0.5835	23.48	30.05	638.7
	(110)	560.52	898.98	1059.41	0.6235	22.8	28.85	657.7
	(111)	380.86	808.71	893.9	0.4709	23.65	30.35	659.7
500	(010)	492.29	825.59	961.22	0.5963	23.82	30.65	738.9
	(110)	519.07	867.43	1010.87	0.5984	23.09	29.35	760.6
	(111)	342.59	724.18	801.13	0.4731	24.21	31.35	736.9
750	(010)	455.81	785.25	907.95	0.5804	24.14	31.25	865.3
	(110)	511.66	784.12	936.29	0.6525	23.38	29.85	918.8
	(111)	314.38	679.18	748.41	0.4629	24.9	32.65	833.1
850	(010)	438.79	764.58	881.54	0.5739	24.14	31.25	940
	(110)	504.76	764.46	916.07	0.6603	23.38	29.85	999.3
	(111)	310.75	653.55	723.66	0.4754	25.31	33.45	900.7
	(010)	378.85	694.38	791.01	0.5456	24.4	31.85	1228.6

1173						6		
	(110)	468.13	727.47	865.08	0.6435	23.25	29.65	1286.2
	(111)	290.6	609.92	675.61	0.4764	26.44	35.7	1218.3
1500	(010)	366.47	620.32	720.48	0.5908	20.69	25.3	1596.4
	(110)	468.64	678.72	824.79	0.6905	19.2	22.95	1608.9
	(111)	161.53	465.97	493.17	0.3466	20.41	24.8	1589.7

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