Turboelectric Distributed Propulsion Protection System Design Trades

C. Ross*, M. Armstrong*, M. Blackwelder*, C.Jones[+], P. Norman[+], S. Fletcher[+]

*Rolls-Royce North American Technologies Inc., +University of Strathclyde

Abstract

The Turboelectric Distributed Propulsion (TeDP) concept uses gas turbine engines as prime movers for generators whose electrical power is used to drive motors and propulsors. For this NASA N3-X study, the motors, generators, and DC transmission lines are superconducting, and the power electronics and circuit breakers are cryogenic to maximize efficiency and increase power density of all associated components. Some of the protection challenges of a superconducting DC network are discussed such as low natural damping, superconducting and quenched states, and fast fault response time. For a given TeDP electrical system architecture with fixed power ratings, solid-state circuit breakers combined with superconducting fault-current limiters are examined with current-source control to limit and interrupt the fault current. To estimate the protection system weight and losses, scalable models of cryogenic bidirectional current-source converters, cryogenic bidirectional IGBT solid-state circuit breakers (CBs), and resistive-type superconducting fault current limiters (SFCLs) are developed to assess how the weight and losses of these components vary as a function of nominal voltage and current and fault current ratings. The scalable models are used to assess the protection system weight for several trade-offs. System studies include the trade-off in fault-current limiting capability of SFCLs on CB mass, alongside the fault-current limiting capability of the converter and its impact on CB fault-current interruption ratings and weight.

Introduction

The NASA N3-X blended-wing body with turboelectric distributed propulsion (TeDP) concept is being studied to achieve N+3 goals such as reduced noise, NOx emissions, and improved energy efficiency. In contrast to conventional podded propulsion aircraft which purposefully segregate the propulsive and lift production functions in the aircraft, TeDP utilizes thrust production as an augmentation to the aerodynamic performance of the vehicle (i.e., boundary layer ingestion, higher bypass ratio, and reduction of drag) [1,2]. The gas turbine engines are used to provide rotational energy to generators which convert this energy to electrical. The electrical power output of the generators is rectified and distributed as a DC system to an array of propulsor motors. Each motor has its own inverter to permit motor speed to be independent of generator speed and to eliminate the risk of loss of synchronization. Between the generator and motor windings, the electrical power system is cryogenic, while the transmission lines are superconducting in order to maximize their efficiency and increase the power density of all associated components [3,4]. Figure 1 illustrates an example TeDP architecture that is being studied that includes fault detection, protection, isolation, and redundancy. This example includes two engines, each powering two generators. Each generator feeds a DC bus with four propulsor motors. Each propulsor motor is cross tied to a second generator to provide redundancy, improve reliability, and reduce propulsor motor power ratings. Figure 2 shows an example physical schematic of the TeDP architecture on a blended-wing body aircraft. The cable length between each of the rectifiers and inverters may reach 30 m, while the distance between the inverters and motors may be as long as 10 m.
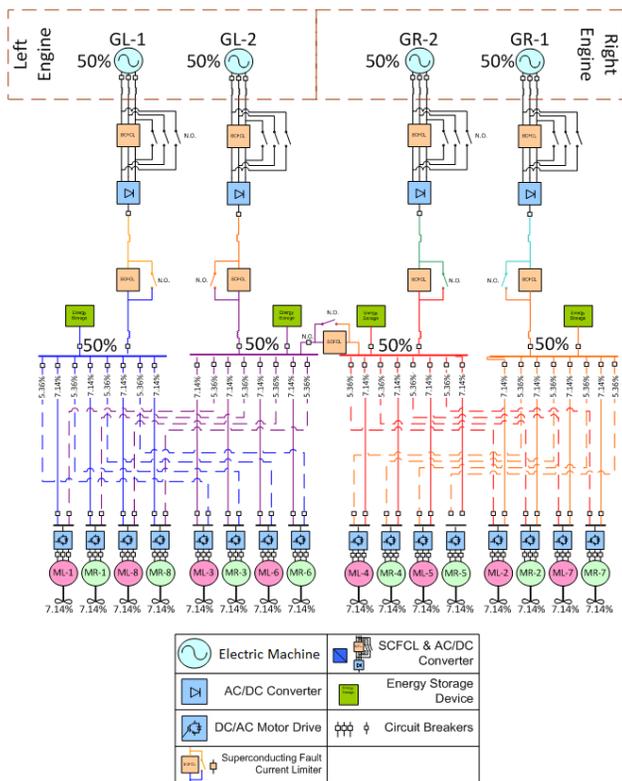
Figure 1. Four-bus inner bus tie multi-feeder TeDP architecture design with 16 propulsors
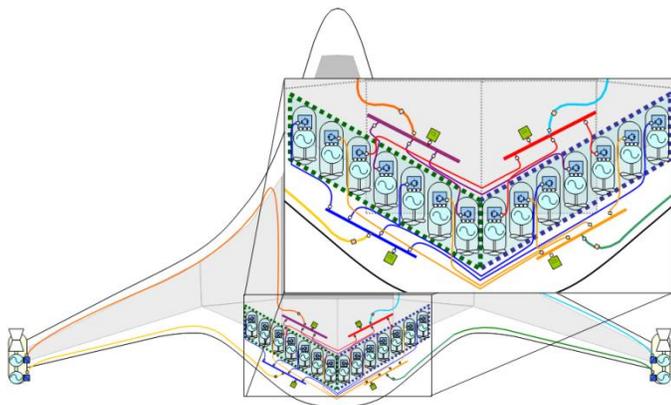

Figure 2. Example TeDP physical schematic with blended-wing body aircraft

The protection of a superconducting DC network poses unique electrical and thermal challenges due to low impedance of the superconductor, operation in the superconducting or quenched states, and weight and efficiency constraints. Due to the low impedance of superconducting components, the time from the initiation of the fault to the peak fault current may be on the order of tens to hundreds of microseconds [5]. The architecture can be designed to withstand this peak current and not quench, or the protection system can include fault tolerance and allow individual component quenches and

recovery in the trade between fault current and protection time versus weight.

In this paper, protection strategies are investigated for the weight critical TeDP electrical system architecture with fixed power ratings, including a general discussion of conventional and superconducting DC protection challenges. Solid-state circuit breakers (SSCBs) including cryogenic operation of IGTBs are analyzed and assessed with the inclusion of superconducting fault-current limiters (SFCLs) and unidirectional or bidirectional current-source converters.

Conventional DC System Protection Challenges

Several challenges surrounding the development of an adequate protection strategy for a DC network have been identified. The nature of these challenges is linked closely to whether the type of converter used is a voltage source converter (VSC) or a current source converter (CSC).

Conventional DC System Protection with a VSC Interfaced Network.

A DC system with a VSC will have a capacitive filter on the DC link to minimize voltage ripple and hold the DC link voltage constant. If a VSC is used with a high capacitance (in the order of millifarads), then it is well documented in the literature [5,6] that high currents will flow in response to a short circuit fault. Figure 3 shows the initial response to a short circuit fault [6]. It is dominated by the discharge from filter capacitors which result in a very high rate of change of current with time (di/dt), a high peak current and a rapid decay in system voltage [6,11].

The initial response of the DC system to the fault is very dependent on line length, as this affects the amount of damping within the system. In the case of DC networks on aircraft, the typically short line lengths in these electrical architectures result in a very underdamped response. The consequence of this is a more rapid development of fault current, with fault current reaching a peak much faster than in a critically or overdamped system. As an example, fault current will develop around 3 times faster in an aircraft electrical system with relatively short line lengths, compared to a typical DC microgrid [6]. Clearly this will result in a high initial di/dt.

The high initial fault current may result in a risk of damage to sensitive components which are in the fault current path or to the capacitors [6]. There is then a much lower, sustained fault current contribution from the VSC. The combination of these two contributions to the fault current can create difficulties in the coordination of protection devices.
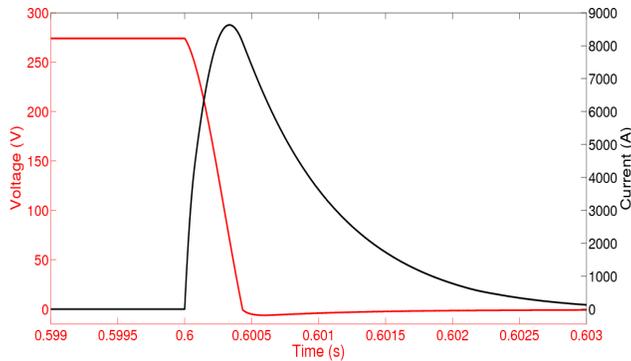
Figure 3. Fault response on a DC bus with a VSC

Following on from this initial high fault current, there are two subsequent system effects which could cause issues for the protection of conventional DC networks [6]. Firstly the voltage on the DC link will drop due to the discharging of the DC link capacitor [6]. If the under voltage protection trips, then this may lead to a propagation of the effects of the fault. Secondly, there will be voltage oscillations due to the inductance and capacitance in the system. These oscillations may result in a negative voltage across the DC link capacitor, which leads to currents flowing in the antiparallel diodes in the converter. These currents may damage the diodes.

A second challenge surrounding the response to a DC fault is that it can be difficult to detect and discriminate faults on a DC network [7]. For example, the converter topology used in a DC system architecture can either have a high or low capacitance filter and either be a current limiting or non-current limiting topology [7]. If the converter filter has a high capacitance, then in response to a fault, there will be an initial high peak current, as the capacitor discharges followed by a sustained fault current. It is difficult to coordinate a protection system to discriminate between these two current levels. However, if the converter is current limited and has a low filter capacitance, then there is no fault current source. In this scenario, it is difficult to detect and determine the location of a fault. If a fault is not detected and protection activated quickly enough, then unacceptable consequences of the fault will occur. These include converter voltage reversal and over voltage transients.

Another type of fault that induces undesired heat generation is DC partial discharge due to voids or contaminates in the dielectric layer of the distribution cable. Partial discharges are small discharges of pico to nanocoulombs of charge. The resulting current would not exceed the circuit protection fault current magnitude and is difficult to detect. Other difficult to detect faults include a partial, or soft, fault between DC poles. The current may be well within the circuit protection current limits, yet generate damaging localized heating. Alternate sensing technologies would be required to detect these types of faults due to their insidious nature from the conventional fault detection perspective.

Conventional DC System Protection with a CSC Interfaced Network

The use of a CSC may overcome some of the challenges presented by using a VSC. A CSC is inherently tolerant to a short circuit DC fault [8] for two reasons. Firstly, the CSC has bidirectional voltage blocking capability. Secondly, the DC link inductive filter significantly reduces the peak fault current and the fault current rise time is close to a magnitude of time difference slower than if a VSC with a capacitive DC link filter is used [6,8]. Recent VSC topologies have been developed which do have fault current blocking capability [9]. However these are multilevel VSC topologies, which were not considered for the protection trades performed. It should be noted, however, that while a CSC may appear to be more fault tolerant than a VSC, for an aerospace application where weight and volume are important, it may not be the preferred solution. In addition, the large filter inductance may introduce challenging post-fault transients.

Superconducting DC Protection Challenges

The negligible resistance in a DC superconducting network results in a system with very little natural damping. As a result faults will propagate rapidly through a system, presenting challenging fault detection requirements and careful thought on how to approach protection co-ordination [5].

Due to the low damping in a superconducting network, the switching of circuit breakers will trigger high frequency oscillations between inductances and capacitances in the system. It has been proposed by Cuzner and Venkataramanan [6] that the control algorithm used for converter control could be used to introduce damping into the system. This would be possible as the DC filter components will keep the frequencies low enough that the converter control will have a suitably fast response.

The second additional protection challenge identified for a superconducting network is the possible quenching of the cables. The impact of this on the system dynamics must be considered. Quenching of a cable will occur if the temperature, current or magnetic field rises above critical levels. For example, if a fault occurs and the current level exceeds the critical current level, the system will quench.

A key decision which must be made in the development of a protection system for a superconducting network is whether it is acceptable to allow the system to quench in response to a fault, or if the system should be designed and operated so that it does not quench. If the system is allowed to quench, then the extra damping provided by the line resistance will reduce the peak fault current. However, a quench results in local heating region which may increase the risk of damaging equipment. Individual coil protection strategies include cold diodes to protect several coils in series so that each coil absorbs its own energy or an active system with heaters or resistor switch.

If the protection approach taken is to not allow the system to quench in response to a fault, then the protection must be able to respond fast enough to isolate a fault before the fault current exceeds the critical current level. To achieve this, careful design and co-ordination of the protection system is required.

Protection Options: Fault Tolerance, Fault-Current Limiting and Response Time, and Devices

Three different protection strategies to overcome these challenges have been identified by the authors: to increase component robustness and fault tolerance, to suppress fault effects through current limiting, and the mitigation of fault effects through fast protection operation. A combination of two or more of the protection strategies presented may be required.

The converter can be designed in such a way to be less susceptible to the effects of a fault on the network. For example, a faulted section of network can be isolated from the rest of the network using the converter to provide isolation [11].

An advantage of a CSC topology is that it provides fault current blocking capability. However there is a trade-off between this inherent capability and the weight and volume of the inductive filter which a CSC requires.

A full bridge VSC can be implemented in this way to limit and interrupt fault current from a DC side fault. If a VSC was intended to perform this protection role, then the filter capacitors on the DC link would require snubber protection to reduce the di/dt experienced by the capacitor in the event of a DC bus bar fault [12].

An important consideration is whether using the isolation properties of converters provides sufficient protection in a superconducting network. If it is not sufficient, then additional protection is required. While the converters will block fault current and isolate the fault from the rest of the system, the faulted DC network may quench due to the initial high fault current [8].

Fast acting protection can also be used to mitigate against the fault effects through the implementation of fast-acting circuit breakers. The circuit breakers chosen must be able to respond quickly enough to the rapidly rising fault current firstly to protect the converters from reverse currents flowing in the diodes, and the protection against undervoltage on the DC link. Secondly, the circuit breakers must respond quickly to prevent system quench. It is clear from discussions presented in [6] that solid state circuit breakers (SSCB) are able to respond quickly enough to a fault in a superconducting network.

A superconducting fault current limiter (SFCL) can be implemented to suppress fault currents. However, for moderate critical current margins, the response time of a resistive-type SFCL can be much slower than an SSCB [13]. The operating time of an SFCL depends on the relative magnitude of the fault and nominal currents. As such resistance increases occur on

the order of around 1 to 10 ms [13] while SSCB operate on the order of microseconds [14]. A key advantage of the SFCL is that it is not only a robust technology due to its low complexity, but that is also lightweight when no transition to normally conducting equipment is required. Therefore it is suited to high power dense applications, such as aircraft electrical systems.

Protection System Trade Studies

Overview of Protection Device Sensitivity Models

For the TeDP architecture, several devices were identified as protection devices, and a scalable model of each of those devices was developed in order to derive component and system mass and efficiency sensitivities to voltage, current, temperature, and other parameters. These scalable models also enable protection system studies and sensitivity analysis. For this architecture, sensitivity models of the current-source converter, (unidirectional or bidirectional), solid-state circuit breaker, and superconducting fault-current limiter were developed. The following sections describe the assumptions and trends used to create the scalable models.

CSC Sensitivity Model

The CSC mass, efficiency, and current interruption time are estimated based on the scalable model for specified power, voltage, AC frequency, and power factor ratings. Additional control parameters that also affect the scalable model estimates are the converter topology, switching frequency, DC ripple voltage, and DC ripple current.

For this study, the topology and switch type are fixed. The model of the mid-point clamped three-level current-source topology using IGBTs [8] was developed. This topology is shown in Figure 4. Depending on the switch module topology, the converter will have unidirectional or bidirectional conducting capability. The upper switch module shown in Figure 4 illustrates a half-bridge topology for unidirectional conducting, and the lower switch module is a full-bridge topology enabling the converter to conduct bidirectionally. For this TeDP architecture, the power converters that convert the generator AC voltage and current to DC are unidirectional and rated at a maximum power of 11.2 MW, which is the engine-out take-off propulsion power requirement. A subset of the power converters that convert the DC distribution voltage and current to AC to drive the propulsor motors are bidirectional and rated at a lower power (approximately 1.2 MW for a 16 propulsor architecture). The ability of those converters to conduct current bidirectionally allows the propulsor electric machines to also operate as generators in the case of windmilling and transfer that power to other loads or the energy storage device.
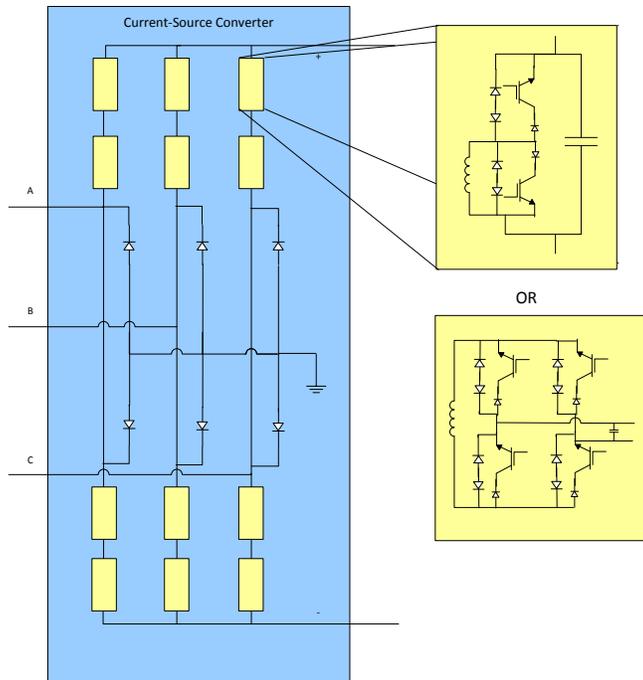
Figure 4. Current-source converter topology with unidirectional or bidirectional switch modules

From the overall converter voltage and current ratings, the subcomponent ratings are derived. Scalable models of the cryogenic subcomponents were developed. These devices include Insulated Gate Bipolar Transistors (IGBTs), diodes, capacitors, and inductors. For a specified voltage, current, and temperature, the subcomponent mass and loss are determined. Using the topology to determine the arrangement of these components, the sum of the component mass and loss estimates are used to estimate the total converter mass and losses.

The DC ripple voltage magnitude is used to determine the capacitance requirements to support the DC bus voltage, and the DC ripple current magnitude is used to determine the inductance requirements for each switching module. The capacitance requirement for the specific current-source converter topology is not analytically known, but it can be approximated using standard topology requirements. For a standard three-phase AC to two-level DC full-wave diode rectifier, the rectifier capacitance for voltage regulation is approximated by:

$$C_{eq} = \frac{I_{dc}}{2f_{ac}\Delta V_{dc}}$$

where I_{dc} is the rated DC current, f_{ac} is the AC frequency, and ΔV_{dc} is the peak-to-peak DC voltage ripple magnitude. Note that the CSC topology differs in that it is actively controlled with IGBTs and the DC side has three voltage levels (mid-point clamped), so this capacitance definition is approximate across the pole-to-pole DC bus. It is apparent from this equation that the AC frequency influences the capacitance; a higher AC frequency lowers the capacitance required for the same DC bus voltage ripple and DC bus current.

Based on this equivalent capacitance, the mass and losses of the capacitors are estimated. A model of a scalable cylindrical film-foil type capacitor with polypropylene dielectric was developed and used to estimate the capacitor mass and losses. Film capacitors are widely used as DC link capacitors and in IGBT snubbers. Therefore film capacitors have been used for this scalable power converter. Tests of this type of capacitor at 77 K environments [15,16] indicate that the capacitance is similar at room and 77 K temperatures while the capacitor equivalent-series resistance decreases by a factor of two at 77 K.

Similarly, the inductance requirement for this CSC topology to achieve a desired DC ripple current is not analytically known but can be approximated from standard topology theory. For the same full-wave diode rectifier with inductive filtering on the DC side, the DC ripple current is approximated by the following phasor equation at the ripple frequency $= 2\pi(2f_{ac})$ [17]:

$$\tilde{I}_{DC,ripple} = \frac{2\sqrt{2}V_{ac}}{3\pi(R + j\omega L - \omega^2 RLC)}$$

Where V_{ac} is the rated rms voltage, R is the DC pole-to-pole resistance, L is DC inductive filter, and C is the equivalent DC capacitive filter. This equation is adapted to the find the equivalent inductance for a specified DC current ripple by assuming that each arm for the three-phase AC side contributes to approximately one third of the total DC current ripple. With this assumption and using the quadratic formula, the arm equivalent inductance is computed.

Based on this equivalent inductance, the mass and losses of the inductors are estimated. The specified inductance, voltage, and current ratings are used by the inductor model to estimate the inductor mass and losses. The scalable inductor model used was similar to the SFCL inductive coil model. However, the main difference between the inductor and SFCLs models is that there is no quench state resistance for which the inductor is sized; the inductor is sized to meet the desired inductance only.

Scaling trends to approximate IGBT ratings were developed based on existing IGBTs and research results of the cryogenic application of IGBTs. The overall converter model specifies the cryogenic device nominal current and blocking voltage ratings. From these specifications, the IGBT mass, conduction voltage drop, turn-on and –off times, and turn-on and –off energies are estimated for the device at the specified device ratings. The IGBT power loss was calculated from the conduction and switching losses [18]. The existing IGBT ratings for ABB, Infineon, and Mitsubishi devices were tabulated, and trends from these devices were developed in order to develop a scalable IGBT within the current and voltage ratings of the known devices. Trends were developed for IGBTs with nominal current in the range of 200-1500 A and nominal blocking voltage in the range of 1.2-6.5 kV.

The cryogenic operation of the IGBTs and diodes is scaled from room temperature IGBT and diode data based on cryogenic testing and research of these devices [19,20,21]. Proportional scaling is used based on these results from tests conducted at temperatures ranging from 50 K to 300 K. The IGBT cryogenic scaling factors used in each of the models using this device is summarized below in Table 1. These scaling factors can be modified and adapted as functions of temperature or other variables to improve the model estimates. Further research and test results are necessary to better approximate the IGBT performance as a function of temperature, voltage, current, and other factors.

Table 1. IGBT Characteristic Scaling for Cryogenic Temperatures

IGBT Characteristic	Scaling Factor Cryo/Room Temp	Comments
Nominal Current (A)	1	
Over Current (A)	1	
Nominal Blocking Voltage (kV)	0.5	35-75% reduction at lower temperatures
Conduction Voltage Drop (V)	1	
Time to turn off (µs)	0.3	5-50% reduction at lower temperatures
Time to turn on (µs)	1	
Turn off energy (J)	0.25	20-33% reduction at lower temperatures
Turn on energy (J)	0.25	20-33% reduction at lower temperatures

The converter packaging mass estimates, which include the heat exchanger, housing, bus bars, and current sensors, are based on scaling of state-of-the-art power converters. Using data from [22,23], mass percentages of the packaging components were estimated. These percentages are summarized in Table 2. Using these percentages, the packing component masses are scaled according to the subtotal mass of the inductor, presspack diodes, and IGBT and series diodes as estimated by the model. More detailed models of these components could be described so that they are more independent of the IGBT and inductor scaling models, such as estimating the heat exchanger mass from the converter losses and thermal transfer capability.

The scalable power converter model can be exercised in numerous ways to estimate the power converter sensitivity to different variables. An example converter specific power sensitivity to DC voltage as computed by this scalable model for the described topology is illustrated in Figure 5.

As seen by the trends, the specific power trend generally increases for higher AC frequencies. Also, for a specific AC frequency, the specific power increases up to a certain DC voltage, then decreases for higher DC voltages. This trend is due in part to the capacitance and inductance requirements as the DC bus voltage varies and the AC frequency varies. The capacitance and inductance requirements are calculated based on the specified DC bus voltage and current percentage ripple which is fixed for each these trends. Generally, the lower the capacitance and inductance requirement, the lower

the mass of those components. In addition, higher AC frequencies reduce the filter capacitance and inductance requirements and thus capacitor and inductor mass. This explains the general increase in specific power for increased AC frequency. The nonlinear specific power trend for a specified AC frequency can be further explained by the capacitance and inductance requirements as DC bus voltage varies. These requirements for an example 400 Hz AC system are illustrated in Figure 6. Note that the capacitance and inductance requirements to meet specified DC voltage and current ripple requirements are a function of the AC electrical frequency. The combination of the minimum inductance and capacitance requirements at approximately 8 kV attributes to the peak total converter specific power at that approximate voltage. Other major contributors to the nonlinearity of the specific power trend are the IGBT and converter housing mass trends.

Table 2. Automotive inverter component mass percentages [23]

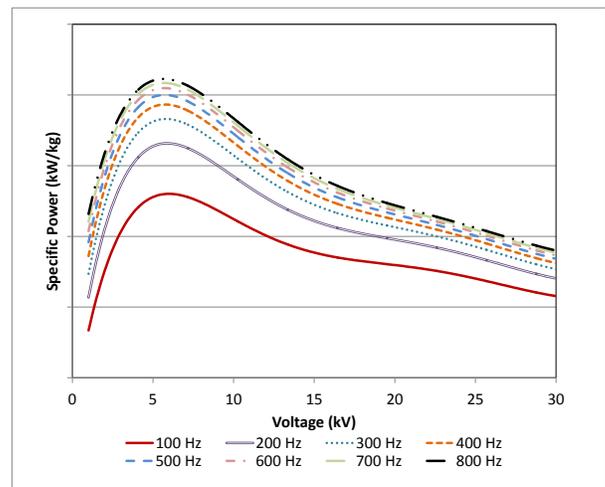| Component	Mass percentage
Heat exchanger	37%
Power modules, gate drivers, PWBs	23%
Housing	15%
Capacitors	12%
Bus bars	7%
Current sensors	6%

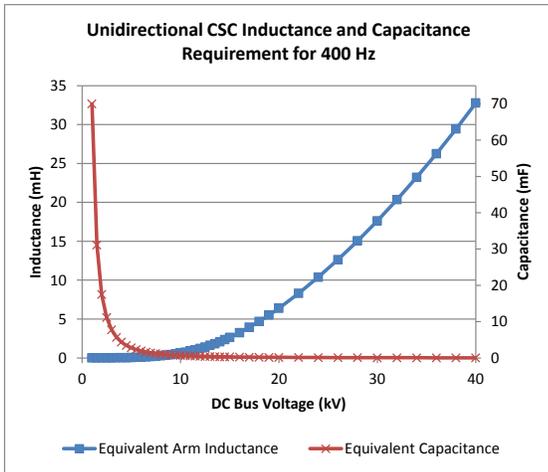Figure 5. Specific power vs DC voltage trends for 11.2 MW scalable CSC

Figure 6. Unidirectional CSC inductance and capacitance requirements for scalable 11.2 MW CSC model

SSCB Sensitivity Model

The SSCB model is structured similarly to the inverter and rectifier models. Given the specified rated power and DC voltage, the component voltage and current ratings are specified. From these component specifications, the component masses and losses are computed and totaled. The SSCB topology studied is illustrated in Figure 7. From this figure, the SSCB components are the conduction diodes, IGBTs with freewheeling diodes, and a metal oxide varistor (MOV). The MOV is used as an overvoltage protection device during switching events.   To explain the protective function of the MOV, consider the equation for the peak voltage across a circuit breaker [24]:

$$v_{CB\ peak} = v_C + \frac{Li}{T_2}$$

where T_2 is the time difference between CB operation and current reaching zero, v_C is the voltage across the filter capacitance, L is line inductance, and v_{CB} is the voltage across the circuit breaker. From this expression it can be seen that the peak voltage across the circuit breaker is dependent on several factors: the voltage across the capacitor, the energy required to be dissipated, and the time taken to dissipate this energy (T_2). The time will be dependent on the characteristics of the MOV, allowing for the possible use of the MOV as an overvoltage protection device.

The scalable IGBT and diode component models developed for the power converter are also used to form the scalable SSCB. The SSCB also includes a varistor whose mass is estimated proportionally to the IGBT mass.
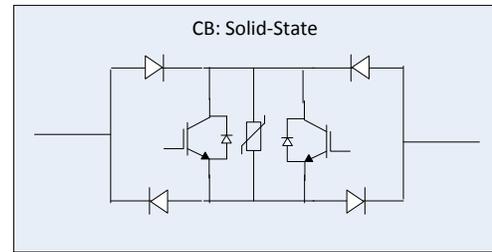

Figure 7. Solid-state circuit breaker topology

An example of a sensitivity trend derived from the SSCB model is shown in Figure 8, which indicates the SSCB specific power sensitivity to DC bus voltage. Unlike the power converter, the circuit breaker model does not use capacitive or inductive energy storage devices, so its nonlinearity is attributed to other reasons. Instead, the nonlinear specific power trend vs. bus voltage is primarily due to the IGBT device scaling as the IGBT mass decreases for lower conduction current requirements at slightly higher voltages. For voltages beyond the peak specific power, the higher blocking voltage rating dominates the IGBT mass scaling.
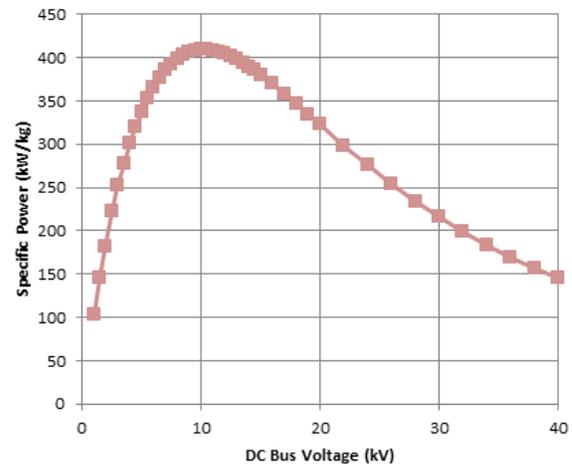

Figure 8. Specific power vs. DC voltage trend from 11.2 MW scalable SSCB model

Superconducting Fault Current Limiter (SFCL) Sensitivity Model

The primary role of the SFCL is to reduce the magnitude of the overcurrent requirements on all electrical system component requirements. This also allows for a reduction in the maximum interruption current required from isolation devices. Consequent to this overcurrent protection, the SFCL provides a quenching "pinch-point" in the system for managing quench events. When properly configured, a quench transition event is initiated and contained to the SFCL device. This quench protection affects thermal management requirements on electrical system components.

The protection system trade studies discussed in this paper are performed using a resistive-type SFCL. In contrast to other

methods of fault-current limiting, resistive-type devices rely on the inherent quench transition properties of a superconducting system. The quench transition is initiated when at least one of the superconductor's critical temperature, current density, or magnetic field properties is exceeded. This quench transition inserts resistance into the system to reduce the fault current. Resistive-type SFCLs are simple and lightweight compared to other devices and are widely used in terrestrial applications. However, it does suffer from an increase in recovery time after the quench event occurs [25].

During a quench event, the superconductor transitions through three regions of operation as the critical current density is exceeded in the resistive-type fault current limiter. These states are flux-creep, flux-flow, and resistive [26]. As the current increases above the critical current, conduction losses increase, which leads to elevated superconductor temperature over time. As discussed by Blair [27] and Nemdili [28], the duration of this process depends on magnitude of the fault current, heat transfer to the cryogenic fluid, and the physical properties of the superconducting material. Configuring quench management for the system is illustrated Figure 9. The solid black line represents the designed quench curve for the SFCL and the dashed blue line represents the quench curve for the adjacent components. The time to quench in both cases is a function of the fault current ratio ($\frac{i_{fault}}{i_{nominal}}$). The current at line A indicates the current at which quench can initiate on the SFCL and the current at line B indicates where quench can occur on the other systems.
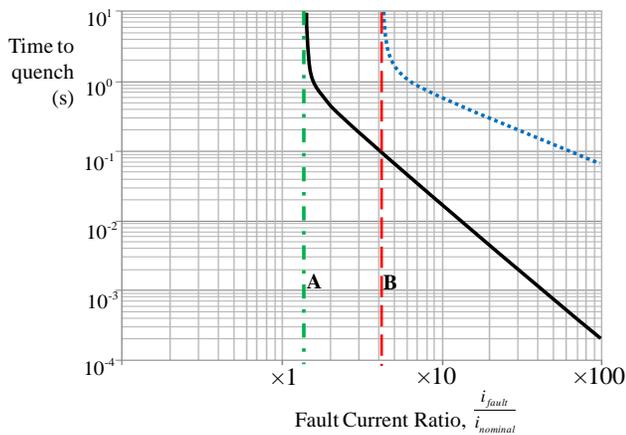

Figure 9 Coordinating quench protection with a fault current limiter.

Quench protection may be ensured in two ways. First, the SFCL is sized so that its quench initiation current is always less than that of the other components (A<B). Second, superconducting material selection for the SFCL can also assist in coordinating quench times. Each superconducting material undergoes quenching at a different rate. For example, BSCCO (Bi-2223) has a faster transition time that YBCO [28]. Therefore, if YBCO is selected for the primary distribution material, a BSCCO fault current limiter sized with similar quench current ratings will quench faster and localize the quench event within that device. However, the quench

transition times are also sensitive to the composition, layering, and coating structure used during superconducting tape/wire manufacturing. These layers are used for structural support and heat removal. Therefore, the selection of distribution and SFCL materials should account for the complete superconductor composition.

A resistive fault-current limiter device is essentially a closely thermally managed length of superconducting cable which is intended to undergo a quench transition during a fault scenario. The length of the superconducting wire used in this system determines the resistance introduced during the fault. Additionally, for a DC distribution system, it may be desirable that the SFCL superconductor be configured to add a desired amount of inductance into the system.

Figure 10 illustrates a generic layout for a SFCL arranged in a solenoidal configuration. The size and thickness of each layer in this configuration is expressed in terms of the minimum required quench resistance, the minimum desired inductance, the nominal and fault currents, the quench energy to be dissipated, and the stresses on the systems.
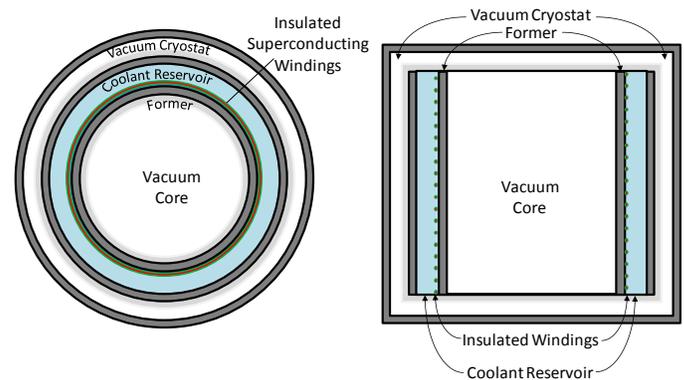

Figure 10 Generic solenoidal layout for a resistive type SFCL.

Several assumptions were made to estimate the overall system mass. The former and cryostat structural masses are estimated from the material performance properties of advanced low temperature zylon fiber/epoxy composite material [29]. A conservative estimate of the volume of the coolant reservoir assumes that all energy dissipated during the quench ($E = \int i^2 R(t)dt$) is absorbed by the coolant from the initiation of the quench until the current is interrupted by another device. While the quench event will result in local boiling of the cryogenic fluid, it is assumed that the bulk energy transfer to the coolant reservoir due to quench heating results in an average temperature rise under the gas transition temperature. This is enabled by providing coolant to the SFCL below this temperature. Venting and coolant recirculation are mechanisms employed to maintain coolant temperatures and pressures. However, the structure of the coolant reservoir is assumed to be sufficient to manage a coolant boil-off of limited duration. Subsequently, as illustrated in the next section, SFCL mass is highly sensitive to the response time of the interruption equipment. Cryocooling and coolant management systems will be affected by quench thermal management strategies.

The superconductor mass is a function of the current requirements as well as geometric and fault performance requirements. The minimum inductance requirements constrain the length and geometry of the superconducting coil. In addition, the minimum quench resistance requirement determines the minimum length of the superconductor. Additionally, the SFCL mass estimate assumes no leads to room temperature, thus negating all the thermal management equipment necessary to transition to conventionally conducting equipment.

Fault-Current Limiter and Circuit Breaker Trade Study

Within the protection system consisting of power converters, circuit breakers, and SFCLs, several trade studies can be conducted from which to determine how to minimize the protection system mass while providing TeDP system damage protection, quench protection, and the ability to reroute power. The first protection system trade discussed is the FCL and CB ratings and resulting fault response times and combined mass. The CB can be used with or without a SFCL. Since the CB mass is a function of the fault-current interruption, voltage blocking, and interruption time ratings, the use of the SFCL may reduce the CB mass by reducing the CB fault-current interruption rating. However, the CB mass savings may be offset by the addition of the SFCL depending on its mass. In addition to the CB fault-current rating, the current withstand ratings of downstream devices may also be reduced with the use of the SFCL.

The actual architecture transient fault response and thus CB fault-current rating depend on the fault impedance, component impedance including SFCL, and bus current control. The transient fault response can be modeled through detailed electrical and thermal transient models or by simplified lumped parameter models according to each protection zone and fault. An example of such a lumped network analysis for a VSC short-circuit underdamped fault response was conducted at the University of Strathclyde [24]. This methodology can be applied to determine the transient fault response of the system and the impact of the SFCL on CB ratings and mass.

The properly designed SFCL will limit the current so that the fault current level is high enough for protection systems to detect the fault but low enough so that protection devices do not have to be rated to withstand or interrupt large currents. As a result of the reduction in fault current, the rating of the circuit breaker will be reduced as well as the weight and physical size of the CB. Using SFCLs with CBs may also increase the reliability of successful fault interruption because the SFCL, when operating as designed, will limit the fault current seen by the CB to its rated value. Requiring the CB to interrupt a smaller amount of fault current may also decrease the fault current interruption time since the CB will be required to dissipate less energy. However, typically for protection device coordination, larger currents will cause protection devices to trip faster than smaller currents. Careful use of SFCLs and protection control schemes need to be implemented to use SFCLs to give the system the most benefit of reduced fault current levels while still having reliable

protection. When SFCLs are used throughout the system to reduce the overall system fault current level, magnetic and thermal stresses on distribution equipment, component cost, and voltage disturbances will be reduced [14,30].

The role and ratings of the SFCL and CB protection devices largely depend on the architecture and fault response. For this study, the protection system is designed to protect each zone from quenching and reroute available power to propulsor motors. From Figure 1, SFCLs are used on the AC cable section between the generators and rectifiers, and on the DC power transmission section from the rectifiers to the distribution buses. Considering the latter zone, the SSCB and SFCL masses and interruption time sensitivities to fault current rating and DC voltage are analyzed. For this zone, each transmission line and subsequent SFCL and CBs are nominally rated to 11.2 MW. The nominal current rating depends on the nominal DC bus voltage rating, which is not yet defined. As a result, these protection system trade studies are conducted within an architecture study to determine the component and system sensitivity to DC bus voltage.

The mass sensitivity of the SFCL device is illustrated in Figure 11-Figure 14. All sensitivities in these charts assume 11.2 MW nominal power capacity, a maximum allowable magnetic field of 0.5T from an inductive coil with a minimum allowable inductor coil diameter of 5cm. The superconducting material is assumed to be BSCCO operating in liquid nitrogen and the electric insulation is assumed to be laminated polypropylene paper with a dielectric strength of 50 kV/mm [31]. The number of windings and the diameter of the inductive coil are varied for each sample point to minimize the overall component mass.

Generally, increasing the voltage decreases the overall mass of the SFCL by decreasing superconductor mass and coil geometry (Figure 11). Conversely, increases to the time to interruption and fault current ratio increase SFCL mass by affecting the cooling requirements during the quench scenario (Figure 12 and Figure 13).
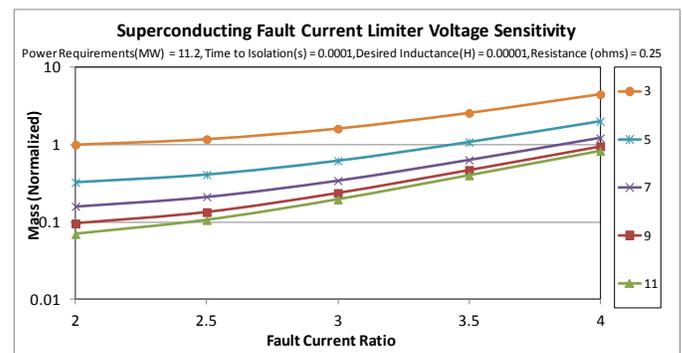

Superconducting Fault Current Limiter Voltage Sensitivity
Power Requirements(MW) = 11.2, Time to Isolation(s) = 0.0001,Desired Inductance(H) = 0.00001,Resistance (ohms) = 0.25

Figure 11 Sensitivity of a11.2MW nominally rated SFCL normalized mass to operating voltage and fault current ratio [Time to Isolation = 0.0001 s, Minimum Desired Inductance = 0.00001 H, Minimum Desired Resistance = 0.25 Ohms].
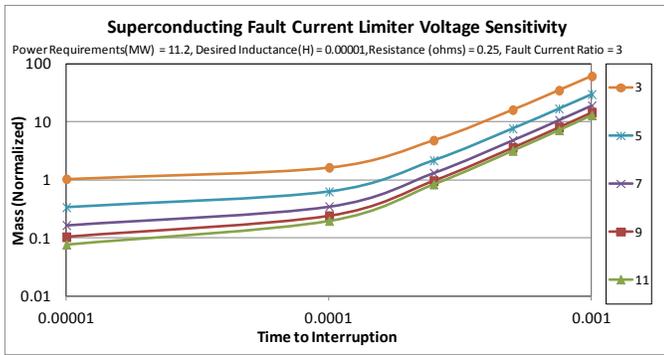
Figure 12 Sensitivity of a11.2MW nominally rated SFCL normalized mass to operating voltage and time to interruption [Minimum Desired Inductance = 0.00001 H, Minimum Desired Resistance = 0.25 Ohms, Fault Current Ratio = 3].
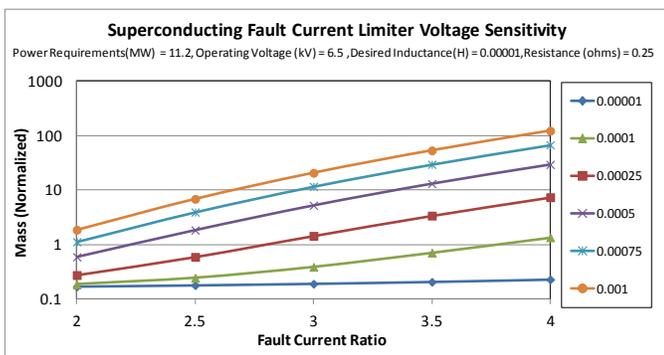

Figure 13 Sensitivity of a11.2MW nominally rated SFCL normalized mass to time to fault interruption and fault current ratio [Operating Voltage = 6.5 kV, Minimum Desired Inductance = 0.00001 H, Minimum Desired Resistance = 0.25 Ohms].

The geometry of the solenoidal SFCL is affected by the resistance and inductance constraints. This depends on which constraint is active for coil sizing. This is illustrated in Figure 14. For SFCL with high minimum inductance requirements, the mass is insensitive to minimum resistance. However, as the inductance requirement decreases, the minimum quench resistance constraint becomes active and the mass is driven by the required length of the superconductor.
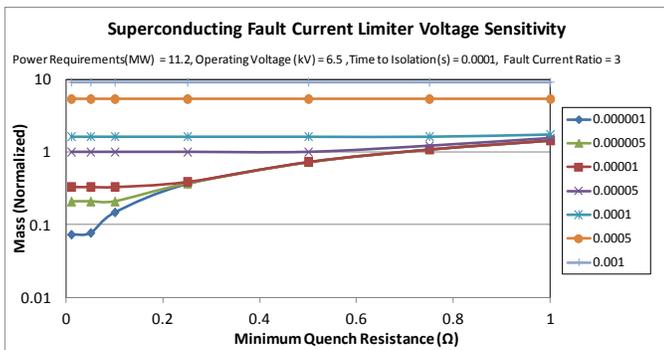

Figure 14 Sensitivity of a11.2MW nominally rated SFCL normalized mass to time to desired minimum inductance and desired minimum quench resistance [Operating Voltage = 6.5 kV, Time to Isolation = 0.0001 s, Fault Current Ratio = 3].

In conjunction with the SFCL mass sensitivities, the SSCB mass sensitivities should be analyzed and understood to determine the role and ratings of both the SFCL and SSCB. Figure 15 shows the rate of increase of the 11.2 MW SSCB mass as fault-to-nominal current ratio increases for several DC bus voltage ratings. The nominal current rating is calculated from the rated DC voltage and fixed 11.2 MW rating. The fault current rating is then calculated according to the specified fault-to-nominal current ratio. Using the SSCB sensitivity model as described previously, the SSCB mass is estimated from the fault current and voltage ratings. As the voltage rating increases, the nominal current rating decreases, which generally decreases the SSCB mass. The SSCB mass increase rate for higher fault current ratings is greater for lower voltage ratings. Considering SSCBs alone, the SSCB mass is minimized for lower fault current and higher voltage ratings. These trends need to be assessed in conjunction with the architecture component sensitivities to voltage to determine the operating voltage that minimizes architecture mass or maximizes architecture efficiency.

In addition to CB mass, it is also important to understand the CB current interruption time trends as the interruption time affects the protection system operation and design. Figure 16 shows current interruption time trends for the 11.2 MW SSCB scaled for several fault-to-nominal current ratios and DC bus voltage ratings. The current interruption times have been normalized and are on the order of 10s of microseconds. For lower voltage ratings, the interruption time trend slope is larger. This indicates that the current interruption time length is less sensitive to fault current rating for higher DC voltages. The current interruption time is fastest for lower fault current and higher voltage ratings.

A third major driver of CB ratings and impact on system performance is the SSCB conduction efficiency. Figure 17 illustrates an efficiency trend for the 11.2 MW SSCB for several DC voltages. The efficiency improves for higher voltage ratings due to the lower conduction losses at lower rated nominal currents.

To conduct a TeDP architecture trade study of the SFCL and SSCB ratings and roles with resulting mass sensitivities, a transient fault analysis of the specific architecture is necessary to determine the fault response with and without an SFCL. From this analysis, the necessary FCL ratings, such as superconducting and quench resistance, inductance, time to quench, and time to interruption, can be determined to achieve a specified fault-to-nominal current ratio. This transient modeling is beyond the scope of the sizing and sensitivity studies for which the scalable models were developed. This section summarizes the trends resulting from scalable SFCL and SSCB sizing models that can be used in conjunction with transient simulations to determine an optimum protection system design for the specified TeDP architecture. As part of a transient analysis, the time constants of the SFCL and SSCB responses must be considered when determining the role of the SFCL in response to a fault. With microsecond interruption

times, the SFCL does not have a large mass, mostly because the cryostat reservoir mass is small and the SFCL is not likely to completely quench. With SSCBs capable of interrupting faults in 10s of microseconds, the fault detection and diagnosis time becomes a significant factor in the time from the fault initiation to the fault interruption and isolation. This delay in fault detection and diagnosis time for the superconducting TeDP architecture is not known and may be significantly longer than the interruption time of an SSCB.
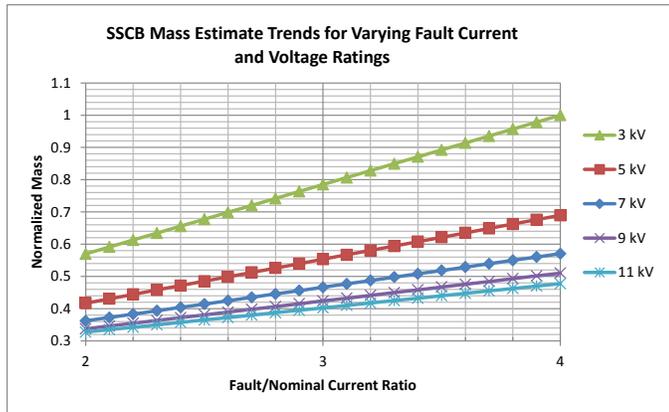
Figure 15. 11.2 MW SSCB mass estimate trends for varying fault current and voltage ratings.
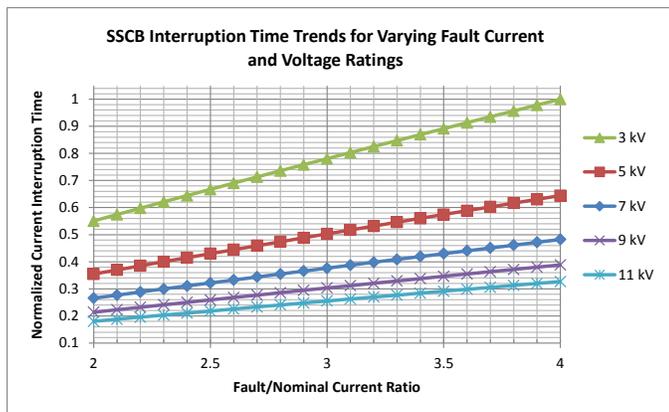

Figure 16. 11.2 MW SSCB interruption time trends for varying fault current and voltage ratings.
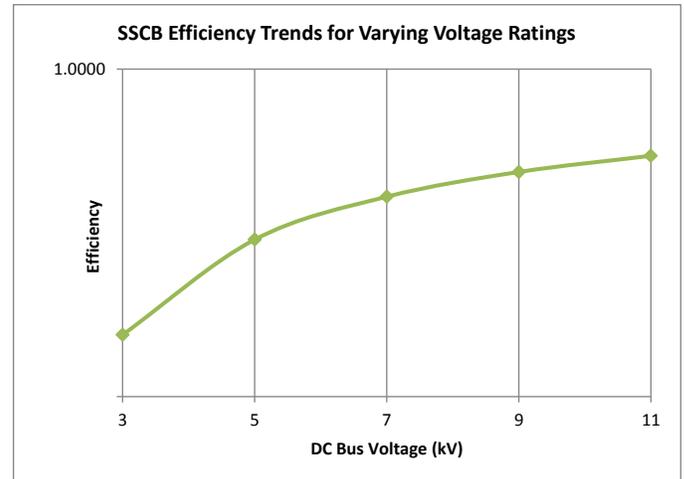

Figure 17. 11.2 MW SSCB efficiency trends for varying voltage ratings.

Power Converter and Circuit Breaker Trade Study

Another trade study of interest within the protection system is the role of power converters as protection devices. Depending on the converter topology, device ratings, and fault type, the power converter can be used to electrically interrupt a fault. Alternatively, a circuit breaker can be used as a protection device to dissipate fault energy and/or provide physical fault isolation. The trade study that follows describes one approach with an example of the mass, efficiency, and interruption time trade-offs when considering the use of power converters or circuit breakers for fault protection. The figures also show how these trades vary as the DC bus voltage varies and an approach for how these trades can be incorporated into a larger architecture voltage trade study.

The trends were derived from the scalable SSCB and unidirectional CSC models described previously. The SSCB and CSC are both rated to 11.2 MW. That is the maximum nominal power at which the components are rated which is required during a failed engine scenario through the cruise segment of the flight. Both the converter and SSCB are sized for operation at 100 K. Other parameters used to develop these trends for the CSC are: 400 Hz AC system, 5 kHz switching frequency, capacitance designed for 20% DC bus voltage magnitude ripple, and 10% DC bus current magnitude ripple. For the sake of illustration and comparison, a fault-to-nominal current ratio of 4:1 is assumed.

For the example described, Figure 18 shows the converter and CB normalized mass comparison and trends as a function of DC bus voltage. The mass calculations are normalized relative to the maximum calculated mass shown in the figure. The cases to compare are the CSC with SSCB for protection (purple with x markers) and CSC only rated for protection (red with square markers). The CSC and SSCB trend is the sum of the converter rated for twice nominal current (blue with diamond markers) and SSCB rated for four times nominal current trends (green with triangle markers). In the first case, the CSC is rated to carry the nominal current while the SSPC

is rated to carry four times the nominal current, which is the designated fault current rating for this example. In this way, the SSPC is sized as the sole protection device. The CSC IGBT ratings are such that the overcurrent ratings are twice the nominal current which is typical for IGBT ratings to allow for overcurrent withstand. In the second case, the CSC is rated to carry the four times nominal current, in which case it can be used as the protection device for DC load faults, and an SSCB is not required. For this trade, the figure indicates that the CSC with SSCB for protection is lighter than the CSC only used for protection for all DC bus voltages. Trends such as these can be developed for different fault-to-nominal current ratios or power ratings, such as for protection of the bidirectional inverter/rectifier used to drive a propulsor motor, to assess the system sensitivity of the use of power converters as protection devices.
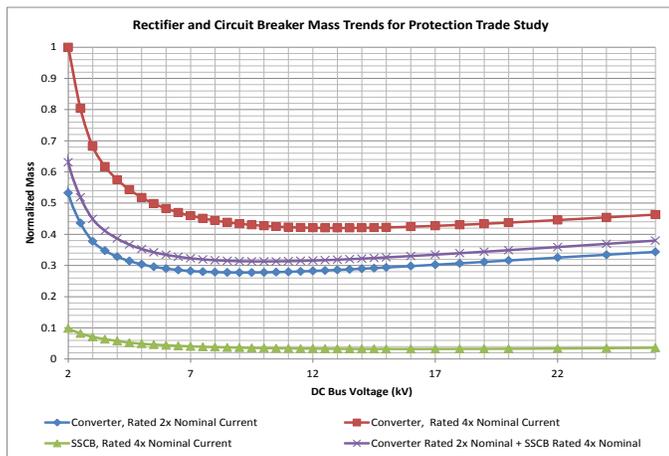

Figure 18. 11.2 MW CSC and SSCB mass comparison trends for protection trade study

Figure 19 shows the efficiency trends for the converter and CB protection trade. This trade indicates that the CSC with SSCB for protection operates more efficiently at the 11.2 MW operating point than the CSC rated for protection for all DC bus voltages. This is due to the voltage and current scaling of the IGBTs and estimated losses. Note that the DC bus voltage that achieves the maximum efficiency is lower than the DC bus voltage that achieves the minimum mass.

In addition to mass and efficiency, the fault interruption time capability of the protection device also plays a role in the design of the protection system. Figure 20 shows a comparison of the CSC with SSCB and CSC only estimated fault interruption times. Note that these estimates do not include time to detect and diagnose the fault. These trends indicate a slightly faster interruption time with the use of the CSC as a protection device over the SSCB. However, the control of the CSC may be more complicated than for an SSCB.
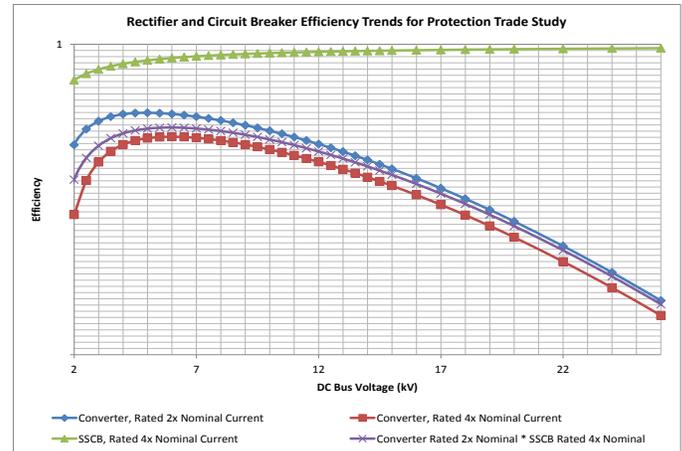

Figure 19. 11.2 MW CSC and SSCB efficiency comparison trends for protection trade study
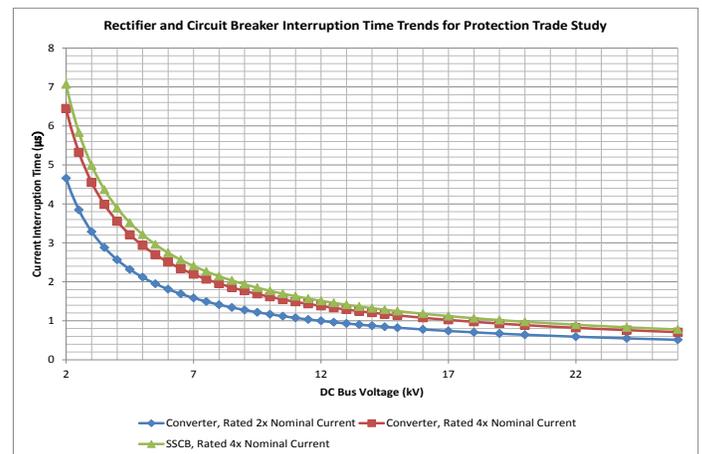

Figure 20. 11.2 MW CSC and SSCB current interruption time comparison trends for protection trade study

Summary/Conclusions

Several TeDP protection system design and operation considerations as well as approaches to conduct protection system trade studies were discussed. The protection system configuration and response is specific to the TeDP architecture, but these considerations are applicable to any partially or fully-superconducting electrical system. The unique quenching behavior of a superconducting network provides additional transient electrical and thermal protection challenges. Scalable architecture and protection component sensitivity models are useful for conducting architecture and protection system sensitivity studies, such as mass and efficiency sensitivities to voltage and temperature. These sensitivity studies enable a systematic approach to optimize the architecture and its protection system design to achieve an objective such as minimizing mass or maximizing efficiency for an aerospace TeDP system.

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Contact Information

Michael Armstrong, PhD
Rolls-Royce North American Technologies, Inc.
Michael.armstrong@liberty.rolls-royce.com
317-230-2257

Acknowledgments

Definitions/Abbreviations

AC	Alternating Current
CB	Circuit Breaker
CSC	Current-Source Converter
DC	Direct Current
IGBT	Insulated Gate Bipolar Transistor
NOx	Mono-nitrogen oxides
SFCL	Superconducting Fault-Current Limiter
SSCB	Solid-State Circuit Breaker
TeDP	Turboelectric Distributed Propulsion
VSC	Voltage-Source Converter