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Comparing SiC MOSFET, IGBT and Si MOSFET in LV distribution inverters

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Abstract—Efficiency, power quality and EMI are three crucial performance drivers in LVDC applications such as electrical supply, EV charging or DC aerospace. Recent developments in SiC MOSFETs and MMC for LVDC promise two significant improvements in LVDC inverter performance. However, the designer is left with many combinations of technology and inverter level to choose from. This paper aims to clarify this choice by identifying one optimum Si design and one optimum SiC design, using detailed loss calculations. An IGBT inverter is included as a baseline. Loss calculations estimate the effects of Si MOSFET switching loss and all parasitic interconnection loss. The validity of the loss estimations are verified using careful experiments on a Si MOSFET cell. Close agreement indicates that the modelling approach is valid for extension to many cells in series, and to the parallel connection of many devices. Despite the lower EMI inherent in MMC inverters, Si MOSFETs risk worse EMI, due to poor reverse recovery characteristic. Slowed device gate switching experimentally demonstrates the reduction in switching noise, promising very low EMI. This initial study has therefore identified two promising candidate SiC and Si MOSFET inverters which will be fully constructed in future work, in order to aid designers in choosing the optimum semiconductor technology and topology for LVDC inverters.

Keywords—Si MOSFET; MMC; SiC MOSFET; loss calculation; efficiency; EMI; EMC; ringing; voltage overshoot; diode reverse recovery; power quality

I. INTRODUCTION

DC-AC converters with high efficiency and high power quality are in increasing demand. Switching to a low voltage dc (LVDC) distribution system simplifies a utility network, leading to improved reliability, elimination of frequency stability and skin effect issues, and improved control over power factor at the point of use [1,2]. Drivers for utility networks include low volume, high power quality, very high efficiency and longevity, and demanding targets for distribution system losses must be met. DC aerospace systems constitute a further LVDC application, where volume and weight are critical (making thermal management highly challenging) and strict EMI requirements must be met, while constantly improving performance and reducing fuel consumption.

To summarize, realizing the advantages of LVDC therefore requires development of highly efficient, high power quality, low EMI inverters. Modular multilevel converters (MMC) have traditionally only been used at HV and MV, however recent work has suggested that when Si MOSFET MMC are applied to LV inverters [2,3], efficiency is improved compared with 2-level inverters. However, the increasing availability of SiC complicates the choice of circuit topology for an LV inverter. It is not currently clear whether SiC or Si MOSFETs will offer superior performance in LVDC applications. This work uses highly detailed theoretical analysis to present an initial comparison of semiconductor technologies for LVDC. Using these results, the myriad possible combinations of semiconductor technology and inverter topology can be reduced to just two circuits which can be compared in full scale experiments to compare SiC and Si MOSFETs for LVDC. Analysis includes all parasitic interconnection losses incurred in the parallel combination of devices, and in the series connection of cells to create MMC. These losses are added in the form of series resistance to the on-state resistance exhibited by the devices. The accuracy of predictions for interconnection loss is experimentally verified using a single MMC cell. This loss, which accumulates with increasing MMC level and increasing parallel connection, is accounted for by the model.

It is helpful to first examine the general trends in efficiency, power quality and EMI of 2-level and MMC inverters.

2-level converters

Power quality can only be improved by increasing the switching frequency, which degrades efficiency and EMI. High switching frequency increases switching loss and requires fast devices, leading to high EMI [4]. Improvements in efficiency by connecting devices in parallel cannot be realised when switching frequency increases (due to parasitic reactances and skin effect), whilst switch timing errors increase when many devices are connected in parallel at high switching frequency. High switching loss in IGBTs forces the use of switching frequencies below 20kHz [5], leading to poor output waveform quality. SiC MOSFETs support 2-level converters at 1kV, but with reduced switching loss than IGBTs due to near elimination of tail current [6] and comparable on-state conduction loss [7], permitting higher switching frequency and lower EMI.

Modular multilevel converters (MMC)

MMC [8] have already been successfully employed in HVDC scale IGBT inverters resulting in significant reduction in conversion losses over comparable 2 level inverters [9]. A similar approach may be applied to LV (1kVdc) where the low cell voltage facilitates the use of low-voltage Si MOSFETs.
With low cell voltage, low $R_{\text{dc, on}}$ MOSFETs may be selected such that the conduction losses do not exceed that of a two level IGBT converter [3].

MMC achieve excellent power quality with low device switching frequency [2,3]. With MMC of around 11-levels or more, switching loss becomes totally insignificant [3]. Low device switching frequency maximizes the efficacy of connecting many devices in parallel to reduce conduction loss, whilst realizing accurate switch timings. With low device switching frequency, and negligible switching losses, device voltage and current transients can afford to slow considerably without degrading converter efficiency. Slow transients should significantly improve EMI [10]. Low MMC cell voltage also reduces EMI, due to reduced ringing amplitude. The MMC further eliminates the need for a bulky, lossy output filter as a result of better waveform quality [11].

Choosing the three highest efficiency devices to represent SiC MOSFET, Si MOSFET and IGBT for comparison with one another was a partly iterative process. The inverter level in which the device is used dictates which device achieves maximum efficiency. For example: in an 11-level MMC, an IGBT with high switching loss, and low conduction loss is more efficient than an IGBT with low switching loss and high conduction loss, however if the same two IGBTs are compared in a 2-level converter then the IGBT with lower switching loss will prove optimal. Therefore, in this paper, the combination of IGBT choice and inverter level which achieves the highest efficiency is used to represent IGBT’s in the comparison. A similar iterative process was carried out to choose the inverter level and commercial device for SiC and Si MOSFETs.

EMI can also be improved through careful control of circuit parasitics or choosing diodes with good reverse recovery characteristic. SiC diodes offer improved diode reverse recovery characteristic compared with either IGBT or Si MOSFET technology, while the introduction of Si MOSFETs to converters risks higher EMI due to their faster switching transients and poorer reverse recovery [12]. The detrimental effects of Si MOSFETs on EMI can perhaps be mitigated by slowing switching transitions. Experiments reported below suggest that dramatic EMI reductions can be realized by slowing gate rise- and fall-time.

II. MODELLING LVDC INVERTER CONFIGURATIONS

LVDC inverters operating from 1kVdc link voltage, and delivering 10kW, at 415Vdc 3-phase will be considered in this analysis. Switching frequency for the 2-level converter is set to 10kHz, with device switching frequency of 10/2kHz in the MMC, where $n$ is the number of levels in the MMC.

The output voltage and load current on phase $a$ is given, as a function of time, $t$, and mains frequency $\omega=2\pi f$:

$$v_a(\alpha) = V_a \sin(\alpha)$$  \hspace{1cm} (1)

$$i_a(\alpha) = I_a \sin(\omega t - \phi)$$  \hspace{1cm} (2)

in which $\cos \phi$ is the power factor. Junction temperature is set to 125°C for all calculations, and it is assumed that heatsinking is sized accordingly. Calculations for all circuit configurations assume that gate voltage conditions are set for minimum on-state losses.

A. IGBT 3-level Converter

With 1kVdc input voltage, a 3-level IGBT converter with a 1.2kV IGBT (Infineon IKW40N120H3 [13]) offers lower loss than a 2-level converter with a 1.7kV rated IGBT. The circuit is shown in Fig. 1.

Conduction losses in the devices are found from [14]:

$$P_{\text{cond, IGBT}} = \frac{1}{2} \frac{d}{d\alpha} \int [d]_a(\alpha) \int [f]_a(\alpha)$$  \hspace{1cm} (3)

$$P_{\text{cond, SiC MOSFET}} = \frac{1}{2} \frac{d}{d\alpha} \int [d]_a(\alpha) \int [f]_a(\alpha)$$  \hspace{1cm} (4)

$$P_{\text{cond, Si MOSFET}} = \frac{1}{2} \frac{d}{d\alpha} \int [d]_a(\alpha) \int [f]_a(\alpha)$$  \hspace{1cm} (5)

$$P_{\text{cond, Si MOSFET}} = \frac{1}{2} \frac{d}{d\alpha} \int [d]_a(\alpha) \int [f]_a(\alpha)$$  \hspace{1cm} (6)

in which $V_{ce0}$ is the IGBT collector-emitter voltage under zero current conditions, $R_{on(T)}$ is the incremental on-state resistance of the IGBT, $V_{d(T)}$ is the diode collector-emitter voltage under zero current conditions, $R_{on(T)}$ is the incremental on-state resistance of the diode. All parameters are linearly interpolated as a function of junction temperature using figures provided by the manufacturer at 25°C and 175°C, for currents in the range 15-50A.

Switching losses are found using a curve fit for turn-on and turn-off losses ($E_{\text{on}}$ and $E_{\text{off}}$ respectively) given in the data sheet, as a function of collector-emitter current, at 175°C, given by (7) and (8). Variation with junction temperature is linearly interpolated between values given for 25°C and 175°C, which is seen to be a reasonable approximation from Fig. 15 of [13].

$$E_{\text{on}} = E_{\text{on, offset}} + \left| i_a(\alpha) \right|^2 E_{\text{on, slope}}$$  \hspace{1cm} (7)
\[ E_{\text{sw}} = i_r(\alpha) E_{\text{off, slope}} \]  
\[ P_{\text{sw, IGBT, 175\degree}} = \frac{\int V_{\text{ref}}}{V_{\text{ref}}} \left[ E_{\text{on, offset}} + \left[ \int_i \sin(\alpha - \phi) \right] E_{\text{on, slope}} \right] \cdot I_{\text{ref}} \]  

where \( E_{\text{on, offset}} \), \( E_{\text{on, slope}} \), and \( E_{\text{off, slope}} \) are constants used in curve-fitting of switching energy as a function of drain current, \( V_{\text{ref}} \) is the dc link voltage, \( V_{\text{ref}} \) is the supply voltage at which datasheet switching loss was measured, and \( f \) is switching frequency. Switching loss at junction temperature \( T_J \) is then found from 
\[ P_{\text{sw, IGBT}} = P_{\text{sw, IGBT, 175\degree}} \left[ 1 - \text{slope}(175 - T_J) \right] \]  

in which \( \text{slope} \) is the slope of total switching loss as a function of junction temperature \( T_J \).

### B. SiC 2-level Converter

The device used for this loss calculation is the 1.7kV Cree CAS300M17BM2 [15], with 16m\( \Omega \) on-state resistance. The SiC MOSFET 2-level converter, shown in Fig. 2, can also benefit from synchronous rectification, hence loss calculations assume that the diodes do not contribute to the conduction loss, and that the MOSFETs are conducting over the complete cycle. This assumption has been shown to be valid previously by the authors [3]. Conduction loss for one MOSFET is found from:
\[ P_{\text{cond, SiC, MOSF}} = \frac{1}{2} \left[ \int_{\text{on}} \left( i_r(\alpha) \right) R_{\text{dc, on}} [T_J] i_r(\alpha) \right] \]  

Switching energy is approximately linearly related, through constants \( K_1 \) and \( K_2 \) to MOSFET drain current as
\[ E_{\text{sw}} = K_1 + K_2 i_r(\alpha) \]  

![Fig. 2 2-level converter using SiC MOSFETs](image)

However, in synchronous rectification mode, a single switching cycle involves two turn-on and turn-off cycles, due to the fact that the diode conducts briefly during the dead time. The switching steps are listed for commutation between the lower and the upper devices, for the case where the load current is negative: 
- At the start \( T_{a2} \) is conducting 
- \( T_{a2} \) turns off and \( D_{a1} \) turns on briefly during the dead time 
- \( T_{a1} \) turns on and \( D_{a1} \) turns off 
- \( T_{a1} \) turns off and \( D_{a1} \) turns on briefly during the dead time 
- \( T_{a2} \) turns back on again and \( D_{a1} \) turns off, and one switching cycle is complete.

Switching energy is then adjusted to allow for a lower gate resistance at a drain current of 300A. Temperature effects on switching loss are seen to be sufficiently small to reasonably be neglected [15],
\[ E_{\text{sw}} = \frac{V_{\text{d}} K_{\text{IGBT}}}{V_{\text{ref}}} \left[ K_1 + K_2 \left( \int_{\text{on}} \sin(\alpha - \phi) \right) i_r(\alpha) \right] \]  

Losses in the SiC 2-level converter at a switching frequency of 10kHz are dominated by switching loss, and so losses for 3-level SiC MMC were calculated, using a lower voltage rated device. However, switching loss in SiC devices does not reduce sufficiently with smaller voltage rating [15], so loss is greater for the 3-level MMC compared with the 2-level.

### C. Si MOSFET Modular Multilevel Converter (MMC)

MOSFET voltage rating is chosen to allow for overshoot voltage up to around 170\%, using overshoot measurements observed by the authors [3]. The topology of a 3-level MMC converter is shown in Fig. 3. The number of cells in each arm is given by \( n \) for a converter with \( n + 1 \) levels. The Si MOSFET MMC calculations have been performed assuming that all operation is in synchronous rectification mode. Hence conduction loss for one cell, \( P_{\text{cond, cells}} \) is given by (11). Switching loss must be doubled for synchronous rectification, as discussed for the SiC converter. Switching loss must be estimated separately for the MOSFET and diode as switching energy is not generally given in Si MOSFET datasheets.

![Fig. 3 3-level converter using Si MOSFETs](image)

Referring to Fig. 3, the current in one arm of phase \( \alpha \) of an MMC converter is given by
\[ i_r(\alpha) = I_{\text{dc}} + \frac{1}{2} i_r(\alpha) \]  

in which \( I_{\text{dc}} \) is the proportion of dc input current corresponding to phase \( \alpha \).

MMC MOSFET switching loss is approximated by
in which \(V_{\text{oss}}\) is the gate-source voltage and \(Q_{\text{gs}}\) is the gate-source charge.

\[ P_{\text{oss, MOSFET cell}} = \frac{f_{\text{SW}} V_{\text{dc}}^2 Q_{\text{oss}}}{2 L_{\text{f}}} \left[ I_{\text{dc}} + \frac{1}{2} I_s \sin(\alpha - \varphi) \right] d(\alpha) \]  

(16)

\[ \text{in which } V_{\text{dc}} \text{ and } I_{\text{dc}} \text{ are the supplied voltage and current at which the gate charges are specified in the datasheet, } Q_{\text{oss}} \text{ is the total gate switching charge[16] given by} \]

\[ Q_{\text{oss}} = \frac{Q_{\text{gs}}(V_{\text{gs}} - V_{\text{th}})}{V_{\text{gs}}} + Q_{\text{gd}} \]  

(17)

\[ \text{in which } Q_{\text{gs}} \text{ and } Q_{\text{gd}} \text{ are gate-source and gate-drain charge respectively, } V_{\text{gs}} \text{ is gate-source plate voltage and } V_{\text{th}} \text{ is threshold voltage. } I_c \text{ is the average gate voltage during the period from threshold to the end of the Miller plateau (18)} \]

\[ I_c = \frac{V_{\text{gs}} - V_{\text{th}}}{R_c + R_g} \]  

(18)

\[ \text{in which } R_c \text{ is external gate resistance, } R_g \text{ is internal gate resistance, } V_{\text{gs}} \text{ is the gate drive voltage and } V_{\text{th}} \text{ is the gate-source voltage during the Miller plateau. The diode switching loss is approximated from reverse recovery charge} \]

\[ P_{\text{oss, diode cell}} = \frac{2 f_{\text{SW}} Q_{\text{rr}}(\pi/\omega)_{\text{dc}}^2}{I_{\text{dc}} / V_{\text{dc}}} \left[ I_{\text{dc}} + \frac{1}{2} I_s \sin(\alpha - \varphi) \right] d(\alpha) \]  

(19)

\[ \text{in which } Q_{\text{rr}(T)} \text{ is the reverse recovery charge, and } V_s \text{ and } I_s \text{ are the reverse voltage and forward current at which } Q_{\text{rr}(T)} \text{ was measured.} \]

**D. Si MOSFET MMC and SiC 2-level with Parallel-connected Devices**

Loss calculations are then performed for Si and SiC MOSFETs operating in synchronous rectification mode, with multiple devices connected in parallel. Formulae used in Section C can be modified for connecting \(k\) devices in parallel by dividing \(R_{\text{ds,on}}\) by \(k\) in (11). However, when attempting to use multiple MOSFETs connected in parallel, particularly for the very low voltage rating devices, parasitic track resistance and solder joints will start to become more significant than the \(R_{\text{ds,on}}\) of the MOSFETs. Measures can be taken to minimize track resistance, but realistic parasitic resistance is likely to reach an order of at least 0.2m\(\Omega\) at each end to connect to the bus connections joining the cells, and perhaps 0.1m\(\Omega\) to connect from the bus to each source and drain. Total on-state resistance for the combined devices can therefore be estimated from

\[ R_{\text{ds, comb}} = 0.4 + \frac{1}{k} (R_{\text{ds,on}} + 0.2) \text{m}\Omega \]  

(20)

Current in each device is now given by

\[ i_{\text{device}}(\alpha) = \frac{1}{k} \left[ I_s + \frac{1}{2} I_s \sin(\alpha - \varphi) \right] \]  

(21)

SiC MOSFETs switching loss is not expected to change with parallel-connected SiC devices.

**III. Modeled Loss Comparisons**

**A. Comparing all Technologies with no Parallel Connection**

Loss is presented for a range of different levels of MMC, 3-level IGBT, and for 2-level SiC MOSFET. Fig. 4 shows results obtained without using any parallel connection. Table 1 lists the devices used for each configuration.

<table>
<thead>
<tr>
<th>Topology</th>
<th>Manufacturer/model</th>
<th>(V_{\text{max}}) (V)</th>
<th>(R_{\text{ds(on)}}) (m(\Omega))</th>
</tr>
</thead>
<tbody>
<tr>
<td>IGBT 3 level</td>
<td>Infineon IKW40N120H3</td>
<td>1200</td>
<td>18.8</td>
</tr>
<tr>
<td>SiC 2 level</td>
<td>Cree CAS300M17BM2</td>
<td>1700</td>
<td>8</td>
</tr>
<tr>
<td>Si MMC 7 level</td>
<td>IR FP4868</td>
<td>300</td>
<td>25.5</td>
</tr>
<tr>
<td>Si MMC 11 level</td>
<td>IR FP4668</td>
<td>200</td>
<td>8</td>
</tr>
<tr>
<td>SiC 17 level</td>
<td>IR FP4468</td>
<td>100</td>
<td>2</td>
</tr>
<tr>
<td>Si MMC 29 level</td>
<td>Infineon IPT007N06N</td>
<td>60</td>
<td>0.75</td>
</tr>
<tr>
<td>SiC 43 level</td>
<td>IR IL47211</td>
<td>40</td>
<td>0.34</td>
</tr>
</tbody>
</table>

DC link voltage, \(V_{\text{dc}}\), is 1kV throughout, and load current is varied to sweep output power (1 phase) from 0.85 to 10kW. Power factor and modulation index are set to 1, \(R_c = 1\). All devices are chosen to ensure overvoltage does not take place during switching overshoot. At MMC levels lower than 7 switching loss is a fairly significant portion of loss [3]. As MMC level is raised above 17 the reduction in cell voltage is no longer significant to drop to the next MOSFET voltage rating until a level of around 29.

**Fig. 4 Losses per phase as a function of output power per phase, with no parallel connection.**

Examining Fig. 4 it can be seen that IGBT losses rise more gradually with rising load current than MMC topologies. This is because the IGBT losses are dominated by on losses caused by \(V_{\text{oss}}\), which rise as a function of \(i_{\text{ds}}(\varphi)\), where MMC losses, determined mainly by on-state resistance loss, are proportional to \((I_s(\varphi))^2\). SiC losses rise very slowly with power because SiC loss comes mostly from switching which rises relatively slowly with increasing current [15]. Consequently, for the Si MMC configurations, above 4kW/phase output power there must be at least 11 levels to exceed IGBT 3-level performance. At least 17 levels are required for Si MMC loss to be lower than SiC, but by 10kW/phase the advantage is turning back to...
SiC. Further increases in MMC level achieves the lowest loss, but at very high cost in complexity.

B. Comparing all technologies with parallel connection

The number of devices connected in parallel is varied from 1 to 12, and total losses per phase are calculated, with $V_{dc}=1kV$ and $P_{out/phase}=3kW$, shown in Fig. 5. Parallel-connected device loss is calculated for all the MMC levels, and for the SiC 2-level. Loss is quite dramatically lowered with just 2 parallel-connected devices at the lower levels of Si MMC. This offers a reduction in circuit complexity, volume and weight as 2 parallel-connected devices require simpler control than higher levels of MMC. Improvements obtained by more than 2 devices connected in parallel become less significant as level number increases. For 29- and 43-level MMC, parallel connection actually worsens loss compared to a lower level MMC using the same number of devices connected in parallel (due to the increasing parasitic losses). For SiC, parallel connection has little impact on loss.

For both (a) and (b), total track resistance was calculated for the PCB, which was not insignificant. Since not all of the heat dissipated in the tracks would act to raise heatsink temperature (some would be radiated), only half of the calculated parasitic resistance was included in the calculation.

V. IMPLICATIONS OF MOSFET MMC FOR EMC

With MMC at higher levels switching loss has been shown to be negligible [3], meaning that an increase in switching loss would not degrade efficiency, allowing slowed switching. In this experiment gate resistance was varied to investigate the relationship between gate-source turn on and diode recovery profile, using the chopper circuit from Section IV. Results are presented for MOSFET drain current in Fig. 7 during MOSFET turn on, and MOSFET drain-source voltage in Fig. 8 during turn off, for external gate resistances, $R_G$, of 5.5–220 Ω.

![Fig. 5 Losses per phase as a function of the number of MOSFETs connected in parallel. $P_{out}$ per phase = 3kW.](image)

IV. EXPERIMENTAL VALIDATION OF Si MMC LOSS

Two sets of loss measurements were taken using a 2-level converter with the IR IRFB4127 [17] driven as a ‘chopper’ at a duty cycle of 50% (a) not in synchronous rectification mode, and (b) in synchronous rectification mode. Measured and calculated results are shown to agree very closely in Fig. 6.

![Fig. 6 Loss dissipated in heatsink for chopper operating with and without synchronous rectification.](image)

As $R_G$ is increased, both peak reverse recovery current, $I_{RRM}$, and ringing gradually reduce during MOSFET turn on. It is noticeable that this effect is smaller than the reduction in over-voltage at turn off. Current ringing amplitude has reduced by a factor of approximately 0.85 due to lower rate of change of forward diode current, $dI/dt$, and maximum $dI/dt$ is lower by a factor of approximately 0.158, which is empirically found to be approximately equal to $\sqrt{(R_G_{old}/R_G_{new})}$.

Electric fields ($E$-fields) are generated through both differential and common-mode currents, with common-mode
currents tending to dominate EMI radiation [18]. E-fields from common mode currents are proportional to both frequency and current magnitude, while E-fields from differential mode currents are proportional to the square of frequency [19]. The frequency of interest here is not the switching frequency, but the RF frequencies contained within the spectrum of the fast switching transients, therefore, slowing the switching transient, thus reducing the peak current and the ringing frequency all act to reduce radiated emissions [19]. The relationship between radiated E-fields caused by current, frequency content (f) and current amplitude (Ipk) are summarized by (24-27).

\[ f \propto \frac{\Delta i}{\Delta t} \propto \sqrt{R_{G_{\text{gs}}}} \frac{\Delta R_{G_{\text{min}}}}{R_{G_{\text{min}}}} \]  
\[ I_{\text{RRM}} = I_{\text{pk}} \]  
\[ E_{\text{common mode}} = 20 \log \left( f_{I_{\text{pk}}} \right) \]  
\[ E_{\text{differential mode}} = 20 \log \left( f_{I_{\text{pk}}} \right) \]  

The effect on \( \frac{\Delta i}{\Delta t} \) and \( I_{\text{RRM}} \) at higher current levels is estimated using (24-27), when \( R_C \) is increased from \( \Omega \) to 220Ω in the model used in Section III C. This change in \( R_C \) is calculated to reduce \( \frac{\Delta i}{\Delta t} \) (and therefore frequency) by \( \sqrt{1/(1/220)} \). This reduced \( \frac{\Delta i}{\Delta t} \) can then be used in the datasheet plot of \( \frac{\Delta i}{\Delta t} \) versus \( I_{\text{RRM}} \) to find that the corresponding reduction in \( I_{\text{RRM}} \) (and therefore ringing amplitude) is a factor of at least 4. Radiation is therefore estimated to drop by approximately 0.25\( \sqrt{1/(220)} \)=35dB in common mode and by 0.25\( \sqrt{1/(220)} \)=59dB for differential mode. Despite this much slower switching speed, total calculated loss does not increase for 11-levels and above.

VI. CONCLUSION

The MOSFET based MMC approach has been shown to produce significantly reduced loss compared with IGBT solutions. The advantage is not so clear between SiC and Si MOSFET MMC. SiC appears to achieve high efficiency with the simplicity of a 2-level converter and promises to achieve low levels of EMI due to good diode reverse recovery profile. Si MOSFET MMC with at least 2 devices connected in parallel and \( \geq 11 \) or more levels promises lower loss than IGBT or SiC in a 10kW 3-phase DC-AC converter. The accuracy of Si MOSFET loss calculations is demonstrated through comparisons of calculated and experimental loss for a single MMC cell, operated as a chopper circuit. This also serves to demonstrate the accuracy of comprehensive estimated parasitic interconnection losses in all the models used in this study. EMI could prove problematic for Si MOSFET MMC compared with SiC. However, experimental results have been presented here showing that slowing of the switching transition using the gate drive can reduce ringing and voltage overshoot, leading to anticipated reduction in radiated electric field of as much as 35-59dB, with no impact on loss.

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