Wideband TV White Space Transceiver Design and Implementation

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***Abstract*—For transceivers operating in television white space (TVWS), frequency agility and strict spectral mask fulfillments are vital. In the U.K., TVWS covers a 320-MHz-wide frequency band in the UHF range, and the aim of this brief is to present a wideband digital up- and downconverter for this scenario. Sampling at radio frequency (RF), a two-stage digital conversion is presented, which consists of a polyphase filter (PPF) for implicit upsampling and decimation, and a filter-bank-based multicarrier approach to resolve the 8-MHz channels within the TVWS band. We demonstrate that the up- and downconversion of 40 such channels is hardly more costly than that of a single channel. Appropriate filter design can satisfy the mandated spectral mask and control the reconstruction error. A field-programmable gate array implementation is discussed, capable of running the wideband transceiver on a single Virtex-7 device with sufficient word length to preserve the spectral mask requirements of the system.**

***Index Terms*—Filter banks, software radio, white space, wideband transceiver.**

I. Introduction

THE switch from analog to digital television (TV) has resulted in the local availability of benign wireless communication channels in the so-called TV white space (TVWS) spectrum, which has triggered a number of important applications including rural broadband access [1], [2]. The latter also offers infrastructure for smart grid [3] and potentially 5G services. In the U.K., the TVWS spectrum ranges from 470 to 790 MHz and is divided into 40 channels of 8-MHz bandwidth each. Wireless transmission over TVWS sets a number of requirements to potential devices, including frequency agility in order to select and change channels depending on geolocation, and the strict adherence to spectral masks which are likely to be imposed by regulators to protect incumbent users [4].

With substantial progress in the area of analog-to-digital (ADC) and digital-to-analog conversion (DAC) (see, e.g., [5]–[7] where devices can operate close to 3 GHz), software-defined radio transceivers that exhibit the frequency agility and flexibility required of future TVWS devices appear viable. Therefore, the aim of this brief is to explore a transceiver design and implementation that is capable of converting the entire 320-MHz TVWS range from and to RF and to discuss some of its characteristics in terms of cost, latency, and selectivity.

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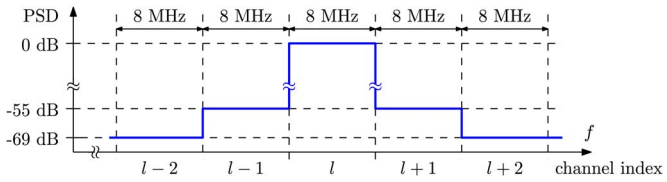

Fig. 1. Spectral mask defining permitted PSD levels in adjacent $(l \pm 1)$ and next-adjacent $(l \pm 2)$ TVWS channels [4].

The permitted interference levels outlined in Fig. 1 cannot be met by standard orthogonal frequency division multiplexing (OFDM). Therefore, filter bank techniques that predate OFDM [8]–[11] have recently seen a revival in the form of filter-bank-based multicarrier (FBMC) modulation [12]–[14] due to their superior spectral confinement and resulting advantages in terms of synchronization over OFDM [15]–[17].

Most FBMC transceivers operate in the baseband, where a number of subchannels or multiple users are allocated to well-defined frequency bands. Popular structures include discrete Fourier transform (DFT) modulated filter banks [8], [15] and derivatives [18] but also iterated halfband schemes such as [11]. Many filter bank schemes currently evolving in the context of frequency agility and cognitive radio [19], [20] are also located in the baseband. In the context of software radio, recently, a number of implementations of wideband receivers based on filter banks have been discussed [21]–[24], whereby very high speed implementations such as [23] are restricted to essentially a DFT, while more flexible filter bank designs such as [21] and [22] do not comment on complexity or attempt a real-time implementation.

Based on initial design work in [25] and [26] for a two-stage architecture and a low-rate implementation in [27], this brief explores the design and real-time field-programmable gate array (FPGA) implementation of a wideband TVWS frequency agile transceiver. In order to accomplish an implementation, different from [25], the number of subbands is restricted to a power of 2. In the following discussion, Section II outlines the overall system, while Section III provides some design details. The multirate implementation and its impact on complexity and latency are explored in Section IV and demonstrated in Section V. This design is ported onto a Xilinx Virtex-7 in Section VI, with the conclusion drawn in Section VII.

II. System Configuration

The proposed transceiver aims to downconvert all 40 channels covering the U.K.'s TVWS spectrum from 470 to 790 MHz. The upconverter in the transmitter must adhere to the strict spectral mask shown in Fig. 1, which regulators are expected

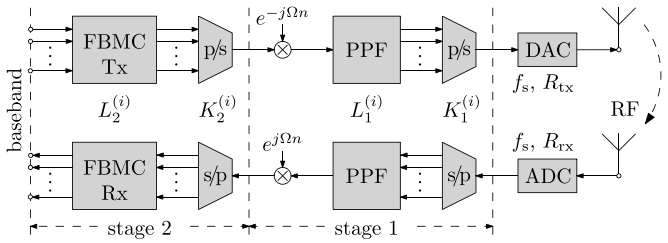

Fig. 2. Proposed multistage TVWS filter bank transmitter (above) and receiver (below) with a PPF in stage 1 and an FBMC modulator in stage 2.

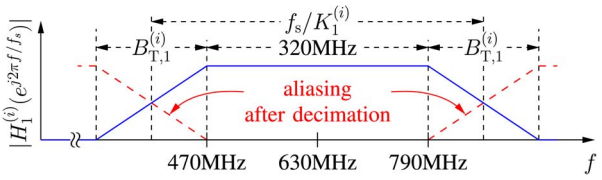

Fig. 3. Stage 1 filter with a passband width of 320 MHz to capture the TVWS spectrum and with transition bandwidth $B_{T,1}^{(i)}$ depending on the selected decimation ratio $K_1^{(i)}$.

to impose [4]. While OFDM-based standards generally exhibit too poor frequency selection to comply with this mask, FBMC systems can provide sufficient frequency selectivity to fulfill this specification.

The implementation of an FBMC system is numerically most efficient with a single filter bank, as it requires fewer coefficients and therefore lower latency than an iterated filter bank with several stages leading to interpolated FIR filters [28]. However, targeting an FPGA implementation, there is a limit to the sampling rate of such devices. Using a polyphase structure, data can be externally multiplexed and demultiplexed into a limited number of streams, with polyphase components running on the FPGA at a lower rate. Therefore, a two-stage approach is adopted, with the proposed transceiver system outlined in Fig. 2.

On the transmitter side—the upper branch in Fig. 2—stage 2 combines 40 TVWS baseband channels each of 8-MHz bandwidth by means of an FBMC synthesis bank into a baseband signal that feeds into stage 1. Stage 1 comprises a PPF, which, together with a position correcting term $e^{-j\Omega n}$, will translate the baseband signal to the UHF range of 470–790 MHz, with a sampling rate f_s and a word length R_{tx}. The real part of the analytic outputs is then fed to a DAC at RF.

The receiver in the lower branch of Fig. 2 operates a dual design to the transmitter. In stage 1, the RF signal is sampled at f_s with word length R_{rx}. A complex-valued polyphase bandpass filter creates an analytic signal which is appropriately modulated with a complex exponential of normalized angular frequency Ω such that the 40 channels of the TVWS spectrum lie flush at dc. In stage 2, an analysis filter bank implementing the FBMC receiver extracts the 40 TVWS baseband channels. Oversampled by a factor of 2, the outputs of the FBMC run at 16 MHz to ease the task of synchronization, subsequent filtering, and further downconversion of the individual 8-MHz channels.

III. Filter Bank Transceiver

This section details the design of the proposed transceiver. Two different designs $i \in \{1, 2\}$ will be proposed, with a decimation/expansion by $K_1^{(i)}$ in stage 1, and $K_2^{(i)}$ channels and a decimation/expansion by $K_2^{(i)}/2$ in stage 2. The computational complexity of the proposed system will be analyzed later in Section IV, but it favors the number of channels in the FBMC $K_2^{(i)}$ to be a power of 2. This differs from a previous design [25], and it will enable the realization on an FPGA to be discussed in Section VI.

A. PPF—Stage 1

In the filter bank receiver, stage 1 extracts the TVWS bands with a center frequency $f_c = 630$ MHz from the RF signal sampled at $f_s = 2.048$ GHz, to create an analytic baseband signal with TVWS channels aligned from dc to 320 MHz. This can be achieved by means of an analytic bandpass filter centered at f_c, whose band limitation will allow decimation by a factor $K_1^{(i)}$. The required filter characteristic is shown in Fig. 3, whereby aliasing is permitted in the transition band, therefore enabling a transition bandwidth $B_{T,1}^{(i)}$

$$B_{T,1}^{(i)} = \frac{2.048\ \mathrm{GHz}}{K_1^{(i)}} - 320\ \mathrm{MHz}. \tag{1}$$

Positive definiteness of (1) admits decimation ratios $K_1^{(i)} \in [1, 4]$. The setting $K_1^{(2)} = 4$ leads to 512-MHz signals which can be realistically interfaced with an FPGA. Instead of filtering at RF and decimating afterward, a polyphase approach will create $K_1^{(2)}$ reduced-rate signals, which are then fed into a polyphase network operating at $f_s/K_1^{(2)}$. The polyphase decomposition of the RF signal was previously accomplished by hardware demultiplexers [25], but instead, the polyphase structure can here be fed by demultiplexed data streams available in recent ADCs such as [6].

The case $K_1^{(1)} < 4$ leads to rates that cannot be directly interfaced with the FPGA, unless oversampled polyphase structures are employed. To demonstrate the tradeoff of a lower decimation in stage 1, we will also be discussing the case $K_1^{(1)} = 2$. The resulting requirements for the design of the PPF $H_1^{(i)}(z)$ are outlined in Fig. 3.

To align the decimated TVWS spectrum with dc, a correction by the lower frequency of 470 MHz after aliasing can be accomplished by selecting $\Omega = 2\pi 470\ \mathrm{MHz} \cdot K_1^{(i)}/f_s$. An alternative implementation would first demodulate the incoming signal by a complex exponential to dc, where a real-valued low-pass filter instead of the bandpass $H_1^{(i)}(e^{j\Omega})$ could be employed. After low-pass filtering, a second modulation step would then realign the decimated TVWS spectrum with dc, although this operation could also be corrected in stage 2 by ensuring that the 8-MHz TVWS channels are extracted by applying appropriate frequency offsets.

The transmitter implementation of stage 1 is a dual of the receiver, with a frequency shift by Ω followed by upsampling. Interpolation can be performed with the bandpass $H_1^{(i)}(e^{j\Omega})$, whereby the widened transition bands do not matter due to the input signal to stage 1 fulfilling tight frequency mask characteristics. The real part of the analytic signal at the bandpass output is then passed to a DAC operating at RF rate. The filter is again implemented in polyphase structure, whereby a polyphase network at $f_s/K_1^{(i)}$ operates on the FPGA

TABLE I
BANDWIDTH REDUCTIONS K_i FOR DIFFERENT RECEIVER STAGES $i = 1, 2$ WITH ASSOCIATED INCREASE IN BIT RESOLUTION ΔR_i AND OTHER PERFORMANCE MEASURES

Design i		1	2
stage 1	$K_1^{(i)}$	2	4
	$\Delta R_1^{(i)}$ / bits	0.5	1
	$L_1^{(i)}$	12	44
stage 2	$K_2^{(i)}$	128	64
	$\Delta R_2^{(i)}$ / bits	3	2.5
	$L_2^{(i)}$	640	320
$C^{(i)}$ / GMAC/s		176.1	213.0
delay $\Delta^{(i)}$ / ns		83.7	40.5
reconstruction error / dB		62.9	63.1
adjacent channel leakage / dB		-65.3	-64.1
next-adj. channel leakage / dB		-71.4	-72.2

with polyphase outputs interfaced to a hardware multiplexer [25]. The latter is often already incorporated in state-of-the-art DACs [7].

B. FBMC System—Stage 2

The two designs for stage 1 necessitate different filter bank approaches for stage 2. With an RF sampling rate of 2.048 GHz and decimations by $K_1^{(i)}$ in stage 1, $K_2^{(i)} = \{128, 64\}$ channels of 8-MHz bandwidth have to be extracted for the three designs in stage 2, respectively, as contained in Table I. For each of the designs, only 40 of the $K_2^{(i)}$ channels will be utilized. Due to their uniform ordering, a modulated filter bank is an efficient approach, which is oversampled by a factor of 2. First, this eases the synchronization efforts of individual TVWS channels in the baseband. Second, oversampling is advantageous as it relaxes the prototype filter $P_2^{(i)}(z)$, which is outlined in Fig. 4, allowing a maximum possible transition bandwidth $B_{T,2}^{(i)}$. This design characteristic assumes that the TVWS channel inputs to Tx stage 2 are perfectly bandlimited to 8 MHz.

We here employ a DFT-modulated filter bank [29], where the analysis filter bank in the transmitter employs an inverse DFT and the synthesis bank in the receiver a DFT, in order to align channels in ascending order from dc to 320 MHz.

IV. IMPLEMENTATION ASPECTS, NUMERICAL EFFICIENCY, AND ROBUSTNESS

This section elaborates on a potential FPGA implementation, focusing on polyphase realizations in Section IV-A, on its computational complexity in Section IV-B, and on word length considerations in Section IV-C.

A. Polyphase Implementations

For stage 1, the receiver requires a hardware demultiplexer to feed $K_1^{(i)}$ polyphase components of the sampled RF signal into the FPGA for polyphase filtering, while in the transmitter, the output of the PPF components is passed out of the FPGA implementation, and it will be multiplexed in hardware to form the RF signal. As mentioned before, such hardware multiplexers are often readily incorporated in state-of-the-art ADCs [6] and DACs [7].

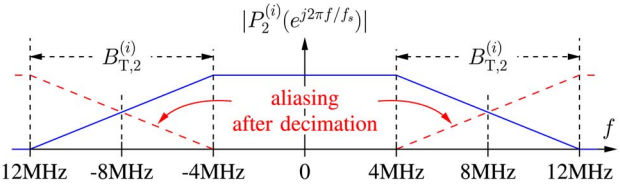

Fig. 4. Stage 2 prototype filter with 8-MHz passband width and decimation to 16-MHz sampling rate. The absolute bandwidths are identical for all designs, which, however, differ in their number of bands $K_2^{(i)}$.

The implementation in Section III-A assumes a complex bandpass PPF, combined with a frequency shift Ω. With a filter length $L_1^{(i)}$, the complexity is $C_1^{(i,a)} = 4L_1^{(i)}/K_1^{(i)} + 4$ real-valued multiply accumulates (MACs). Alternatively, the stage 1 signal could be filtered by a real-valued low-pass filter, requiring a modulation at both the input and output of stage 1, leading to $C_1^{(i,b)} = 2L_1^{(i)}/(K_1^{(i)}) + 4K_1^{(i)} + 4$. The second implementation is only favored if

$$C_1^{(i,a)} > C_1^{(i,b)} \quad \longleftrightarrow \quad L_1^{(i)} > 2\left(K_1^{(i)}\right)^2 \tag{2}$$

which, for the selected values $K_1^{(i)} = \{2, 4\}$, is not satisfied.

For stage 2, different implementations are possible [15]. Since circular buffers are not advantageous for FPGA implementations, we have selected polyphase implementations according to [30], which require only one tapped delay line, a set of multipliers, and the transform on which the modulated filter bank is based, such as in this case a DFT implemented via a fast Fourier transform.

B. Computational Complexity and Latency

With the complexity of the stage 1 filter considered in Section IV-A and the PPF bank requiring $2L_2^{(i)} + 4K_2^{(i)} \log_2 K_2^{(i)}$ MACs [30] at the lower rate of stage 2, the total complexity of a transmitter or receiver as shown in Fig. 2 is given by

$$C^{(i)} = \left(L_1^{(i)} + \frac{L_2^{(i)}}{K_2^{(i)}} + 2\log_2 K_2^{(i)} + 1\right)\frac{4f_s}{K_1^{(i)}} \tag{3}$$

measured in real-valued MACs/s. For stage 2, the complexity of up- and downconverting 40 channels with a DFT-modulated filter bank is the same as that for a single channel, plus the modulating transform, i.e., a $K_2^{(i)}$-point DFT. The overall complexity in (3) is likely to be dominated by the stage 1 filter of length $L_1^{(i)}$ and is listed for the two different implementations in Table I.

The latency of a filter bank transmitter or receiver, assuming linear phase prototype filters, is given by

$$\Delta^{(i)} = \frac{L_1^{(i)}}{2f_s} + \frac{L_2^{(i)}K_1^{(i)}}{2f_s}. \tag{4}$$

The latency will be dominated by the lower rate stage 2 filter, with the overall transmitter or receiver delay for the two implementations shown in Table I.

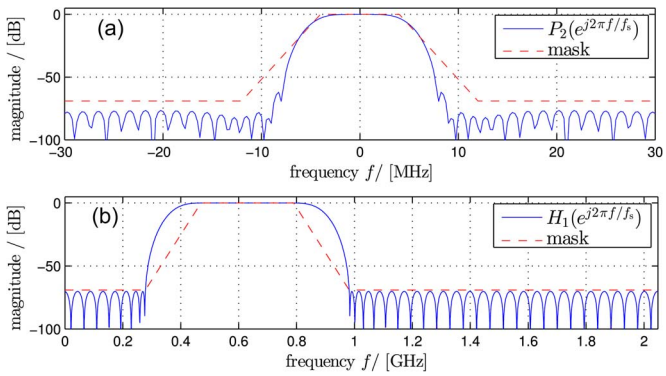

Fig. 5. Magnitude responses of (a) stage 2 and (b) stage 1 prototype filters.

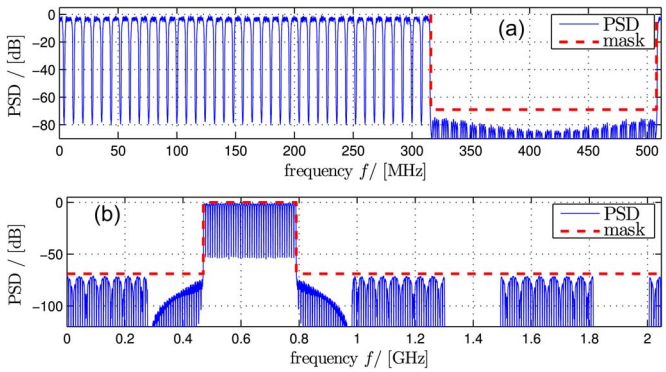

Fig. 6. PSDs of the transmit signal after (a) stage 2 and (b) stage 1. Dashed lines.

C. Word Length Requirements

To achieve the spectral mask as defined in Fig. 1, the transmitter demands a dynamic range of -69 dB [4], which requires at least 12-bit word length all the way up to the DAC. The DAC characterized in [7] offers a word length of $R_{\mathrm{tx}} = 16$ bits. Therefore, we here assume a 16-bit fixed-point resolution for the data as well as for the coefficients of both stage 1 and 2 filters in the transmitter, with a higher resolution for the accumulators and appropriate scaling prior to any rounding.

In the receiver, the succession of filtering and decimation leads to a gain in effective word length, whereby one extra bit of resolution is obtained for every oversampling by a factor of 4, since a reduction in bandwidth also leads to a reduction in noise power without curtailing signal power. Thus, the virtual gain in bits for the proposed filter bank transceiver is $\Delta R = \log_4 K = (1/2)\log_2 K$, where K is the reduction in bandwidth. With the overall reduction in bandwidth from 2.048 GHz to 8 MHz, $K = (2.048\ \mathrm{GHz}/8\ \mathrm{MHz}) = 256$ yields a gain in resolution by $\Delta R = 4$ bits.

The overall gain of $\Delta R = 4$ bits is divided over the different filter bank stages into $\Delta R = \Delta R_1^{(i)} + \Delta R_2^{(i)}$ as shown in Table I for the three different implementations. Thus, the coefficient quantization for each stage has to be selected such that the greatest gain can be realized, requiring an extra resolution of at least 2 and 3 bits for stage 1 and 2 filters compared to their input signals, respectively. With this extra resolution of $\Delta R = 4$ bits, the targeted ADC [6] with $R_{\mathrm{rx}} = 12$ bits therefore provides a resolution of 16 bits for the downconverted 8-MHz TVWS channels given processing with appropriate word lengths throughout the receiver chain.

V. Design, Simulations, and Results

A. Filters and PSDs

The prototype filter for stage 1 is constructed using a minimax design, while stage 2 employs a root Nyquist system [31], [32], with magnitudes shown in Fig. 5. Responses can be seen to satisfy the stopband edges and adjacent channel attenuation of -69 dB imposed by the spectral mask in Fig. 1 [4]. Only design $i = 2$ using $K_1^{(2)} = 4$ and $K_2^{(2)} = 64$ with its simpler stage 1 as discussed in Section III-A and lower latency according to Table I is demonstrated here.

The power spectral densities (PSDs) of simulated Tx signals after stages 1 and 2 are shown in Fig. 6, whereby each TVWS channel is loaded with a 5.33-MHz signal [25]. The stage 2 transmitter output, containing the 320-MHz TVWS baseband across 40 of the $K_2^{(2)} = 64$ channels, is depicted in Fig. 6(a). Fig. 6(b) displays the PSD of the stage 1 output occupying the TVWS band 470–790 MHz with the spectral mask satisfied.

B. Reconstruction Error and Adjacent Band Leakage

Testing the overall filter bank transceiver back-to-back as shown in Fig. 2, the reconstruction error between transmitted and received 5.33-MHz channels, as well as the leakage level into adjacent channels, is provided in Table I. The measured mean square error between the input and the output is equivalent to the reconstruction error of the filter bank and therefore linked to the prototype filter design [31]. Due to the selection of the filter lengths $L_j^{(i)}$ for the jth stage in the ith design to comply with the overall desired spectral mask, all implementations meet the imposed requirement of at least -55 dB for the adjacent and -69 dB for the next-adjacent channels [4].

VI. FPGA Realization

Based on the complexity analysis in Section IV-B, the design $i = 2$ with its more straightforward stage 1 but higher computational complexity has been implemented on a Virtex-7 XC7VX550T using the Xilinx ISE 14.6 software suite. In the transmitter, the word length is maintained at 16 bits throughout all stages to the output. In the receiver, a 12-bit signal is obtained from the ADC, which is allowed to grow by the appropriate gain in resolution up to 13 bits at the output of stage 1 and 16 bits at the output of stage 2, as outlined in Section IV-C. A complex exponential with 16-bit word length performs the frequency shifts in both Tx and Rx.

In order to ensure that the timing requirements were met with stage 1 running at 512 MHz, postplace and route timing analysis was performed. The analysis reported a minimum clocking period of 1.606 ns, giving a maximum operating frequency of 622 MHz. Table II lists the hardware resources used by the design in terms of look-up tables (LUTs), flip-flops (FFs), DSP48E1s, and slices. Fig. 7 shows the PSDs obtained with a bit-true and cycle accurate simulation in Simulink, with the system maintaining its spectral mask compliance.

TABLE II
TRANSCEIVER HARDWARE RESOURCE UTILIZATION ON A VIRTEX7-XC7VX550T FPGA DEVICE

logic utilisation	number used	available	percentage used
LUTs	83566	346400	24%
FFs	63108	692800	9%
slices	26297	86600	30%
DSP48E1 units	1748	2880	60%

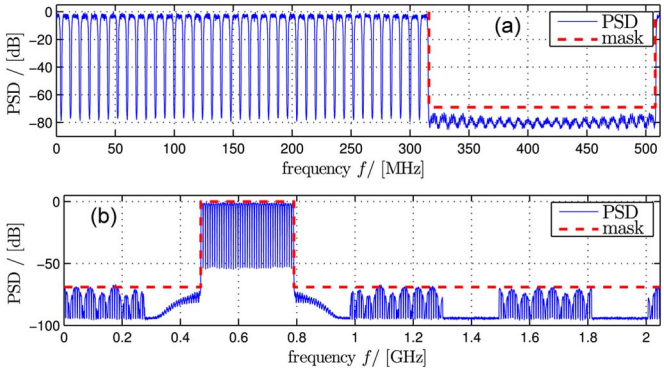

Fig. 7. PSDs after (a) stage 2 and (b) stage 1 obtained by a bit-true and cycle accurate simulation with 16-bit word length.

VII. CONCLUSION

We have discussed a two-stage filter bank transceiver design with the capability to simultaneously up- and downconvert the entire U.K.'s TVWS range of 40 8-MHz wide channels by sampling at the radio frequency. The system satisfies regulatory requirements w.r.t. the spectral mask as well as hardware limitations on the sampling rate and the FPGA devices. Among two discussed parameterizations, a tradeoff between complexity and latency arises. The design exploits additional word length resolution due to oversampling and can cope with fixed-point implementations while still satisfying design requirements. Results of an FPGA implementation have been reported, with the more costly design fitting comfortably onto a Virtex-7 device.

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