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Optimisation of Passive System Components to Minimise DC Circuit Breaker Stresses in Multi-Terminal Systems

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SUMMARY

HVDC circuit breaker designs have commonly included additional series inductance to reduce the rate of rise of current during the initial transient period after a fault occurs, minimising the peak current stress that the circuit breaker must endure. A method of approximating the peak fault current and energy dissipation in a circuit breaker is developed, through circuit analysis of a multi-level converter (MMC) under fault conditions. These approximations are validated against simulation results for an 800kV MMC system.

KEYWORDS

HVDC, Multi-Level Converter, DC Circuit Breakers, Current Limiting Inductors

1 INTRODUCTION

The growth of renewable energy has led to the development of large offshore wind-farms utilising voltage source converter (VSC) based high voltage dc (HVDC) technology, allowing connection over longer distances than is possible with standard HVAC. Voltage source converters facilitate connection to weak ac networks, such as wind-farms, by enabling independent control of both real and reactive power flows. Their fixed polarity voltage more readily enables networked HVDC when compared to line commutated (LCC) converter based systems [1]. HVDC networks allow the interconnection of multiple wind farms and shore connections, so that redundancy is achieved and capital expenditure is reduced [2].

Two-level and half-bridge multi-level VSC converters are, however, susceptible to dc-side faults, which result in high fault current and rapid voltage collapse that, due to low network impedance, can propagate over large distances to other converter stations within milliseconds.

DC circuit breakers, for HVDC applications, have been developed to allow the faulted area of a network to be quickly isolated, with minimal impact on the healthy parts of the network which can then continue to exchange power during the fault [3-5]. The high projected cost of circuit breakers, which is a function of their complexity, volume and operational requirements, is however an impediment to the realisation of multi-terminal HVDC networks. Optimisation of passive components has the potential to reduce circuit breaker operating requirements, and therefore cost.

2 DC REACTOR OPTIMISATION

The requirements for high voltage, current and speed HVDC circuit breakers (DCCB) has led to complex, expensive and bulky designs. During faults voltage collapses rapidly, leading to a high rate of rise of current during the initial transient period. Proposed circuit breaker designs intended for high-speed operation in VSC systems have included additional series inductance, as shown in Figure 1, to reduce this rate of rise so that peak current stress is reduced in the circuit breaker [6].

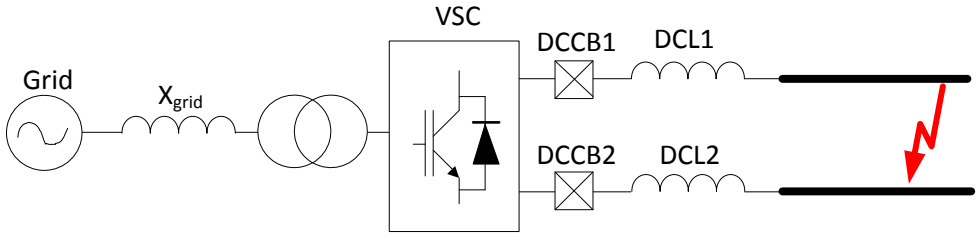

Figure 1: Location of additional dc inductance (DCL)

At present, inductor sizing appears to be driven by the maximum capability of the circuit breaker technology [3]. As new mechanical circuit breaker designs increase the current breaking capability, the amount of dc inductance (DCL) may no longer be driven by restrictions of circuit breaker technology [4]. In this case, any additional inductance should be sized in order that the whole system cost, including the capital costs of the dc circuit breaker, associated peripherals (such as dc inductance) and steady-state losses, can be minimised.

2.1 Typical Results – Impact of DC Inductance

To demonstrate the effect of additional dc inductance (DCL), Figure 2 shows simulation results, produced using the model described in Section 4, for three different values of DCL. So that the natural response of the system can be observed, circuit breakers are not operated.

Over the one second time period following the fault, the steady-state current in all three cases settles to approximately 20kA, as shown Figure 2a. However, the current magnitude during the initial transient period, shown in Figure 2b, is closely related to the amount of additional inductance. Typical circuit breaker designs for VSC HVDC applications operate within a 2ms to 10ms time-frame, enabling the

exploitation of the significant reduction in peak current during this initial transient that results from the inclusion of additional inductance.

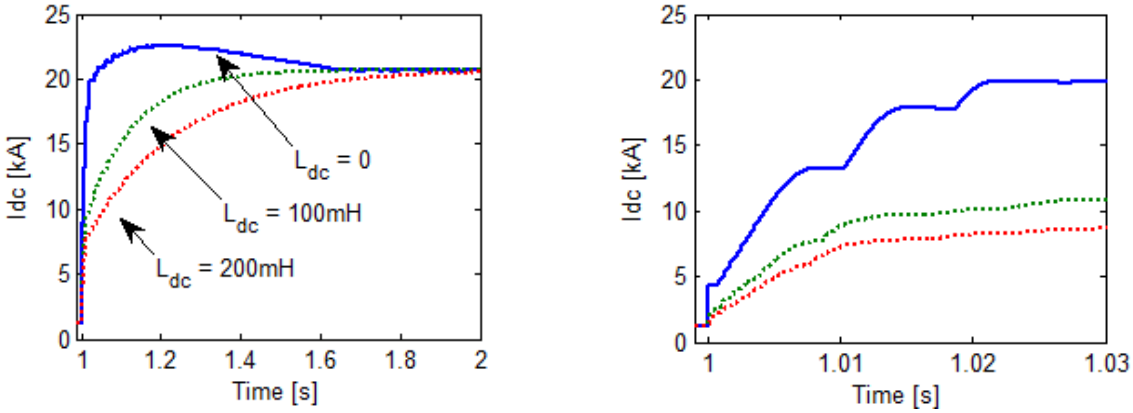

Figure 2: Typical current profiles during dc fault (a) for DCL=0, 100 and 200mH, and (b) expanded view

3 DC CIRCUIT BREAKER STRESS ESTIMATION

Through circuit analysis, simplification and approximation, the circuit breaker peak current and energy dissipation requirements may be estimated for a given value of dc inductance and system configuration. The analysis is performed for a pole-to-pole fault at the cable/overhead line interface, where there is minimum impedance between the fault and driving voltage source. This condition results in the largest current stress. Further, the converter is blocked, by inhibiting all IGBTs, immediately following the fault. This assumption facilitates a simplified equivalent circuit.

3.1 Peak Current

The network and transformer impedances are referred to the converter side to simplify analysis, as shown in Figure 3a. If the circuit breakers open within a short space of time and the influence of commutation between phases is minimal, then it can be assumed that fault current is built up mainly in the two phases with the greatest line-to-line voltage. Fault current will conduct through the upper arm of the most positive phase and return through the lower arm of the most negative phase. The other arms can, therefore, be neglected. During this time, the diodes in series with the cell capacitors are reverse biased and can also be neglected. The faulted system can therefore be reduced to the equivalent circuit shown in Figure 3b.

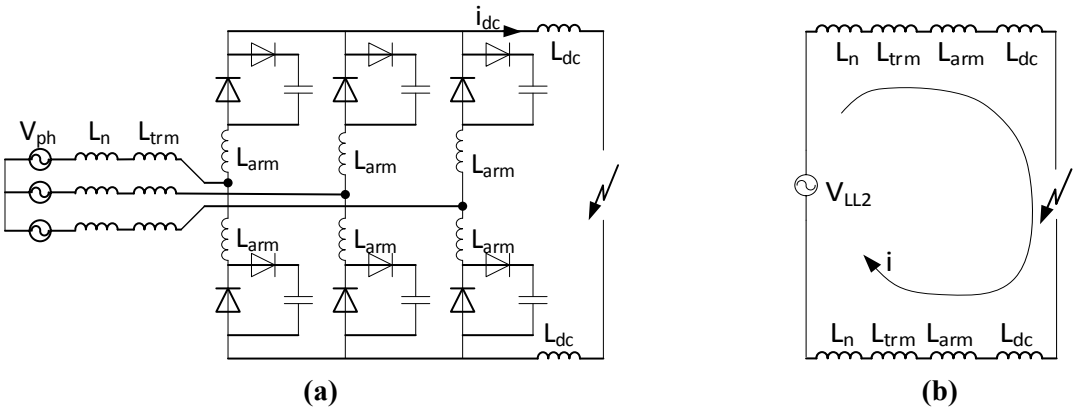

Figure 3: (a) AC network and MMC equivalent circuit under fault, and (b) simplified equivalent circuit

During the short period before the circuit breaker opens, converter current is composed of fault current and pre-fault current components. The additional fault current contribution over the time period can be approximated by (1), where T_{cb} is the breaker opening delay and L_{ac}=(L_n,+L_{trm}+L_{arm}), as defined in Table 1.

$$\Delta I = \frac{\sqrt{2}V_{LL2}}{2(L_{\mathrm{ac}} + L_{\mathrm{dc}})} T_{cb} \tag{1}$$

For positive initial power, i.e. from the ac side to the dc side, the pre-fault and fault currents are additive, generating a larger peak current. Therefore, the peak current through the circuit breaker may be approximated by (2), where I_0 is the pre-fault current flow in the dc line.

$$\hat{I} = \Delta I + I_0 \tag{2}$$

For negative initial power flow, the current through the dc inductance must increase through zero before further increasing in the positive direction. Assuming the converter is blocked immediately after the fault, this pre-fault current must pass through the cell capacitors, as shown in Figure 4.

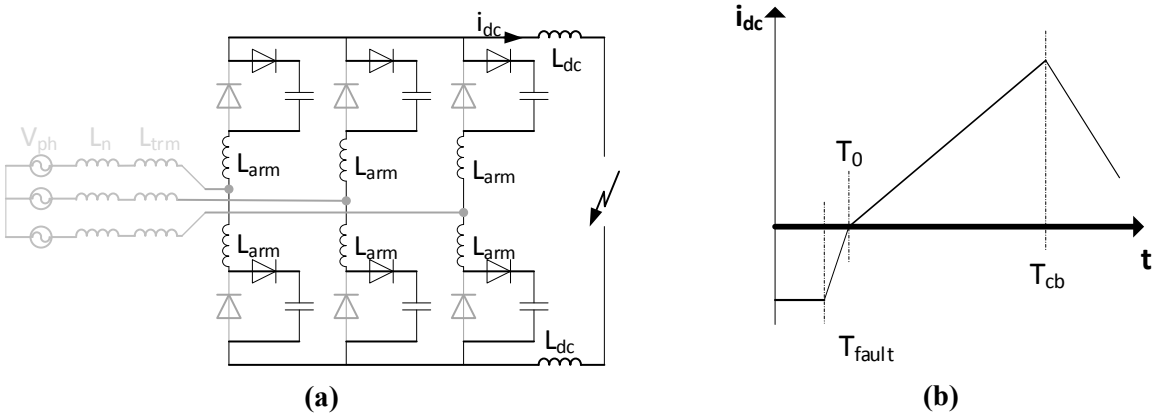

Figure 4: Current path for negative initial power flow

Assuming that the capacitor voltages remain nearly constant at V_{dc}, while energy is transferred from the dc inductance, the time for the dc current to reach zero can be approximated by (3).

$$T_0 = \frac{L_{dc}}{V_{\mathrm{dc}}} I_0 \tag{3}$$

The time period over which the dc current increases is correspondingly reduced by this amount. Therefore, the peak current stress, when power flow is initially negative, can be approximated by (4).

$$\hat{I}_{dc} = \frac{\sqrt{2}V_2}{2(L_{\mathrm{ac}} + L_{\mathrm{dc}})} (T_{cb} - T_0) \tag{4}$$

3.2 MOV Energy Dissipation

When the circuit breaker opens, the ratio of dc to ac inductance influences the voltage present at the interface between the converter and L_{dc}. If the ratio L_{dc}:L_{ac} is small the voltage at the converter terminals will rise. This voltage is, however, clamped by the cell capacitors once it reaches the cumulative voltage in one arm, i.e. V_{dc}. In this case, the time period for the current to reach zero can be approximated by (5).

$$\Delta T_{\mathrm{cb}} = \frac{2L_{\mathrm{dc}}}{V_{\mathrm{cb}} - V_{\mathrm{dc}}} \hat{I}_{dc} \tag{5}$$

As the amount of dc inductance is increased, and the ratio L_{dc}:L_{ac} increases, a larger proportion of the voltage is dropped across L_{dc} so that the voltage at the converter terminals may not rise to V_{dc} and the cell capacitors will not clamp. In this case the time for current to reach zero can be approximated by (6), where V_{ac} is there effective applied ac voltage.

$$\Delta T_{cb} = \frac{2(L_{\text{ac}} + L_{\text{dc}})}{V_{\text{cb}} - V_{\text{ac}}} \hat{I}_{dc} \tag{6}$$

Energy is dissipated in each of the circuit breakers whilst dc current decays from its peak value. Ideal waveforms for the dc current, circuit breaker voltage and energy dissipation are shown in Figure 5.

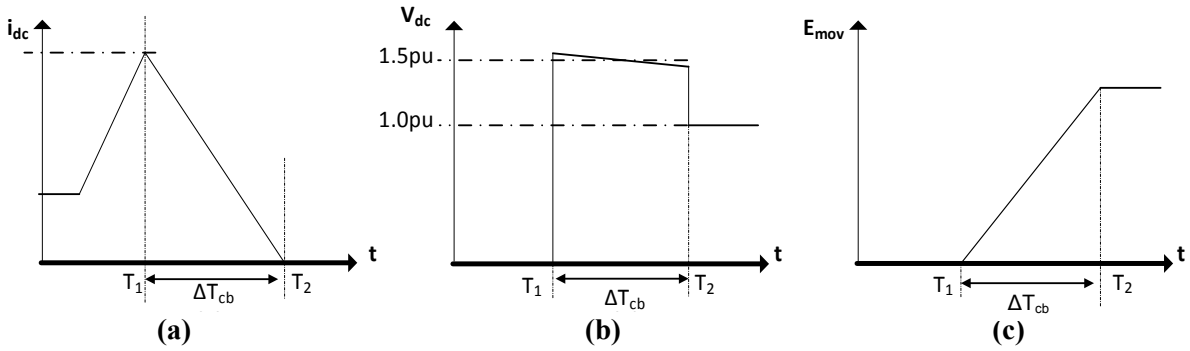

Figure 5: Idealised waveforms for (a) dc current, (b) circuit breaker voltage, and (c) MOV energy

Given that (5) and (6) are linear, and that $\overline{I}_{\text{dc}}$ can be approximated by $\hat{I}_{\text{dc}}/2$, then the energy dissipation in a single circuit breaker may be approximated by (7).

$$E_{\text{dccb}} = \overline{I}_{\text{dc}} \overline{V}_{\text{cb}} \Delta T_{\text{cb}} \tag{7}$$

4 VALIDATION

To verify the estimated peak current and energy dissipation, faults were simulated for a range of dc inductances and the resulting peak currents and energy dissipation recorded.

A point-to-point network was used for the study, allowing initial power flow to be established prior to the fault being applied, whilst also reducing simulation complexity. DC circuit breakers are placed at the positive and negative poles of each converter station, as shown in Figure 6, and are operated 5ms or 10ms after the fault is applied. DC circuit breaker measurements are taken from DCCB11.

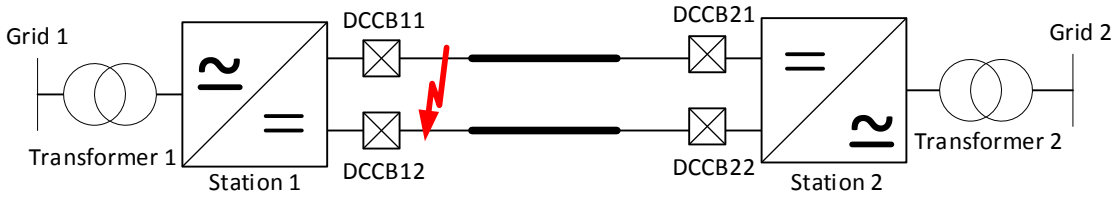

Figure 6: Point-to-point system used to validate circuit breaker peak current and energy estimates

A fault is initiated one second into the simulation, and the circuit breakers are opened after a time delay T_{cb}. The simulation study examines system performance for dc inductance values in the range 10mH-410mH. To ensure that the method used is valid over a range of initial conditions, simulations are carried out where pre-fault power flow is +1GW, 0 and -1GW. Peak current and circuit breaker energy dissipation are recorded in each simulation case. For positive power flow current is estimated using (2), for zero power flow current is estimated using (1), and for negative power flow current is estimated using (4), where the system parameters are defined in Table 1.

Table 1: System Parameters

Parameter		Value	Notes
V_{dc}	DC voltage	800kV	Pole-to-pole
S_c	Rated power of converter	1000MW	0.95 power factor
V_{LL1}	Nominal ac network voltage	400kV	Line-to-line RMS
V_{LL2}	Nominal converter side voltage	392kV	Line-to-line RMS
L_{trm}	Transformer leakage impedance	0.2pu	92.9mH (referred to converter side)
L_{arm}	Arm inductor impedance	0.05pu	46.5mH per arm
S_n	AC network strength	10GVA	L_n=48.9mH (referred to converter side)
V_{cb}	DCCB clamping voltage	600kV	1.5pu system voltage

5 COMPARISON OF RESULTS

The simulated and approximated peak current and circuit breaker energy dissipation are compared for different circuit breaker operating speed, represented by the time delay T_{cb}. To assess the estimation method under different conditions, simulations were carried out for power flows of P = ±1GW and P = 0, using the system shown in Figure 6.

5.1 Circuit Breaker Delay = 5ms

The simulated and approximated peak currents in the circuit breaker, for each of the power flow conditions, are shown in Figure 7, where the circuit breaker is opened 5ms after the fault is applied. When dc inductance is small and the pre-fault power flow is positive (contributing to fault current), representing the worst case, there is approximately a 5% error between simulated and predicted peak circuit breaker current.

There is approximately 1.75kA difference between the maximum (corresponding to P=+1GW) and minimum (corresponding to P=-1GW) peak currents over the range of dc inductance. This difference constitutes a significantly higher percentage of the peak current magnitude as the value of dc inductance increases.

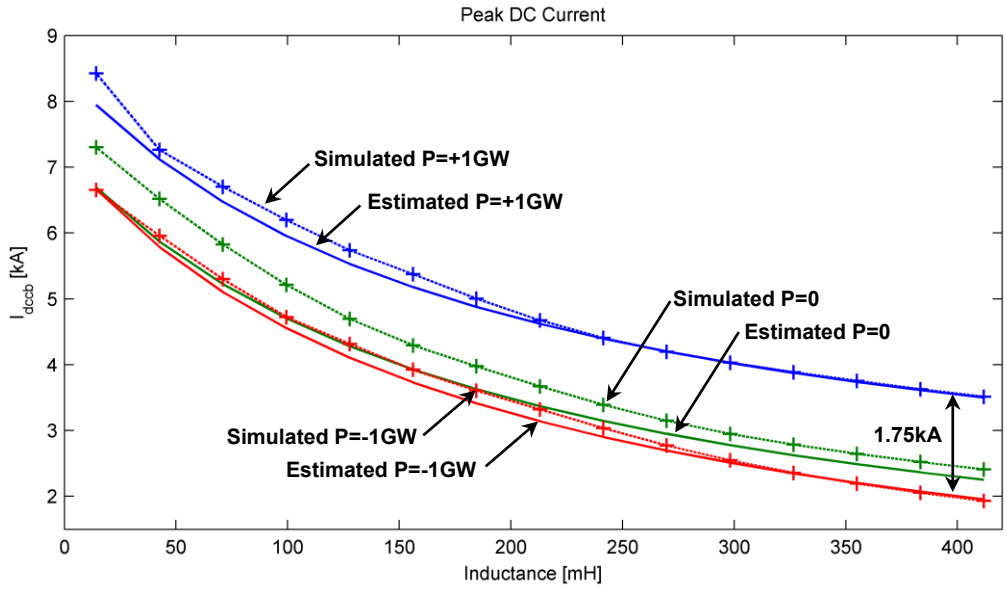

Figure 7: Comparison of simulated and estimated dc circuit breaker peak currents, with T_{cb} = 5ms

Figure 8a presents simulated DCCB energy dissipation for power flows P = ±1GW and P = 0. As with the peak current measurements, energy dissipation is higher when pre-fault current flow contributes additively to fault current. Figure 8b-d compare estimated and simulated energy dissipation for the three power flow cases. Equation (7) is used to calculate the energy dissipation based on the estimated current decay time. In the region where L_{dc}:L_{ac} is approximately less than unity, the capacitors conduct clamping the voltage, and the decay time may be estimated from (5).

As the ratio L_{dc}:L_{ac} is increased, (5) is no longer valid and (6) must be used to estimate current decay time. The effective ac driving voltage V_{ac} is affected by the phase relationship between the ac grid voltage and current, set by the point on the ac wave at which the fault occurs and the current commutation through the converter diodes. Maximum circuit breaker energy dissipation (E_{max}) occurs when the ac voltage is effectively in phase with the ac current ($V_{ac} = \sqrt{2}V_{LL2}$), whilst minimum energy dissipation (E_{min}) occurs when the ac voltage and current are orthogonal ($V_{ac} = 0$). In each case, curves are shown for estimated maximum energy E_{max}, minimum energy E_{min}, and the average, E_{ave}, of these two values. The simulation results show a maximum error of approximately 20% when L_{dc} = 180mH, corresponding to L_{dc}:$L_{ac} \approx 1$. For L_{dc} > 180mH, the results show good agreement with the estimated average energy E_{ave}.

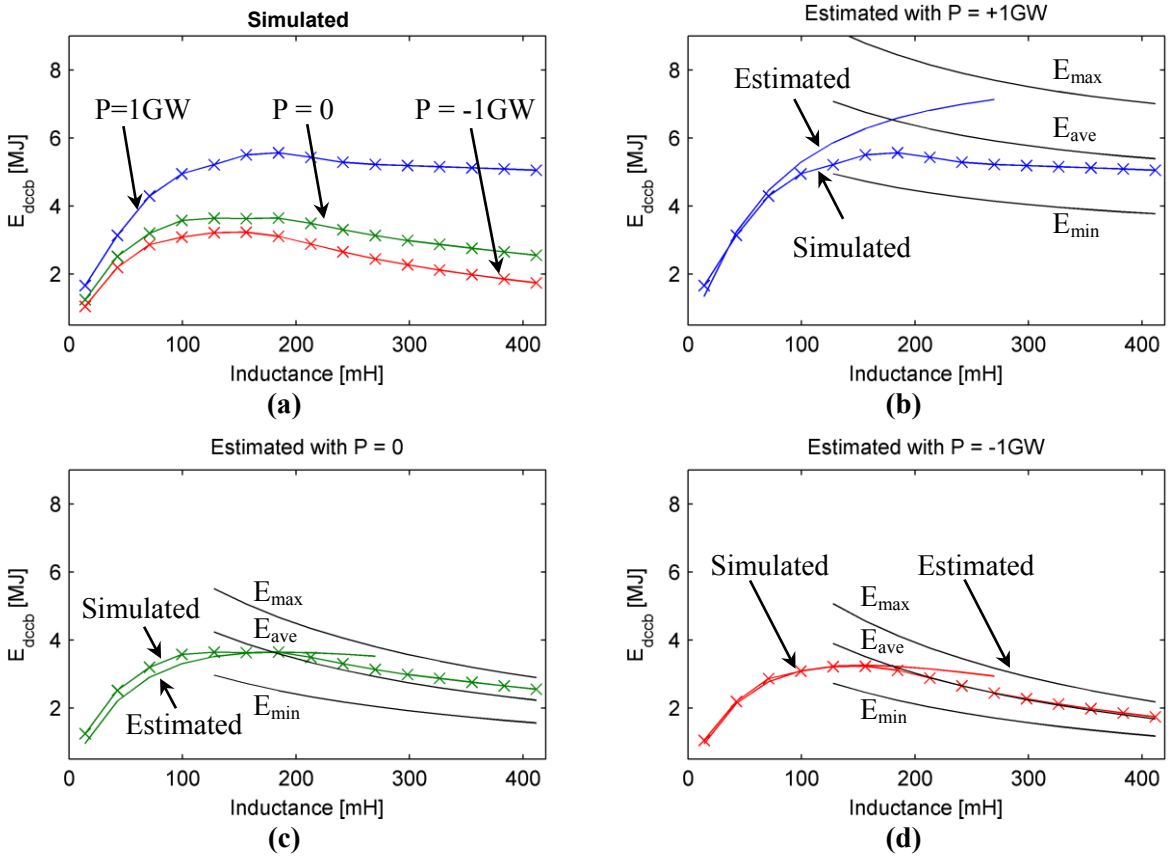

Figure 8: Comparison of simulated and estimated DCCB energy dissipation for initial power flows of +1GW, 0 and -1GW, with T_{cb} = 5ms

5.2 Circuit Breaker Delay = 10ms

High-speed, mechanical dc circuit breakers, currently under development, have operational speeds in the region of 10ms [4]. Results of a simulation study assessing the performance of the system containing a dc breaker operating in this time-frame, and using additional dc inductance to reduce the peak current, are presented.

Figure 9 compares the simulated and estimated peak dc currents for a range of additional dc inductance values, with T_{cb} = 10ms. For low values of L_{dc}, and P = +1GW, there is an approximate 35% error between the estimated and simulated results. Peak current estimations, obtained using (1),

(2) and (4), are based on the assumption that circuit breaker operates within a few commutation periods and that the influence of commutation between converter arms is minimal. However, with T_{cb} = 10ms, the current build up takes place over several commutation periods and the effective voltage at the ac side is reduced because of commutation effects. This leads to larger errors between the estimated and simulated results than for those found when T_{cb} = 5ms. As the dc inductance is increased the error reduces significantly, to approximately 10%. This may be attributed to the lower current, and therefore the smaller commutation overlap.

From Figure 7, with T_{cb} = 5ms and L_{dc} = 50mH, peak current is approximately 7.5kA. Simulation results presented in Figure 9 show that the same result may be achieved using a mechanical circuit breaker with a 10ms opening time, and approximately 175mH of additional dc inductance.

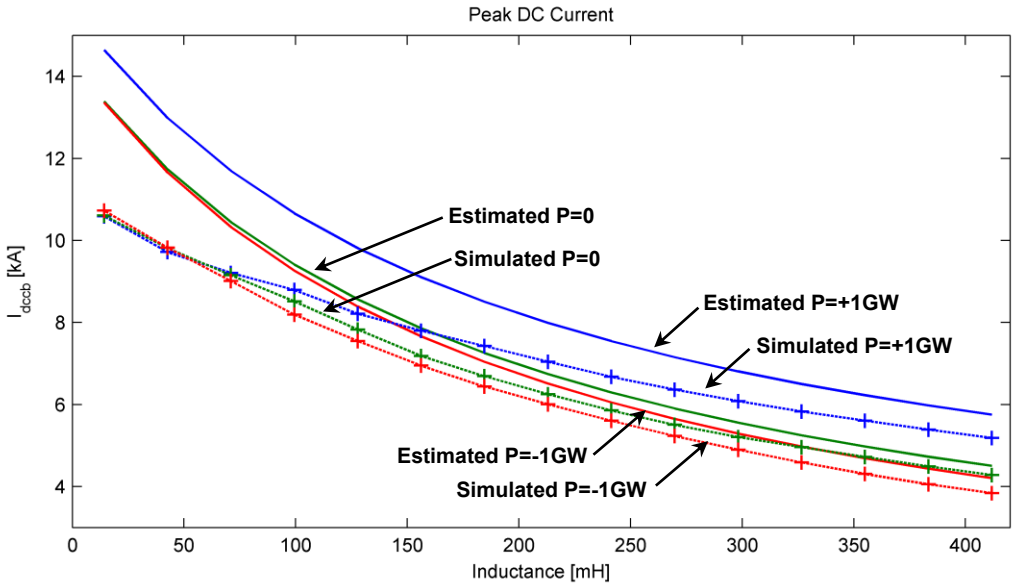

Figure 9: Comparison of simulated and estimated dc circuit breaker peak currents with T_{cb} = 10ms

Figure **10** compares estimated and simulated energy dissipation for the three power flow conditions, with T_{cb} = 10ms. Equation (7) is used to calculate the energy dissipation based on the estimated current decay times, calculated by (5) for the clamping and (6) non-clamping conditions.

When (7) is combined with (5) or (6), an $\hat{I}_{dc}{}^{2}$ term is introduced. Therefore, the error in peak current estimation is compounded in the estimation of energy dissipated, leading to an increased error (see Figure 10). Where L_{dc} is small and the error in estimated peak current is largest, the error in estimated energy dissipation is significant for this reason.

As L_{dc} is increased, the energy dissipation estimate improves as the error in peak current estimate decreases. When L_{dc} is greater than approximately 180mH, the lower bound estimate for energy dissipation agrees more closely with that from simulation. The simulation results show that, for the worst case, DCCB energy does not exceed 10MJ even after L_{dc} is increased beyond 180mH.

6 CONCLUSION

Empirical simulation results have shown that additional dc inductance can be an effective tool for reducing the peak current stress in dc circuit breakers. As these inductors form part of the main conduction path, they must be designed to ensure low power loss. The requirement for dc, high-current operation poses practical design challenges. The cost and scale of dc circuit breakers for high-voltage applications are closely related to their peak current capability. The reduction in peak current offered by dc inductors may therefore be sufficient to justify their inclusion.

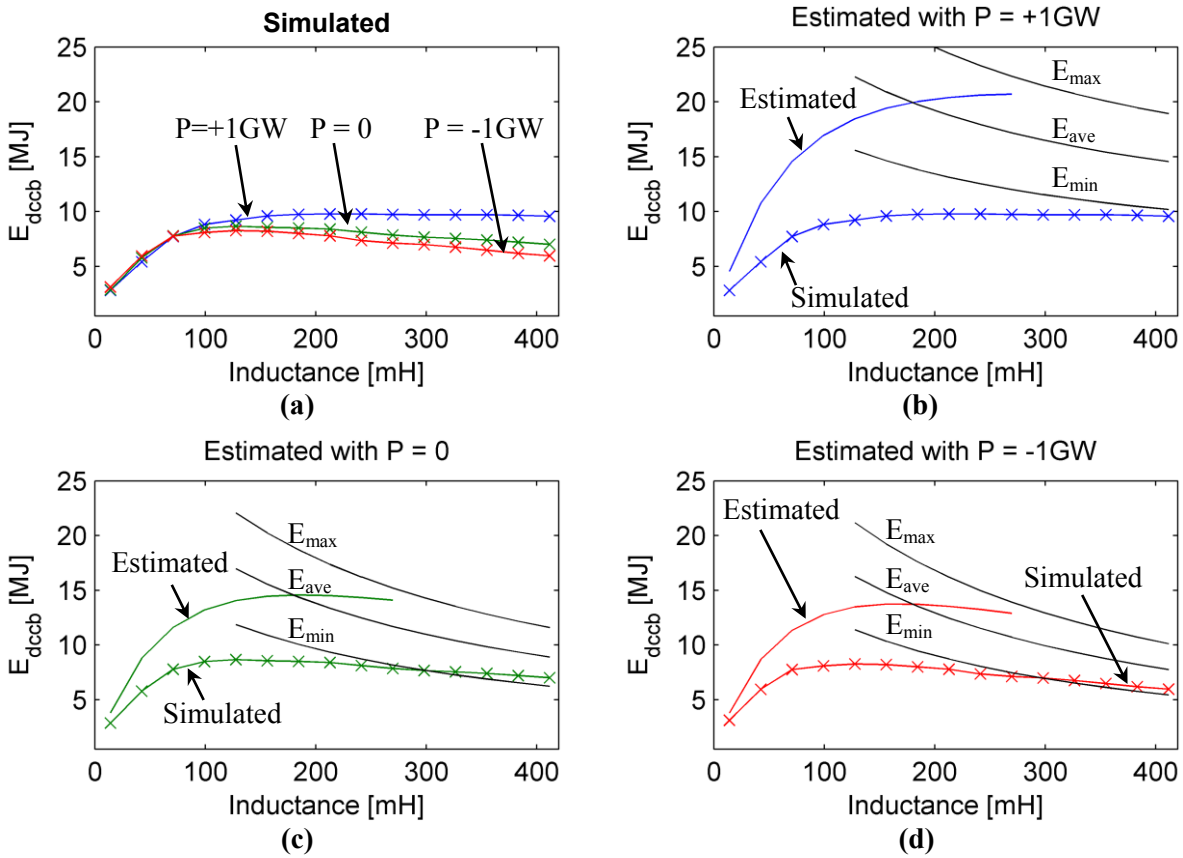

Figure 10: Comparison of simulated and estimated DCCB energy dissipation for initial power flows of +1GW, 0 and -1GW, with Tcb = 10ms

Key performance indices of fault current rise and DCCB energy dissipation are dependent upon the transient response of the converter over a number of commutation cycles. Accurate figures for these quantities can only realistically be obtained through time-domain simulation, which requires extensive parametric studies to identify trends and interactions resulting from component choice. The approximate mathematical analysis presented facilitates understanding of the underlying factors which relate parameter choice, peak current and DCCB energy.

The method of estimating circuit breaker peak current requirement has been shown to produce results that are accurate to within 10% of values obtained through simulation, when assuming very short DCCB opening time. The analysis has also enabled estimation of circuit breaker energy dissipation. Maximum and minimum energy dissipation boundaries have been defined according to converter parameters, allowing the cost and scale of circuit breaker surge arresters to be estimated.

When considering a mechanical circuit breaker with 10ms opening time, the assumptions used to estimate peak current and energy dissipation become less valid when the additional dc inductance is small. Comparison of simulated and estimated results show that as the inductance increases, the error reduces. To further improve accuracy, the effect of commutation between the converter arms must also be considered.

Although thorough analysis is required for individual system studies, the technique provides an indicative tool for estimation of the influence of dc inductance on peak current and energy dissipation. It is sufficient to enable initial assessment of the trade-off between additional capital cost, footprint and losses associated with the inclusion of additional dc inductance, and the cost associated with a higher performance circuit breaker, prior to performing detailed simulation studies.

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