New Emerging Voltage Source Converter for High-Voltage Application:
Hybrid Multilevel Converter with dc Side H-Bridge Chain Links

G.P. Adam and B.W. Williams

Abstract—Hybrid multilevel converters are more attractive than the traditional multilevel converters, such as modular converters, because they offer all the features needed in a modern voltage source converter based dc transmission system with reduced size and weight, at a competitive level of semiconductor losses. Therefore, this paper investigates the viability of a hybrid multilevel converter that uses dc side H-bridge chain links, for high-voltage dc and flexible ac transmission systems. Additionally, its operating principle, modulation and capacitor voltage balancing, and control are investigated. This paper focuses on response of this hybrid multilevel converter to ac and dc network faults, with special attention paid to device issues that may arise under extreme network faults. Therefore the hybrid multilevel converter with dc side chain links is simulated as one station of point-to-point dc transmission system that operates in an inversion mode, with all the necessary control systems incorporated. The major results and findings of subjecting this version of the hybrid converter to ac and dc networks faults are presented and discussed.

I. INTRODUCTION

Recently, a number of mixed topologies voltage source converters, known as hybrid multilevel converters, have been proposed [1-6]. These hybrid converters aim to optimize converter key performance indices during operation in power systems. The main indices for HVDC converters are [7-12]: output current and voltage quality, resiliency to ac and dc network faults, conversion losses, and modularity and footprint. Hybrid converters discussed in the literature during the last decade include the hybrid multilevel converter (HMC) with ac side cascaded H-bridge cells, H-bridge alternative arm modular multilevel converter, HMC with half or full bridge cascaded cells connected across the dc link, and HMC with dc side cascaded H-bridge chain links [3, 6, 12-18].

Among the hybrid topologies mentioned, the HMC with ac side cascaded H-bridge cells investigated in [2, 5, 19, 20] has achieved dc fault reverse blocking capability with fewer H-bridge cascaded cells, hence it is anticipated to have smaller footprint than other topologies, including the well established half and full bridge modular multilevel converters. In addition, it has higher dc link voltage utilization because it uses the H-bridge cell floating capacitors as a virtual dc link to increase the maximum fundamental voltage. However, its major drawbacks are high conversion losses, and requires a number of tuned

filters to attenuate the 5th and 7th harmonics that may arise from mis-synchronization of the two-level converter (main high power stage) and H-bridge cascaded cells (series active filter stage). Without such filters, the converter transformer may be exposed to excessive *dv/dt* from the low energy spikes shown in [19].

The H-bridge alternative arm modular multilevel converter proposed in [3, 21] is attractive for HVDC applications as it has the dc fault reverse blocking capability feature, with lower conversion losses than HMC with ac side cascaded cells, and with half the number of cells of the modular multilevel converter. Reduced converter losses are achieved by operating the converter upper and lower arms in a complementary manner, with each arm operating for half fundamental cycles plus a small overlap period (the period where both arms operate together). The overlap period is introduced to ensure soft current commutation between the upper and lower arms. However, the converter arms experience a large inrush current during overlap when the phase currents are lagging or leading their corresponding fundamental phase output voltages. Also, restoration of the cell capacitor voltages to a pre-disturbance state following dc side faults is slower than with the hybrid converter with ac side cascaded H-bridge cells and the modular multilevel converter. This is because cell capacitor voltage balancing is achieved over several fundamental cycles rather sub-cycle as with other converter topologies.

A HMC with half or full bridge cells connected across dc link presented in [6, 21] is promising for high-voltage applications as it has the same number of cells per phase and footprint as the hybrid converter with ac side cascaded H-bridge cells for the same dc link voltage and ac side voltage. However, its main drawback is that the voltage stress on the converter switches cannot be maintained tightly around a specific set-point when the converter adjusts its terminal voltage relative to grid voltage when manipulating reactive power exchange with the grid. This compromises converter voltage control and black start capability, which is necessary in applications such as connection of offshore wind farms and power restoration to ac networks following blackout. However, the authors in [6] attempted to address this shortcoming, exploding unconventional 3rd harmonic injection.

The HMC with dc side cascaded chain links presented in [21] is suited for high-voltage dc and flexible ac transmission systems (HVDC and FACTS), see Fig. 1. However, reference [21] does not provide detailed discussion of the converter operation and control, and its response to different network faults. In addition, some of the potential attributes and limitations of this type of hybrid converter in high-voltage applications are not highlighted. Therefore, this paper aims to discuss the operating principle and control of the HMC with dc side cascaded H-bridge cells, followed by detailed exploration of its responses to ac and dc network faults. Additionally, the impact of the ac and dc network faults on the converter switching devices voltage and current stresses will be assessed. To achieve these objectives, the hybrid converter with dc side cascaded H-bridge cells is simulated as HVDC transmission stations, with basic control systems detailed in the test system in Fig. 2.

II. HYBRID MULTILEVEL CONVERTER WITH DC SIDE CASCADED H-BRIDGE CHAIN LINKS

(A)Operating principle and capacitor voltage balancing

Fig. 1 shows the three-phase hybrid converter with N_c dc side cascaded H-bridge chain links. Total voltage across the cascaded H-bridge cells must equal the full dc link voltage (V_{dc}), thus the voltage across each H-bridge cell capacitor must be maintained at V_{dc}/N_c. Each H-bridge cell generates three voltage levels $\pm V_{dc}/N_c$, and 0. The cascaded H-bridge cells in each phase are controlled using $v_{HB}(t) = V_{dc}\left[1 - m \times \sin(\omega t - \phi) \times \text{sign}\left(\sin(\omega t - \phi_x)\right)\right]$ to generate the multilevel voltage waveform shown in top left of Fig. 1 (phase a), where m is modulation index, x stands for phases a, b and c, and $\phi_a=0$, $\phi_b=-⅔\pi$ and $\phi_c=⅔\pi$. In this manner, the voltage across the H-bridge cells is subtracted from the main dc link voltage to produce a rectified voltage $v_m(t)$ across the main H-bridge cell as shown in Fig. 1. The polarity of $v_m(t)$ is reversed during the negative half of each fundamental cycle of the target modulating signal '$v_x(t)=m\sin(\omega t+\phi_x)$' by controlling the appropriate switching devices of the main bridge to synthesize the converter phase output voltage waveform shown in the top right of Fig. 1. In this paper, the staircase modulation is realized without calculation of the switching angles as in the fundamental frequency switching; instead it is realized by direct tracking of the reference voltage. The voltage step which is equal to the voltage across one cell capacitor is defined as $b= V_{dc}/N_c$, therefore the number of H-bridge cell capacitors selected to realize each voltage level in the H-bridge voltage waveform $v_{HB}(t)$ is defined by $a=round(v_{HB}(t)/b)$. Based on the polarity of the current flowing in the H-bridge cells, the bi-polar capability of each H-bridge cell is exploited to maintain converter cell capacitor voltage balancing by flipping polarities of the inserted cell capacitors in the power path in a manner that allows them to charge and discharge in order to ensure zero active power exchange with the ac side. By incorporating this capacitor voltage balancing into the modulation process, the number of cell capacitors must be subtracted from and added to the main dc link voltage are determined by $X=a+floor(½(N_c-a))$ and $Y= floor(½(N_c-a))$ respectively. Using this approach, at least one cell capacitor needs to be bypassed during every sampling period. Implementation of such modulation and capacitor voltage balancing requires sorting of the cell capacitors in ascending and descending order. The sampling period is selected so as to permit insertion of the capacitors needed to synthesize the peak fundamental voltage corresponding to the maximum modulation index during a quarter of the fundamental period. On this basis, the minimum sampling frequency f_s required can be expressed in terms of the number of cells and the fundamental frequency, f, by $f_s \geq 4N_c f$. In general, the modulation and capacitor voltage balancing of the H-bridge cells of the hybrid converter used in this paper are summarised as follow:

a) Sort the cell capacitors in ascending and descending order using [A, IX]=sort(Vc, 'ascend') and [B, IY]=sort(Vc, 'descend') respectively. V_c represents vector matrix of the cell capacitor voltages; A and B are sorted vector matrices of the cell capacitors in ascending and descending order; and IX and IY are index matrices that contain the order of the elements of A and B in the original matrix V_c during each sampling period.

b) Considering the voltage level '*a*' needed to be synthesized in each phase, the number of cells to be subtracted 'X' and added 'Y' to the main dc link voltage 'V_{dc}' are identified as previously defined.

c) Taking into account the current polarity through the H-bridge cells, the generic code is summarized in Table I. $S_x(k,i)$ represents the state of switch i^{th} in the k^{th} cell, where i=1,2,3 and 4, k=1,2,...N_c. $S_x(k,1)$ and $S_x(k,3)$ represents the states of the two top switches in the H-bridge number k^{th}, and $S_x(k,2)=1-S_x(k,1)$ and $S_x(k,4)=1-S_x(k,3)$.

Table I: Generic code for selection of the appropriate H-bridge cell capacitor voltage magnitudes, accounting for the current polarity in each arm

$I_d \geq 0$	$I_d < 0$
for j=1:Nc	*for j=1:Nc*
if(j<=X)	*if(j<=X)*
$S_x(IX(j),1)=0;$	$S_x(IY(j),1)=0;$
$S_x(IX(j),3)=1;$	$S_x(IY(j),3)=1;$
elseif(j>X&j<=X+Y)	*elseif(j>X&j<=X+Y)*
$S_x(IX(j),1)=1;$	$S_x(IY(j),1)=1;$
Sx(IX(j),3)=0;	$S_x(IY(j),3)=0;$
else	*else*
$S_x(IX(j),1)=1;$	$S_x(IY(j),1)=1;$
$S_x(IX(j),3)=1;$	$S_x(IY(j),3)=1;$
end	*end*
end	*end*

The total voltage waveform across the H-bridge chain links of each phase can be expressed as:

$$v_{HB}(t) = V_{dc} - \sum_{j}^{a} V_{cj} \qquad (1)$$

For a large number of H-bridge cells, the summation term in (1) can be replaced by $mV_{dc}\left|\sin(\omega t + \varphi_x + \delta)\right|$, therefore, (1) may be written as:

$$v_{HB}(t) = V_{dc} - mV_{dc}\left|\sin(\omega t + \phi_x + \delta)\right| \qquad (2)$$

Where δ is the load angle (angle of the fundamental voltage of the converter terminal voltage measured relative to grid voltage or voltage at the bus where the input to phase locked loop is taken).

From Fig. 1, the rectified voltage waveform $V_m(t)$ across the high-voltage main bridge can be expressed by:

$$v_m(t) = V_{dc} - v_{HB} = mV_{dc}\left|\sin(\omega t + \phi_x + \delta)\right| \qquad (3)$$

The ac voltage across at the terminal of the high-voltage main bridge of each phase is defined by:

$$\begin{aligned} v_{a1}(t) &= mV_{dc}\left|\sin(\omega t + \phi_x + \delta)\right| \operatorname{sign}\left(\sin(\omega t + \phi_x + \delta)\right) \\ &= mV_{dc}\sin(\omega t + \phi_x + \delta) \end{aligned} \qquad (4)$$

Equation (4) shows that the hybrid converter with dc side cascaded H-bridges can generate twice the fundamental voltage of other voltage source converter topologies that modulate their dc link voltage between -½V_{dc} and ½V_{dc} (such as the modular converter). This means that the hybrid converter with dc side cascaded cells can output twice the power of other converter

topologies using the same dc link voltage and current stress on the switching devices. This is one of the innocuous features of this type of hybrid converter that can be used to increase converter power rating, without footprint expansion.

The voltage across each H-bridge cell capacitor is:

$$v_c(t) = \frac{1}{C}\int i_y dt \qquad (5)$$

where i_y represents the average current flow of each cell capacitor over one sampling period, and can be defined by assuming all the cell capacitors are evenly utilized over 0 to π using:

$$i_y(t) = \begin{cases} \frac{I_m}{N_c}(1 - m\sin(\omega t + \delta + \phi_x))\sin(\omega t + \phi_x + \varphi) \end{cases} \qquad (6)$$

Assume the phase output current is $i_x = I_m \sin(\omega t + \phi_x + \varphi)$; where φ represents the power factor angle and I_m is the phase current amplitude. Substituting (6) into (5) the following expression for cell capacitor voltage is obtained:

$$v_c(t) = \frac{I_m}{N_c C}\int \begin{bmatrix} \sin(\omega t + \phi_x + \varphi) - \frac{1}{2}m\cos(\varphi - \delta) \\ +\frac{1}{2}m\cos(2\omega t + \delta + 2\phi_x + \varphi) \end{bmatrix} dt \qquad (7)$$

$$v_c(t) = \frac{I_m}{N_c \omega C}\begin{bmatrix} -\cos(\omega t + \phi_x + \varphi) - \frac{1}{2}m\cos(\varphi - \delta)\times\omega t \\ +\frac{1}{4}m\sin(2\omega t + \delta + 2\phi_x + \varphi) \end{bmatrix} + K \qquad (8)$$

Assuming that the cell capacitors are fully charge at t=0, $v_c(0) = \frac{V_{dc}}{N_c}$, therefore the integral constant K is obtained as $K = \frac{V_{dc}}{N_c} + \frac{I_m}{\omega N_c C}\left[\cos(\phi_x + \varphi) - \frac{1}{4}m\sin(\delta + 2\phi_x + \varphi)\right]$. Therefore, the approximate expression of cell capacitor voltage is rearranged as:

$$v_c(t) = \frac{V_{dc}}{N_c} + \frac{I_m}{N_c \omega C}\begin{bmatrix} \cos(\phi_x + \varphi) - \frac{1}{4}m\sin(\delta + 2\phi_x + \varphi) \\ -\cos(\omega t + \phi_x + \varphi) - \frac{1}{2}m\cos(\varphi - \delta)\times \mathrm{mod}(\frac{\omega t}{2\pi}) \\ +\frac{1}{4}m\sin(2\omega t + 2\phi_x + \delta + \varphi) \end{bmatrix} \qquad (9)$$

Equation (9) shows that the cell capacitor voltage ripple and the drift of the final settling point from V_{dc}/N_c depends on phase current magnitude, load power factor φ, load angle δ, modulation index m, and cell capacitance. In addition, equation (9) states that for a large number of cells per phase and properly sized cell capacitance, the cell capacitor voltage ripple and drift from the desired set-point V_{dc}/N_c tends to be sufficiently small and mainly determined by $I_m/\omega CN_c$ (note that the terms inside the parenthesises are in per units and small). For example, for a converter with a 320kV dc link, 100 cells per phase (N_c=*100*), C=*1mF*, cell capacitor rated to block 3.2kV in steady-state at rated current $I_m = 1200\sqrt{2}$ A and ω=100π, $\frac{I_m}{\omega CN_c} = 54V$, which is approximately 1.7% the rated capacitor voltage.

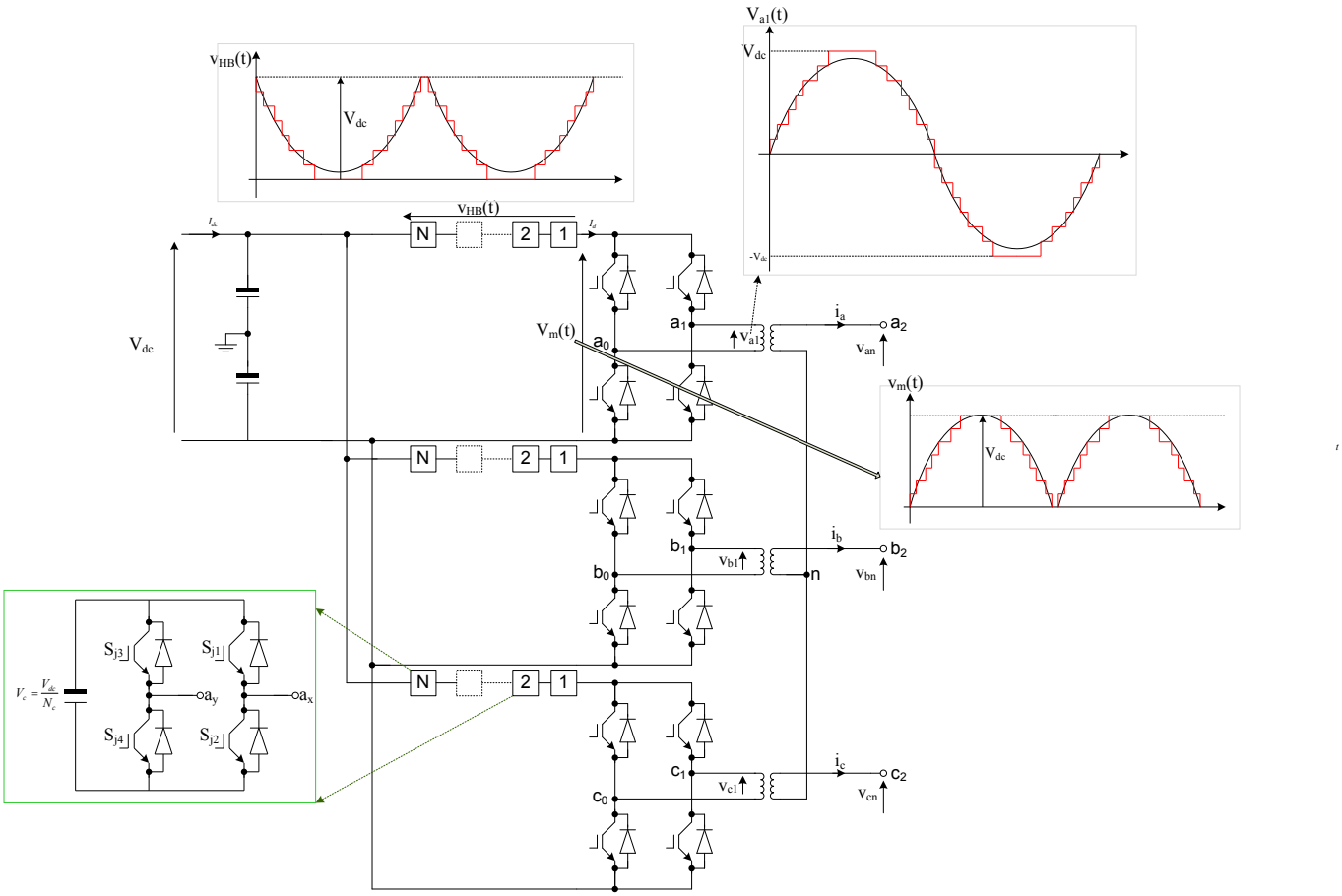


Fig. 1: Three-phase hybrid multilevel converter with dc side cascaded H-bridge cells

The total energy the dc side H-bridge cell capacitors exchange with the ac side can be estimated as follows:

$$\begin{aligned} W &= \int v_{HB}(t) i_x(t) dt \\ &= \int I_m V_{dc} \sin\left(\omega t + \phi_x + \varphi\right)\left(1 - m\sin(\omega t + \delta + \phi_x)\right) dt \\ &= \frac{V_{dc} I_m}{\omega}\left[\begin{array}{l} -\cos(\omega t + \phi_x + \varphi) - \frac{1}{2} m \cos(\varphi - \delta) \times \mathrm{mod}(\frac{\omega t}{2\pi}) \\ +\frac{1}{4} m \sin(2\omega t + 2\phi_x + \delta + \varphi) \end{array}\right] + K_1 \end{aligned} \quad (10)$$

Assuming the same initial operating condition used to obtain K_1 from (8), $W(0) = N_c \times \frac{1}{2} C\left[\frac{V_{dc}}{N_c}\right]^2 = \frac{1}{2}\frac{CV_{dc}^2}{N_c}$, K_1 is $K_1 = \frac{1}{2}\frac{CV_{dc}^2}{N_c} + \frac{V_{dc} I_m}{\omega}\left[\cos(\phi_x + \varphi) - \frac{1}{4} m \sin(2\phi_x + \delta + \varphi)\right]$. Therefore the total energy of the H-bridge cell capacitors, including the fluctuating component is:

$$W = \frac{1}{2}\frac{CV_{dc}^2}{N_c} + \frac{V_{dc} I_m}{\omega}\left[\begin{array}{l} \cos(\phi_x + \varphi) - \frac{1}{4} m \sin(2\phi_x + \delta + \varphi) \\ -\cos(\omega t + \phi_x + \varphi) - \frac{1}{2} m \cos(\varphi - \delta) \times \mathrm{mod}(\frac{\omega t}{2\pi}) \\ +\frac{1}{4} m \sin(2\omega t + 2\phi_x + \delta + \varphi) \end{array}\right] \quad (11)$$

The energy per capacitor W_1 can be expressed by:

$$W_1 = \frac{W}{N_c} = \tfrac{1}{2}C\left[\frac{V_{dc}}{N_c}\right]^2 + \frac{V_{dc}I_m}{\omega N_c}\begin{bmatrix}\cos(\phi_x+\varphi)-\frac{1}{4}m\sin(2\phi_x+\delta+\varphi)\\ -\cos(\omega t+\phi_x+\varphi)-\frac{1}{2}m\cos(\varphi-\delta)\times\mathrm{mod}(\frac{\omega t}{2\pi})\\ +\frac{1}{4}m\sin(2\omega t+2\phi_x+\delta+\varphi)\end{bmatrix} \quad (12)$$

The constant terms enclosed in parentheses in (9) and (12) represent the drift in the cell capacitor voltage, and the accumulated energy in the cell capacitors needed to be eliminated by the capacitor voltage balancing strategy. $\frac{1}{2}C\left[\frac{V_{dc}}{N_c}\right]^2$ represents the energy each cell capacitor must store in order to be able to maintain its voltage at V_{dc}/N_c. The time dependent terms represent the fluctuating components that cause the cell capacitor voltage to oscillate around V_{dc}/N_c.

(B)Control system

The control system adopted in this paper to assist with the illustration of the steady-state and transient performance of the HMC, is comprised of active and reactive power loops and an ac voltage loop that adjusts the converter reactive power exchange with the grid at B_1 in order to maintain the voltage at bus B_1 (see Fig. 2). The active and reactive powers are designed with the assumption that the voltage vector at B_1 is aligned with the *d*-axis of the *d-q* synchronous reference frame that is rotating with speed ω. Assuming (i_d, i_q), (v_d, v_q) and (E_d, E_q) are *d-q* components of the current and voltages i_{abc}, v_{abc} and E_{abc} respectively. Therefore, the converter ac side dynamics at fundamental frequency, which are associated with power generation, can be expressed as:

$$\frac{di_d}{dt} = -R_t/L_t\, i_d + (E_d - v_d + \omega L_t i_q)/L_t \quad (13)$$

$$\frac{di_q}{dt} = -R_t/L_t\, i_q + (E_q - v_q - \omega L_t i_d)/L_t \quad (14)$$

Assuming the voltage magnitude at B_1 is maintained constant, thus the currents i_d and i_q in (13) and (14) can be replaced by P/v_d and $-Q/v_d$, (where v_q=0, and P and Q are converter active and reactive power output); then (13) and (14) can be written with P and Q representing the state variables as follow:

$$\frac{dP}{dt} = -R_t/L_t\, P + [(E_d - v_d)v_d - \omega L_t Q]/L_t \quad (15)$$

$$\frac{dQ}{dt} = -R_t/L_t\, Q - [E_q v_d - \omega L_t P]/L_t \quad (16)$$

Let $u_d = (E_d - v_d)v_d - \omega L_t Q$ and $u_q = -E_q v_d + \omega L_t P$ be estimated using a simple proportional integral (PI) controller as $u_d = \alpha_p(P^* - P) + \alpha_i\int(P^* - P)dt$ and $u_q = \alpha_p(Q^* - Q) + \alpha_i\int(Q^* - Q)dt$, where α_p and α_i are the proportional and integral gains. After replacing the integral parts of u_d and u_q with λ_d and λ_q, and substituting u_d and u_q in (15) and (16), the following equations described the decoupled control of active and reactive powers:

$$\begin{bmatrix} \frac{dP}{dt} \\ \frac{d\lambda_d}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{(R_t+\alpha_p)}{L_t} & \frac{1}{L_t} \\ -\alpha_i & 0 \end{bmatrix} \begin{bmatrix} P \\ \lambda_d \end{bmatrix} + \begin{bmatrix} \frac{\alpha_p}{L_t} \\ \alpha_i \end{bmatrix} P^* \qquad (17)$$

$$\begin{bmatrix} \frac{dQ}{dt} \\ \frac{d\lambda_q}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{(R_t+\alpha_p)}{L_t} & \frac{1}{L_t} \\ -\alpha_i & 0 \end{bmatrix} \begin{bmatrix} Q \\ \lambda_q \end{bmatrix} + \begin{bmatrix} \frac{\alpha_p}{L_t} \\ \alpha_i \end{bmatrix} Q^* \qquad (18)$$

Note the feed-forward terms in Fig. 2 are obtained from the output of the power controller u_d and u_q as $E_d = \left(u_d + v_d^2 + \omega L_t Q\right)/v_d$ and $E_q = \left(u_q + \omega L_t P\right)/v_d$.

The gains for the active and reactive power controller are selected using $\alpha_p = \frac{8}{T_s} L_t$ and $\alpha_i = \frac{16 L_t}{\zeta^2 T_s^2}$, where ζ and ω_n are damping and the natural frequency, and $T_s = \frac{4}{\zeta \omega_n}$ represents settling time. Reactive power reference Q^* is obtained from the ac voltage controller as $Q^* = \beta_p(|v_{abc}^*| - |v_{abc}|) + \beta_i \int (|v_{abc}^*| - |v_{abc}|) dt$, where β_p and β_i are the proportional and integral gains of the ac voltage controller. The overall control system used in this paper is summarised in Fig. 2. Note an unconventional version of third harmonic injection is exploited in Fig. 2, which enhances cell capacitor voltage balancing by extending the region around the zero voltage level, ensuring the dc link voltage is modulated between *0* and V_{dc} regardless of modulation index. It has been established that the amount of 3rd harmonic needed for cell capacitor voltage balancing is $E_{3rd} = (m-1)\sin 3(\theta + \delta)$, where *m* is modulation index and δ is the load angle (the angle of the converter terminal voltage *E* relative to that at the point of common coupling at B_1).

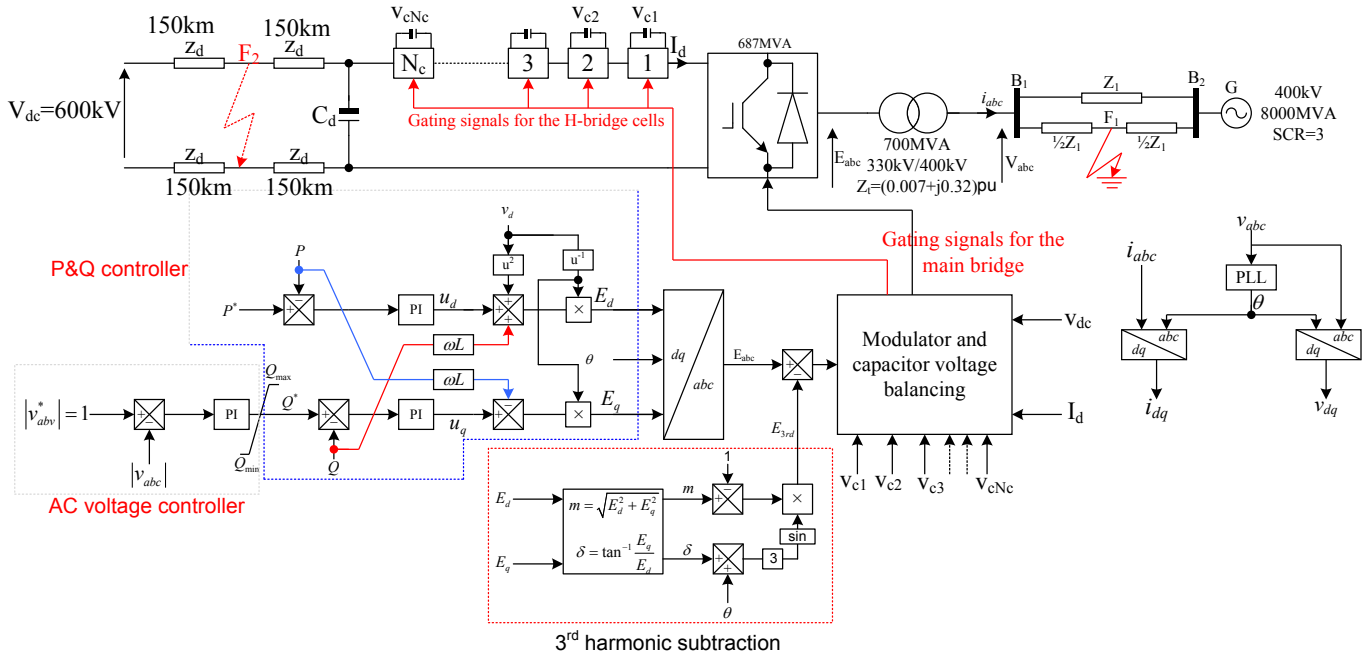


Fig. 2: Test system and control system used throughout this paper
(main dc link capacitance=30μF; H-bridge cell capacitance=400μF; dc cable parameters: resistance=0.01Ω/km, inductance=0.5mH/km, and capacitance=0.2nF/km; ac cable lines parameters: resistance=0.0127Ω/km, inductance=0.9337mH/km and capacitance=12.74nF)

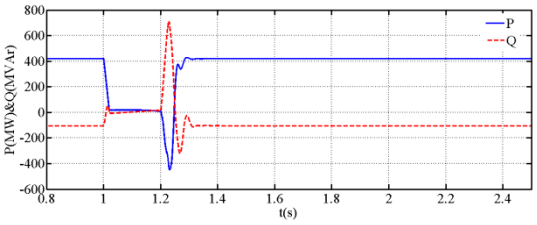
III. Performance Evaluation

This section assesses the transient response of the HMC with dc side cascaded H-bridge cells to ac and dc network faults. The assessment is conducted when a hybrid converter with 11 H-bridge cells per phase is simulated as a HVDC transmission system station, with the control system summarised in Fig. 2. The power circuit of hybrid converter in Fig. 2 is represented in detail, with each H-bridge cell and main bridge modelled using the universal bridge from the power electronic library of the SimPower system in Matlab-Simulink. In the universal bridge, the switching device (IGBT and its freewheeling diode) mimics conduction of the physical device. Modulation and capacitor voltage balancing is written in the S-function format and incorporated within the Simulink environment to run with the time basis of the power circuit. The control system is built using discrete blocks available in the Simpower system library. All the results presented are obtained when the hybrid inverter in Fig. 2 injects 0.7pu (420MW) active power to grid, regulating the ac voltage at B_1 at 1.0pu, assuming the converter has static reactive power limits of ±0.9pu (±450MVAr).

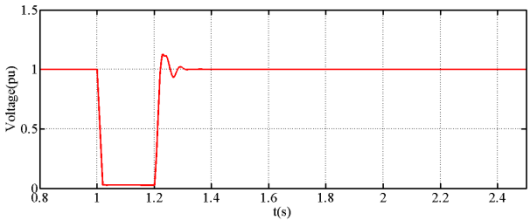
A) AC fault

Fig. 3 displays simulation results when the test system in Fig. 2 is subjected to a temporary three-phase fault at F_1, with a 200ms fault duration. Figs. 3a and 3b show inverter active and reactive power exchange with the grid at B_1, and voltage magnitude at B_1. Despite the large voltage depression at B_1 as a result of fault at F_1, the hybrid converter with dc side cascaded H-bridge cells is able recover to the pre-fault condition, with the proposed power controller successfully restraining current injection into fault, as expected and shown in Fig. 3c. The zoomed version of the inverter current around the fault period displayed in Fig. 3d shows that hybrid converter injects a high quality current waveform into grid, without the need of ac side

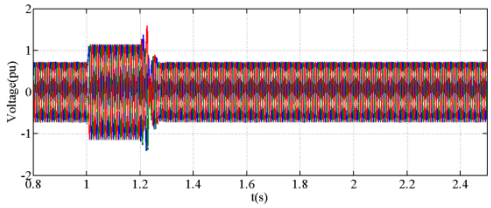
filters (except transformer leakage inductance). Fig. 3e shows that the voltage stresses on the converter switches remains controlled as the voltages across the dc side cascaded H-bridge cell capacitors are tightly maintained, with a maximum voltage excursion of less than 5%. Also, the hybrid converter presents a high quality voltage waveform to converter transformer with low harmonic content and *dv/dt* (Fig. 3f). Fig. 3g presents a sample voltage waveform across the dc side cascaded H-bridge cells of a phase during steady-state. Observe that operating the hybrid converter in this manner minimizes the number of switching transitions per phase, hence switching losses. Based on the results presented in Fig. 3 it can be concluded that the presented hybrid converter is promising and competitive to the modular multilevel converter in high-voltage applications, as it offers all the features needed in modern VSC-HVDC transmission systems.



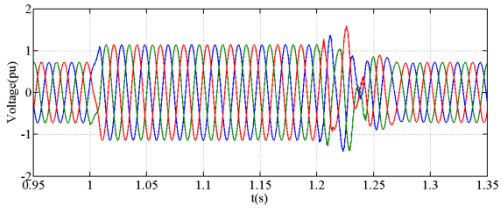
a) Active and reactive power at B_1



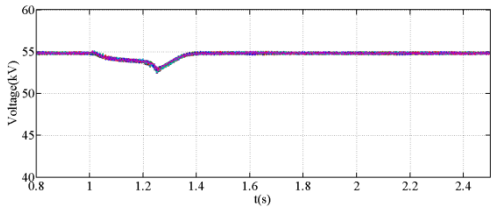
b) Voltage magnitude at B_1



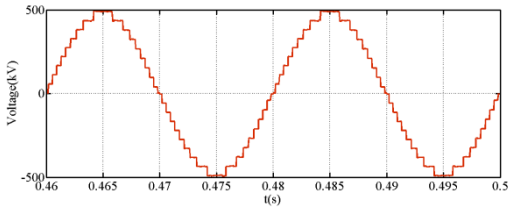
c) Current waveforms inverter injects into B1



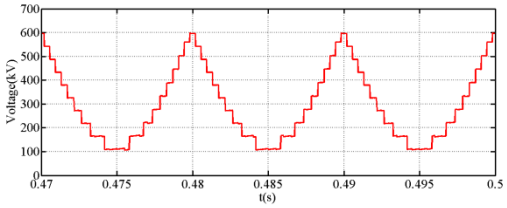
d) Inverter current zoomed around fault period



e) Voltage across the 33 H-bridge cell capacitors of the three phases



f) Phase voltage inverter presents to converter transformer (THD=4.8%)



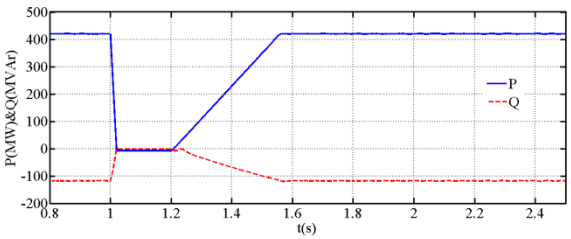
g) Sample of the voltage across the phase H-bridge cells

Fig. 3: Response of hybrid multilevel converter with dc side cascaded H-bridge cell to three-phase ac network fault

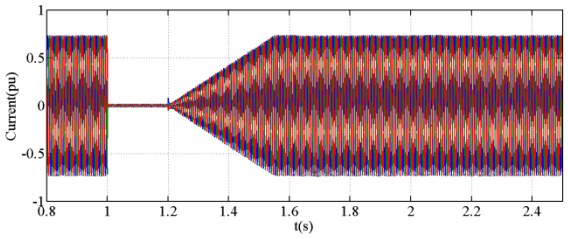
B) DC fault

To illustrate hybrid converter response to dc side faults, the test system in Fig. 2 is subjected to pole-to-ground and pole-to-pole dc network faults at F_2, of 200ms fault duration. In an attempt to prevent uncontrolled current flow in the converter switches and minimize transients following fault clearance and during the restoration period, the gating signals to converter switches are inhibited and the active power command is reduced to zero. The gating signals are restored immediately the fault is cleared, while the active power command is ramped up gradually to pre-fault value of 0.7pu with a slope of 4pu/s.

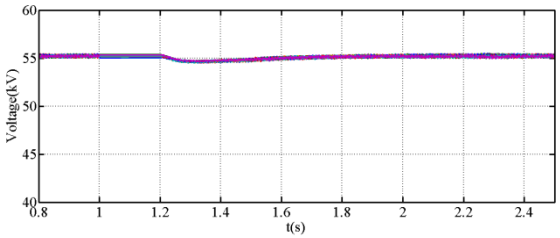
Fig. 4 presents results for a pole-to-ground dc fault at F_2. Figs. 4a, 4b and 4c show that the HMC with dc side cascaded H-bridge cells is able to ride through the pole-to-ground dc fault, without exposing the ac system and converter switches to over-current and over-voltages. Additionally, Figs. 4a and 4b show that the hybrid converter successfully blocks the power path between the ac and dc sides, thus it exchanges zero active and reactive powers with the grid at B1, and no current flows in the converter switches. Fig. 4c shows the H-bridge cell capacitors experience limited disturbance during the pole-to-ground dc side fault.



a) Active and reactive power converter exchanges with B1



b) Current waveforms hybrid converter injects into B1



c) Voltage across the 33 H-bridge cell capacitors of the three phases

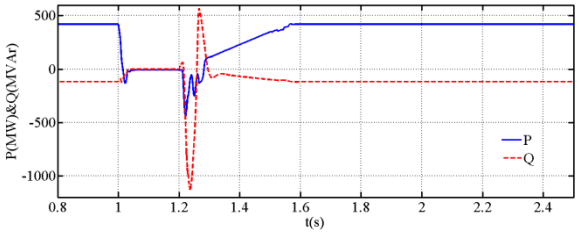
Fig. 4: Response of hybrid converter with dc side cascaded H-bridge cells to pole-to-ground dc side fault

Furthermore, to examine the resiliency of the hybrid converter to a worse case dc side fault, the test system in Fig. 2 is subjected to pole-to-pole dc fault at point F2, with a 200ms fault duration. Fig. 5 displays simulation results when the hybrid converter with dc side cascaded H-bridge cells is subjected to a pole-to-pole dc side fault. Results presented in Figs. 5a and 5b show that the hybrid converter recovers from the worse case fault scenario, and eliminates any uncontrolled current in-feed from the ac side to the dc side. However, the converter switches experience a significant inrush current during restoration, as the converter main dc link capacitor and cable distributed capacitors recharge rapidly from the ac side in an attempt to establish the pre-fault dc voltage level. Fig. 5c shows the pole-to-pole dc fault exposes the nearby ac networks to significant voltage depression during the restoration period. Fig. 5d shows the voltages across the H-bridge capacitors of the hybrid converter are maintained during the fault period (when converter is blocking), but suddenly drop close to zero during the restoration period. Energy transfers rapidly from the H-bridge cell capacitors in an attempt to support the dc link voltage build up. This recharge of the dc side capacitors during the system restoration period causes a significant reduction in cell capacitor voltages. Such an extreme and abrupt drop in cell capacitor voltage is not acceptable, as it will create a large inrush current in the dc side that may damage the converter switches. Proper sizing of the H-bridge cell capacitor may minimize the cell capacitor voltage drop. Also small current limiting inductance in series with the H-bridge cells is needed to keep the inrush current within tolerable limits.

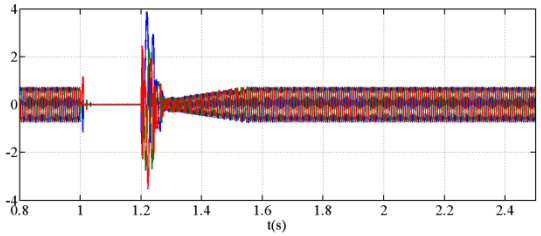
Fig. 6 shows the voltage across the H-bridge cells of the three phases for different cell capacitances C_m. For smaller cell capacitance the voltage across the cell capacitors experience a larger reduction and recover faster; while the reduction in capacitor voltages is significantly reduced, but much slower to recover with larger cell capacitance. This means the overall

energy stored in cell capacitors must be several times greater than that in the dc link main capacitor plus dc line distributed stray capacitors. Such a condition can be satisfied for shorter HVDC links, but is difficult for longer links.

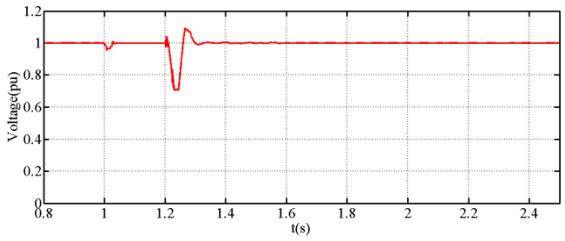
Based on the results presented in Figs. 4, 5 and 6 it can be concluded that the hybrid converter is a promising candidate for HVDC links that employ underground and submarine cables where the likelihood of pole-to-pole dc faults are extremely rare.



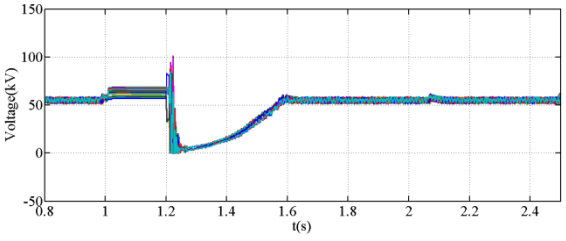
a) Active and reactive power at B1res



b) Current waveforms inverter injects into B1



c) Voltage magnitude at B1



d) Voltage across the 33 H-bridge cell capacitors of the three phases

Fig. 5: Response of the hybrid converter with dc side cascaded H-bridge cell to solid pole-to-pole dc network fault.

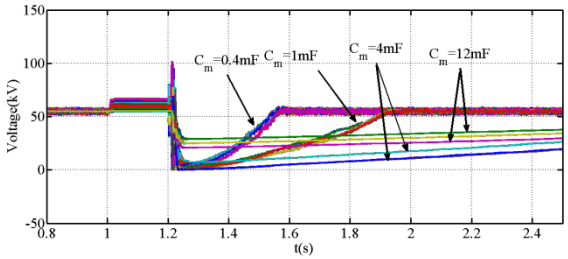


Fig. 6: Voltage across the cell capacitors of the three phases for the same operating condition and different cell capacitances

IV. CONCLUSIONS

This paper presented the operating principle of the HMC with dc side cascaded H-bridge cell, including the basis of modulation and capacitor voltage balancing, and control when operated as a HVDC station. It has been demonstrated that the HMC with dc side H-bridge chain links offers all the features needed in modern voltage source converter based HVDC and flexible ac transmission systems, including dc fault reverse blocking capability. Based on the results and discussion presented in this paper, the attributes and limitations of the hybrid converter with dc side cascaded H-bridge cells can be summarised as follow:

- Offers decoupled control of active and reactive powers, independent of the energy balance of the cell capacitors, hence is suitable for variable voltage applications and connection of offshore oil platforms and wind farms (unlike the version of the hybrid converter presented in [6]).
- Requires half the number of cell capacitors as the modular multilevel converter, but twice as many as the HMC with ac side cascaded H-bridge cells investigated in [2].
- Produces more voltage levels per phase than a modular converter for the same number of cells per arm, hence produces better quality output voltage. This is likely to be achieved at slightly higher on-state losses compared to the modular converter.
- High-voltage main bridge operates at the fundamental frequency, with no synchronization issues with the H-bridge cascaded cells as in [19].
- Resilient to ac and dc network faults. However, its survivability from worse case dc network faults in long HVDC link is challenging due to the large inrush current that may flow in the converter switches during system restoration.

V. REFERENCES

[1] G. P. Adam, S. J. Finney, B. W. Williams, D. R. Trainer, C. D. M. Oates, and a. D. R. Critchley, "Network Fault Tolerant Voltage-Source-Converters for High-Voltage Applications," in *IET, the 9th International conference on AC and DC Power Transmission*, London, UK, 2010.

[2] G. P. Adam, K. H. Ahmed, S. J. Finney, K. Bell, and B. W. Williams, "New Breed of Network Fault-Tolerant Voltage-Source-Converter HVDC Transmission System," *Power Systems, IEEE Transactions on,* vol. PP, pp. 1-1, 2012.

[3] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer†, D. R. Critchley†, and R. W. Crookes†, "A New Hybrid Multi-Level Voltage-Source Converter with DC Fault Blocking Capability," in *IET ACDC2010*, London,UK, 2010.

[4] L. Hui, W. Kaiyu, Z. Da, and R. Wei, "Improved Performance and Control of Hybrid Cascaded H-bridge Inverter for Utility Interactive Renewable Energy Applications," in *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, 2007, pp. 2465-2471.

[5] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, P. Ibaez, and J. L. Villate, "A Comprehensive Study of a Hybrid Modulation Technique for the Neutral-Point-Clamped Converter," *Industrial Electronics, IEEE Transactions on,* vol. 56, pp. 294-304, 2009.

[6] R. Feldman, M. Tomasini, J. C. Clare, P. Wheeler, D. R. Trainer, and R. S. Whitehouse, "A hybrid voltage source converter arrangement for HVDC power transmission and reactive power compensation," in *Power Electronics, Machines and Drives (PEMD 2010), 5th IET International Conference on*, 2010, pp. 1-6.

[7] G. O. Kalcon, G. P. Adam, O. Anaya-Lara, S. Lo, and K. Uhlen, "Small-Signal Stability Analysis of Multi-Terminal VSC-Based DC Transmission Systems," *Power Systems, IEEE Transactions on,* vol. 27, pp. 1818-1830, 2012.

[8] A. A. Rockhill, M. Liserre, R. Teodorescu, and P. Rodriguez, "Grid-Filter Design for a Multimegawatt Medium-Voltage Voltage-Source Inverter," *Industrial Electronics, IEEE Transactions on,* vol. 58, pp. 1205-1217, 2011.

[9] H. Sepahvand, L. Jingsheng, and M. Ferdowsi, "Investigation on Capacitor Voltage Regulation in Cascaded H-Bridge Multilevel Converters With Fundamental Frequency Switching," *Industrial Electronics, IEEE Transactions on,* vol. 58, pp. 5102-5111, 2011.

[10] M. A. Perez, J. Rodriguez, E. J. Fuentes, and F. Kammerer, "Predictive Control of AC–AC Modular Multilevel Converters," *Industrial Electronics, IEEE Transactions on,* vol. 59, pp. 2832-2839, 2012.

[11] Z. Qing-Chang and G. Weiss, "Synchronverters: Inverters That Mimic Synchronous Generators," *Industrial Electronics, IEEE Transactions on,* vol. 58, pp. 1259-1267, 2011.

[12] F. Carnielutti, H. Pinheiro, and C. Rech, "Generalized Carrier-Based Modulation Strategy for Cascaded Multilevel Converters Operating Under Fault Conditions," *Industrial Electronics, IEEE Transactions on,* vol. 59, pp. 679-689, 2012.

[13] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-Voltage Multilevel Converters—State of the Art, Challenges, and Requirements in Industrial Applications," *Industrial Electronics, IEEE Transactions on,* vol. 57, pp. 2581-2596, 2010.

[14] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-Based HVDC Power Transmission Systems: An Overview," *Power Electronics, IEEE Transactions on,* vol. 24, pp. 592-602, 2009.

[15] J. Pereda and J. Dixon, "Cascaded multilevel converters: Optimal asymmetries and floating capacitor control," *Industrial Electronics, IEEE Transactions on,* vol. PP, pp. 1-1, 2012.

[16] W. Song and A. Q. Huang, "Fault-Tolerant Design and Control Strategy for Cascaded H-Bridge Multilevel Converter-Based STATCOM," *Industrial Electronics, IEEE Transactions on,* vol. 57, pp. 2700-2708, 2010.

[17] L. Yun-Feng, Z. Zheng-Ming, Q. Chang, and Z. Xigen, "A novel three-phase multilevel voltage source converter," in *Power Electronics and Motion Control Conference, 2000. Proceedings. IPEMC 2000. The Third International*, 2000, pp. 1172-1175 vol.3.

[18] L. Zixin, W. Ping, Z. Haibin, C. Zunfang, and L. Yaohua, "An Improved Pulse Width Modulation Method for Chopper-Cell-Based Modular Multilevel Converters," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 3472-3481, 2012.

[19] G. P. Adam;, S. J. Fionney;, and a. B. Williams, "Network Fault Tolerent Voltage Source Converters for High-Voltage applications," presented at the IET 9th International Conference on AC and DC Power Transmission systems, London, UK, 2010.

[20] S. Fukuda, T. Yoshida, and S. Ueda, "Control Strategies of a Hybrid Multilevel Converter for Expanding Adjustable Output Voltage Range," *Industry Applications, IEEE Transactions on,* vol. 45, pp. 827-835, 2009.

[21] D. R. Trainer, C. C. Davidson, C. D. Oates, N. M. Macleod, D. R. Critchley, and R. W. Crookes, "A New Hybrid Voltage-Sourced Converter for HVDC Power Transmission," presented at the Cigre2010, 2010.

VII. BIOGRAPHY
VI.

G.P. Adam is working as a research fellow with Institute of Energy and Environment, University of Strathclyde in Glasgow, UK. Dr Adam has a PhD in Power Electronics from University of Strathclyde in 2007. His research interests are fault tolerant voltage source multilevel converters for HVDC systems; control of HVDC transmission systems and multi-terminal HVDC networks; voltage source converter based FACTS devices; and grid integration issues of renewable energies. Dr Adam has authored and co-authored several technical reports, and journal and conference papers in the area of multilevel converters and HVDC systems, and grid integration of renewable power. Also, he has contributed in reviewing process for several IEEE and IET Transactions and Journals, and conferences.

B.W. Williams received the M.Eng.Sc. degree from the University of Adelaide, Australia, in 1978, and the Ph.D. degree from Cambridge University, Cambridge, U.K., in 1980. After seven years as a Lecturer at Imperial College, University of London, U.K., he was appointed to a Chair of Electrical Engineering at Heriot-Watt University, Edinburgh, U.K, in 1986. He is currently a Professor at Strathclyde University, UK. His teaching covers power electronics (in which he has a free internet text) and drive systems. His research activities include power semiconductor modelling and protection, converter topologies, soft switching techniques, and application of ASICs and microprocessors to industrial electronics.