

Three-Phase AC Side Voltage-Doubling High Power Density Voltage Source Converter with Intrinsic Buck-Boost Cell and Common Mode Voltage Suppression

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Abstract—The three-phase two-level voltage source converter (VSC) is widely employed in power conversions between AC and DC for its four-quadrant operation and control flexibility. However, it suffers from the low output voltage range with a peak value of half DC-link per phase, which necessitates the use of either high DC-link voltage or bulky step-up transformer to enable the medium voltage operation. Additionally, the high common mode (CM) voltage between AC loads neutral points and ground may reduce the service life and reliability of electric machinery. In this paper, a three-phase AC side voltage-doubling VSC topology with intrinsic Buck-Boost cell is analyzed. By this configuration, the AC side voltage is doubled with the phase peak value equal to DC-link. That is, only half of the DC side capacitor bank is needed to generate the same output voltage. The proposed converter uses its buck-boost cell as a virtual voltage source to synthesize negative half of the output voltage by modulating its output AC phase voltage around the negative bus (which is the real zero when grounded). This permits the average CM voltage to be suppressed to zero, and loads connected to converter AC side not to withstand any DC voltage stress (reducing the insulation requirement). Modeling and control design for both rectifier and inverter modes of this converter in synchronous reference frame have been investigated to ensure a four-quadrant three-phase back-to-back system. Experimental results have verified the feasibility and the effectiveness of the proposed configuration and the designed control strategies.

Index Terms— AC side voltage-doubling, Common mode voltage suppression, Intrinsic Buck-Boost Cell, Three-phase Back-to-Back system, Four-quadrant operation.

I. INTRODUCTION

Power electronics based energy conversion systems have achieved deep penetration in low, medium and high voltage applications such as power transmission and reactive power compensation, grid interfacing of renewable energy, machine drives, etc. Since traditional AC grids still dominate in power systems, AC power conversion involving

amplitude regulation, phase and frequency control, active power and reactive power management for utility/micro-grid applications has always drawn many attentions of both academia and industry.

The back-to-back (B2B) VSC configuration is widely used among various AC conversion solutions for its superiority on control simplicity, voltage utilization over the Matrix Converter and dynamic performance over other current source converter based solutions [1, 2]. This is because it offers four-quadrant operation ability, decoupling of the two connected AC sides and independent control of active/reactive power. Nowadays, VSC together with its B2B configuration have overstepped the traditional power traction area and spread into the utility applications, such as PV (photovoltaic) grid connection, wind energy interfacing, flexible AC and high voltage DC transmission systems (FACTS and HVDC) [3-9].

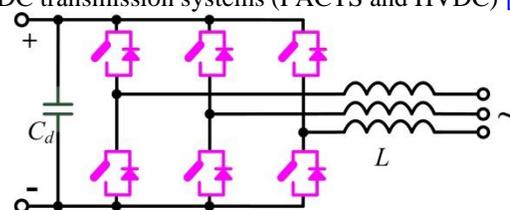


Fig. 1 Three-phase two-level voltage source converter.

The three-phase two-level converter depicted in Fig. 1 is widely accepted for AC-DC and DC-AC power conversion systems in research and industry. However, in this topology, the peak value of AC side voltage per phase cannot exceed half of DC link voltage with traditional Sinusoidal Pulse Width Modulation (SPWM). Although the Triplen Sinusoidal Pulse Width Modulation (TSPWM), Space Vector Modulation (SVM) and Selective Harmonic Elimination (SHE) methods have been developed to extend the fundamental voltage output range in AC side, the increase is not obvious (15.5% for TSPWM/SVM, and slightly larger for optimized SHE) [10]. In addition, three-phase balanced conditions should be guaranteed to insure this extension in voltage utilization, otherwise, low order harmonics will be observed in the line-to-line voltages and line currents. This is because zero sequence components will emerge in phase voltage when it goes beyond the envelopes of the positive and negative DC-link, which can only be neutralized under three-phase balanced situation. Therefore, operation in medium and high voltage applications requires high DC-link voltage (minimum of twice peak fundamental voltage) or the bulky step-up

Manuscript received on August 1, 2014; revised on September 23, 2014; accepted on October 24, 2014. This work was supported by EPSRC 'Underpinning Power Electronics 2012: Converters Theme' research programme (EP/K035096/1).

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transformer for voltage matching, which in turn increases the system cost, size and weight.

The CM voltage between AC and DC sides is inherent for all bridge type solutions. The three-phase two-level VSC in Fig. 1 may impose DC voltage stress on the AC side loads depending on the adopted grounding arrangement [11, 12]. When the negative terminal is grounded, the output phase voltage relative to real ground varies around half DC-link, and this requires the AC loads to be able to withstand DC voltage stress [13]. Furthermore, the voltage fluctuation around half DC-link on the load neutral point may exacerbate the bearing voltage problem in machine drives such as wind turbine interfacing. The split DC-link capacitor with parallel balancing resistors can be employed to address the problem of DC voltage stress and reduce the impact of the CM voltage. However, this solution is less attractive as it introduces additional loss and cost.

A certain case under the spotlight recently is the transformerless PV integration area where many efforts have been made to diminish this CM component across the parasitic capacitor between the PV arrays and ground. The H5, H6 and HERIC schemes are candidates to suppress the CM leakage current [14]. However, the CM voltage component still exists and keeps constant in these situations. The virtual DC bus concept [15] and HA4S converter [16] have been advanced to eliminate the CM voltage by direct connection between ground terminals. Unfortunately, the solutions above are in single-phase application and originate from the H-bridge topology. Thus, it is difficult to transplant these derived converters directly into three-phase condition.

In this paper, a three-phase AC side voltage-doubling (ACVD) converter with intrinsic Buck-Boost cells (IBBCs) has been proposed, which can generate the AC phase voltage with a maximum peak value equal to full DC-link voltage, doubling the output range of the traditional three-phase two-level VSC. On the other hand, the DC-link can be halved when the same output voltage is demanded. Consequently, either the line transformers or the DC capacitor bank can be reduced to form a compact and cost-efficient system. In addition, the dv/dt problem can be largely relieved by the reduced DC-link voltage. Since the proposed topology inherits a real ground fixed at negative bus, its output phase voltage is modulated around this ground. As a result, DC voltage stress exerted on the AC loads can be suppressed to zero, and this will suppress the magnitude of CM voltage to an average of zero, as seen by the load neutral points. Hence, reduced bearing voltage/current can be expected. Further employment of either composited hardware configuration or optimized modulation strategy can eliminate the high frequency components of the CM voltage, which is beyond the scope of this paper [17-19]. The ACVD converter is capable of being employed in PV integration, wind energy interfacing and distributed FACTS areas potentially. The rest of the paper is organized as follows. Operational principle of the proposed converter is described in Section II. Section III analyses the voltage and current stresses on the power switches and presents some design issues for passive components. In Section IV, modeling process of the three-phase ACVD-VSC for inverter and rectifier modes in synchronous reference frame (SRF) is established. Then, Section V presents the

design of the control strategies minutely. Afterwards, experimental verifications are presented in Section VI to confirm the validity of the proposed converter. Finally, conclusions drawn and highlight of major findings are summarised in Section VII.

II. OPERATIONAL PRINCIPLE OF THE ACVD CONVERTER

The proposed three-phase ACVD-VSC is shown in Fig. 2(a), where the IBBC is inserted into each phase of two-level converter to achieve an extended output voltage range. The single-phase circuit under inverter mode depicted in Fig. 2(b) clarifies the structure of the topology in detail. It can be seen that the IBBC consists of L_1 and C_1 , while L_2 and C_2 make up the output stage filter. The two power switches S_1 and S_2 conduct complementarily. Furthermore, V_{dc} is the input voltage, and i_1 , v_1 , i_2 and v_2 represent the four state variables on the passive components L_1 , C_1 , L_2 and C_2 respectively. Notice that v_1 should be reversed relative to the input voltage to ensure the magnetic reset of the flux linked in L_1 . Similarly, i_1 and i_2 are also in opposite directions to keep the voltage balance on C_1 .

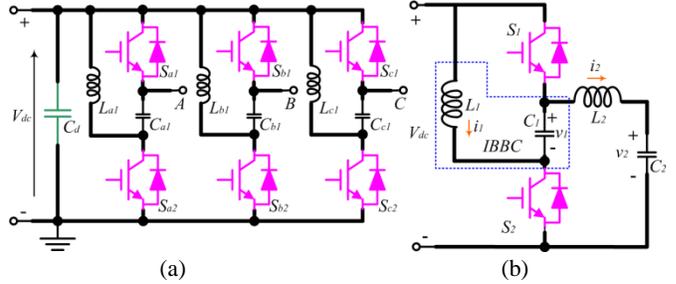


Fig. 2 Proposed ACVD Converter: (a) configuration in three-phase (without filter); (b) single-phase unit operated in inverter mode.

Operation of the proposed converter can be described using two modes as follow:

Mode 1: S_1 is turned on. Output voltage v_2 fed from V_{dc} is generated relative to ground. Also, this mode creates a zero loop of inductor L_1 and capacitor C_1 for charging the buck-boost capacitor with reversed polarity as V_{dc} .

Mode 2: When S_2 is on, the IBBC capacitor is employed as a virtual voltage source to generate the negative voltage on the output. The inner inductor L_1 is also charged to store energy to get ready for the energy transfer in the subsequent switching cycle.

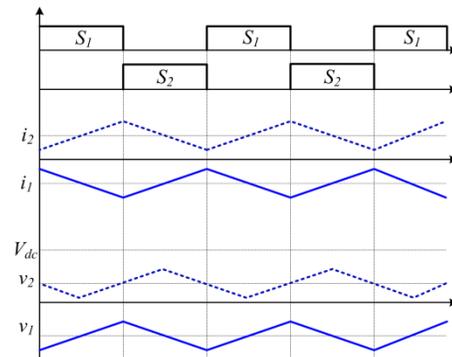


Fig. 3 Steady state waveforms of the proposed converter in a stationary operation point when v_2 , i_2 are positive and i_1 is negative

Fig. 3 demonstrates the steady state waveforms of the proposed converter in a fixed operation point with the

assumption that v_2 , i_2 are positive and i_1 is negative. The output voltage v_2 always falls inside the envelope combined by input voltage and IBBC voltage, which guarantees the energy balance in the inductance. Similarly, the inductor currents i_1 and i_2 will charge and discharge the capacitors in each switching cycle to obtain the composed voltage outputs.

In further, the four-quadrant operation of the ACVD-VSC is interpreted by Fig. 4. In Fig. 4(a) and Fig. 4(b), i_2 flows out of the converter to the load, accordingly i_1 should either discharge C_1 or feed its stored energy back to the DC-link. The alternative situation where i_2 flows into the converter from the load and i_1 draws energy from the DC side to deliver it to C_1 can be seen in Fig. 4(c) and Fig. 4(d). Thus, it is concluded that the proposed converter is a qualified candidate for the four-quadrant operational VSC applications.

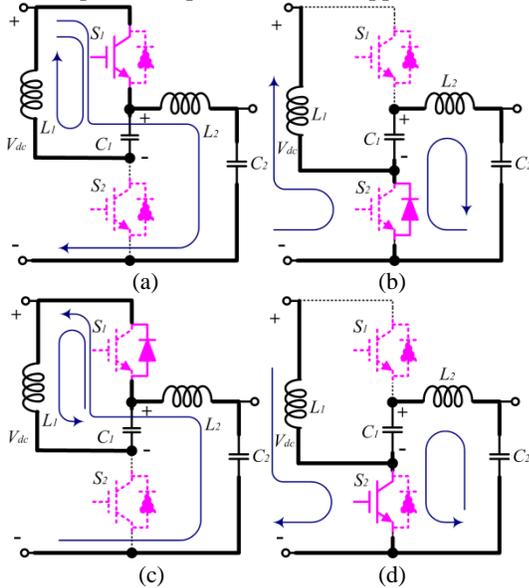


Fig. 4 Switching modes for the proposed converter to implement four-quadrant operation: (a) S_1 turns on with outflow load current; (b) S_2 turns on with outflow load current, (c) S_1 turns on with inflow load current, (d) S_2 turns on with inflow load current.

Based on the above analysis, the differential equations that describe the dynamics of the proposed converter are interpreted in (1),

$$(1) \quad \begin{cases} L_1 \frac{di_1}{dt} = u(v_1 - V_{dc}) + V_{dc} \\ C_1 \frac{dv_1}{dt} = u(i_2 - i_1) - i_2 \\ L_2 \frac{di_2}{dt} = u(V_{dc} - v_1) + (v_1 - v_2) \\ C_2 \frac{dv_2}{dt} = i_2 - i_o \end{cases}$$

where u is the switching function defined as follows,

$$(2) \quad u = \begin{cases} 1, & S_1 \text{ turns on} \\ 0, & S_2 \text{ turns on} \end{cases}$$

Considering the case where switching frequency is sufficiently high compared to fundamental frequency of the AC voltage being synthesized, the assumption that all the state variables can be viewed as constant is valid. Therefore, the derivative terms in (1) can be set to zero, and the average

value of the switching function u over one switching period is equal to the duty cycle D , then equation (1) is reduced to:

$$(3) \quad \begin{cases} D(V_1 - V_{dc}) + V_{dc} = 0 \\ D(I_2 - I_1) - I_2 = 0 \\ D(V_{dc} - V_1) + (V_1 - V_2) = 0 \\ I_2 - I_o = 0 \end{cases}$$

After algebraic manipulation of first and third equations in (3), voltage transfer ratio of proposed converter is obtained as:

$$(4) \quad M = \frac{V_2}{V_{dc}} = 2 - \frac{1}{D}$$

Fig. 5(a) shows the plot of M versus D and it is observed that a bipolar voltage output can be achieved when the duty cycle varies around 0.5.

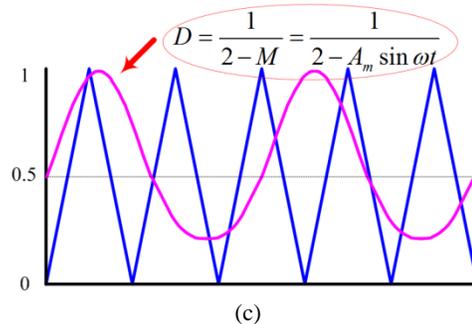
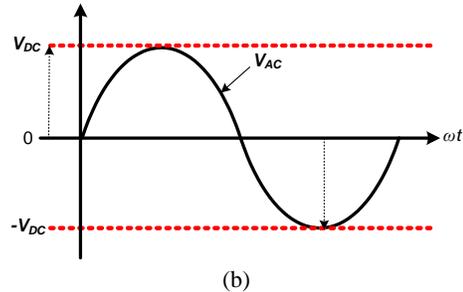
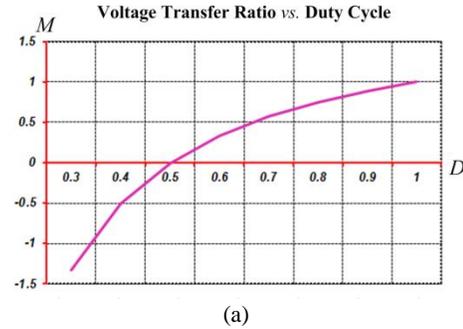


Fig. 5 Voltage output range and modulation for the proposed converter: (a). voltage transfer ratio vs. duty cycle; (b). AC side output voltage range; (c). open loop modulation strategy based on transfer ratio.

From Fig. 5(b), the maximum modulation index is 1pu for the peak value of phase voltage (V_{dc}), which is twice of that in two-level converter ($1/2V_{dc}$). In addition, triplen harmonic injection idea can further extend this range to 1.55pu. Equivalently, the output line-to-line peak voltage can reach 2pu ($2V_{dc}$) in that case. Due to this large extension in DC utilization, reduced DC-link voltage and dv/dt can be achieved.

Notice that inner capacitance can be significantly less than DC link because of the fluctuant voltage across it. Besides, the asymmetry between the two voltage levels synthesized during

modes 1 and 2 may potentially distort the output voltage by even order harmonics when the modulation strategy in Fig. 5(c) is adopted, where A_m is the modulation index. Therefore, proper converter operation with sinusoidal output voltage and current requires countermeasures to be incorporated in the modulation strategy to neutralize the negative impact of the distortion, which will be investigated in later sections.

From the above analysis based on single-phase situation, it can be found that the DC-link and AC side share the common ground. Consequently, in the three-phase three-wire system, the average value of the CM voltage between DC-link ground and AC neutral point must be zero for any balanced condition.

III. PERFORMANCE EVALUATION OF VOLTAGE/CURRENT STRESS AND INTEGRATED MAGNETIC SOLUTION

In this section, a brief analysis of the voltage/current stress of power switches and some design issues for the passive components are demonstrated. The additional IBBC may exert some extra voltage/current stress on the devices. So it is important to unveil the quantitative relationship between the electrical stresses of the semiconductor switches and the output power, based on which the guidelines of the device selection is provided. Besides, the integrated magnetic technique can be employed to integrate the two inductors into one magnetic core, compacting the installations and reducing the core costs.

A. Voltage Stress Analysis

According to (3), the voltage on C_1 and C_2 are given by (5) and (6) respectively. The opposite polarity of V_{dc} and V_1 offers the possibility to generate the bipolar voltage on C_2 .

$$V_1 = (1 - 1/D)V_{dc} \quad (5)$$

$$V_2 = (2 - 1/D)V_{dc} \quad (6)$$

Consequently, the reverse blocked voltage of the power switches S_1 and S_2 can be calculated by (7).

$$V_{RB} = V_{dc} - V_1 = V_{dc} / D \quad (7)$$

In further, since the maximum output-input voltage ratio is A_m , the voltage stress is then shown by (8).

$$V_{RB} = (2 - M)V_{dc} = (2 - A_m \sin \omega t)V_{dc} \quad (8)$$

It is noticed that the duty cycle D varies from 0.33-1.0 in the maximum output condition when A_m reaches the peak value 1. The maximum voltage stress on the power switches of the proposed converter is two times of DC voltage plus peak of the output phase voltage. Compared with the two-level topology, voltage stress will increase by 50% in extreme conditions. However, this increase in voltage stress is logical, because the presented ACVD converter holds the same DC utilization as full-bridge converter but with half number of switches. In other words, it has same number of switches as two-level topology but with twice DC link voltage utilization. This attribute is achieved by the incorporation of IBBC. The fluctuant voltage across C_1 makes small value AC capacitor available but causes the increase in power switches [20].

B. Current Stress Analysis

After manipulation of equation (3) for the current state variables, equations (9) and (10) are obtained, and observe that

currents i_1 and i_2 are in opposite direction, which is necessary for the energy balance of the C_1 .

$$I_1 = (1 - 1/D)I_2 \quad (9)$$

$$I_2 = V_2 / R = I_o \quad (10)$$

The current of the IBBC inductor i_1 should pass through either S_1 or S_2 to store and release energy alternatively. From Fig. 4, the total current for the power switches should be the sum of absolute value of the two current state variables. Since I_1 and I_2 are always in opposite directions, the total current stress of each power switch can be expressed as in (11).

$$I_c = |I_1| + |I_2| = |I_1 - I_2| \quad (11)$$

In general, the power switch current can be in further clarified as (12), where φ is the power factor angle, ω is the angular frequency of the output voltage and I_{om} represents the maximum value of the load current.

$$I_c = |I_1 - I_2| = (I_{om} / D) \cdot \sin(\omega t + \varphi) \quad (12)$$

Considering (4), the equation (12) then can be developed as follows:

$$I_c = (2 - A_m \sin \omega t)I_{om} \sin(\omega t + \varphi) \quad (13)$$

It can be deduced that some second order harmonic current will be introduced by the IBBC. The peak value of the power switch current happens when equation (13) reaches the maximum. An approximate margin of three times of the load current should be considered in practical design. Notice that the output current of this converter is to be approximately half of that in two-level topology with the same DC-link and same power rating since output voltage can be doubled due to the introduced IBBC, which makes the current stress not to be a problem for the proposed converter.

C. Passive Device Selection



Fig. 6. Equivalent model of the power path for inner capacitor C_1 of ACVD converter: (a) S_2 is on, S_1 is off; (b) S_1 is on, S_2 is off.

Since L_2 and C_2 form the output filter of the proposed ACVD converter, L_2 and C_2 can be selected using well established filter design method of the conventional two-level VSC as illustrated in [21]. Whilst L_1 and C_1 are selected based on the switching model from AC point of view since all the state variables are AC. The equivalent power paths for inner capacitor C_1 is shown in Fig. 6. When S_2 is on and S_1 is off, inner capacitor C_1 is in series with output filter inductor L_2 as in Fig. 6(a). In order to make the AC component of the voltage across C_1 follow up the output voltage and avoid the large high frequency oscillation on C_1 , the resonant frequency of C_1 and L_2 is placed in the interval of fundamental and switching frequencies (f_0 and f_{sw}). With L_2 , C_2 and f_{sw} are all known; the geometrical mean in (14) is used to calculate C_1 as:

$$f_r = 1 / (2\pi \cdot \sqrt{C_1 L_2}) = \sqrt{f_0 f_{sw}} \quad (14)$$

In the proposed ACVD converter, the inner inductor L_1 is employed as a buffer for energy transfer from DC-link to C_1 in the periods where the upper switch of each phase leg is on. Additionally, It has similar function as MMC arm inductance,

which can limit the inrush current from the capacitor C_1 when the upper switch of each phase leg is on [22]. In Fig. 6(b), L_1 and C_1 are in series. Large L_1 value will cause large fundamental voltage drop and limit the magnitude of high frequency current ripple. In this sense, the characteristic impedance of L_1 and C_1 in (15) should be used as a compromise between the output power range and ripple current demand.

$$z_0 = \sqrt{L_1 / C_1} \quad (15)$$

D. Potential Use of Magnetic Integration

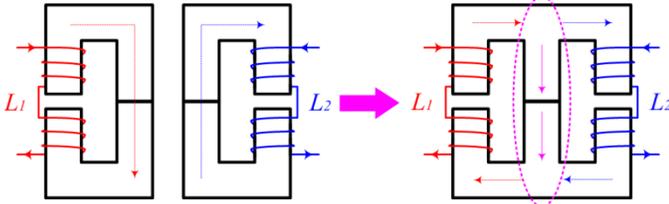


Fig. 7 Principles of the integrated magnetic solution.

The IBBC introduces an extra inductor into the proposed converter per phase. In order to improve the power density, the magnetic integration technique is competent to integrate the IBBC inductor and output filtering inductor into one magnetic core [23-25]. Fig. 7 interprets the solution for the magnetic integration technique, where a three-leg EE type magnetic core is employed. Some air gaps are inserted into the two outer legs while no air gap exists in the center leg. The IBBC inductor L_1 is wound around one outer leg and the filtering inductor L_2 is reversely wound around another outer leg. In this way, the magneto-motive force will be distributed mostly on the outer legs and the two inductors can be decoupled effectively. Fig. 7 shows that the flux linkage of the two inductors will be in opposite directions, so the average component of the total flux in the center leg is diminished and the cross section area of the center leg is reduced. Therefore, the power density and the efficiency can be enhanced with the proposed magnetic integration method.

This approach is restricted to low and medium power stages at present due to the limited window area of the commercial high magneto-conductivity core.

IV. MODELING OF THREE-PHASE ACVD CONVERTER IN SYNCHRONOUS REFERENCE FRAME

The Park transformation based decoupling model for the three-phase two-level VSC is widely employed to implement independent control of active and reactive power. Since the reference becomes DC value in SRF, zero steady state errors are expected with proportional-integral (PI) controller. In this section, the modeling of the proposed ACVD-VSC in SRF is performed to establish an insight view of the control design. In order to establish a general law for the operational analysis and control design, resistive load conditions have been assumed here and in the upcoming control design section. For proper design, the load current can be treated as a new state variable. Thus, the order of the state space equations and transfer functions that describe the proposed converter will increase. Besides, extra measurements are necessary. However, the overall procedure stays the same.

The proposed converter is capable of forming a three-phase four-wire system, where the DC ground and AC ground is connected directly. Thus, each phase can be controlled independently. This configuration can be employed in UPS and aero-space applications. However, the analysis below is only based on three-phase three-wire system.

A. The Inverter Mode

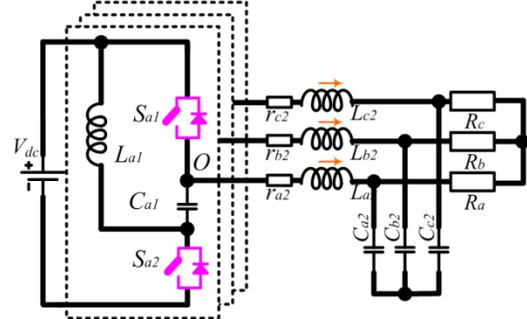


Fig. 8 Rearrangement for the proposed three-phase inverter.

The rearrangement of the three-phase ACVD-VSC as an inverter is depicted in Fig. 8. From the instantaneous value based state space equations in (1) and assumptions in (16), the three-phase AC side equations can be expressed as in (17).

$$\begin{cases} L_2 = L_{a2} = L_{b2} = L_{c2} \\ C_2 = C_{a2} = C_{b2} = C_{c2} \\ R = R_a = R_b = R_c \\ r_2 = r_{a2} = r_{b2} = r_{c2} \end{cases} \quad (16)$$

$$\begin{cases} L_2 \frac{d}{dt} \begin{bmatrix} i_{a2} - i_{b2} \\ i_{b2} - i_{c2} \\ i_{c2} - i_{a2} \end{bmatrix} = \begin{bmatrix} v_a - v_b \\ v_b - v_c \\ v_c - v_a \end{bmatrix} - r_2 \begin{bmatrix} i_{a2} - i_{b2} \\ i_{b2} - i_{c2} \\ i_{c2} - i_{a2} \end{bmatrix} - \begin{bmatrix} v_{a2} - v_{b2} \\ v_{b2} - v_{c2} \\ v_{c2} - v_{a2} \end{bmatrix} \\ RC_2 \frac{d}{dt} \begin{bmatrix} v_{a2} - v_{b2} \\ v_{b2} - v_{c2} \\ v_{c2} - v_{a2} \end{bmatrix} = R \begin{bmatrix} i_{a2} - i_{b2} \\ i_{b2} - i_{c2} \\ i_{c2} - i_{a2} \end{bmatrix} - \begin{bmatrix} v_{a2} - v_{b2} \\ v_{b2} - v_{c2} \\ v_{c2} - v_{a2} \end{bmatrix} \\ L_2 \frac{d}{dt} \begin{bmatrix} i_{ab2} \\ i_{bc2} \\ i_{ca2} \end{bmatrix} = \begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} - r_2 \begin{bmatrix} i_{ab2} \\ i_{bc2} \\ i_{ca2} \end{bmatrix} - \begin{bmatrix} v_{ab2} \\ v_{bc2} \\ v_{ca2} \end{bmatrix} \\ RC_2 \frac{d}{dt} \begin{bmatrix} v_{ab2} \\ v_{bc2} \\ v_{ca2} \end{bmatrix} = R \begin{bmatrix} i_{ab2} \\ i_{bc2} \\ i_{ca2} \end{bmatrix} - \begin{bmatrix} v_{ab2} \\ v_{bc2} \\ v_{ca2} \end{bmatrix} \end{cases} \quad (17)$$

where $\{v_a, v_b, v_c\}$ represents the converter output phase voltage (measuring from poles $O = \{O_1, O_2, O_3\}$ relative to the ground), and V_{dc} is the DC side input voltage. Additionally, R and r_2 are the load and filter reactor (L_2) resistances respectively.

With the definition of u in (2), the extended three-phase switching function can be denoted as in (18). The converter output voltage is then defined in (19). It is noticed that the proposed converter exhibits some time-variant behaviour that makes the large signal modeling with complete decoupling infeasible. Thus, some approximations have been made to facilitate the development of the fundamental average model which is necessary for control design and simplicity of the analysis.

$$u_i = \begin{cases} 1, & S_{i1} \text{ turns on} \\ 0, & S_{i2} \text{ turns on} \end{cases} \quad (i = a, b, c) \quad (18)$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} V_{dc} + \begin{bmatrix} 1-u_a & 0 & 0 \\ 0 & 1-u_b & 0 \\ 0 & 0 & 1-u_c \end{bmatrix} \begin{bmatrix} v_{a1} \\ v_{b1} \\ v_{c1} \end{bmatrix} \quad (19)$$

To synthesize sinusoidal output voltage based (5), the IBBC voltage is expected to contain both DC and AC components. According to the previous analysis shown by (13), second order harmonic current will emerge in the IBBC inductor. Consequently, AC voltage of IBBC capacitor contains both the fundamental and the second order harmonic. When neglecting the second order harmonic for simplicity, (20) is obtained. After application of the classical average method to switching function, equation (19) is rearranged into (21), which can be simplified as (22),

$$\begin{bmatrix} v_{a1} \\ v_{b1} \\ v_{c1} \end{bmatrix} \approx - \begin{bmatrix} V_{dc} \\ V_{dc} \\ V_{dc} \end{bmatrix} + \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (20)$$

$$\begin{bmatrix} \overline{v_a} \\ \overline{v_b} \\ \overline{v_c} \end{bmatrix} = \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} V_{dc} + \begin{bmatrix} d_a-1 & 0 & 0 \\ 0 & d_b-1 & 0 \\ 0 & 0 & d_c-1 \end{bmatrix} \begin{bmatrix} V_{dc} - \overline{v_a} \\ V_{dc} - \overline{v_b} \\ V_{dc} - \overline{v_c} \end{bmatrix} \quad (21)$$

$$\begin{bmatrix} \overline{v_a} \\ \overline{v_b} \\ \overline{v_c} \end{bmatrix} = \begin{bmatrix} 2-1/d_a \\ 2-1/d_b \\ 2-1/d_c \end{bmatrix} V_{dc} \triangleq \begin{bmatrix} m_a \\ m_b \\ m_c \end{bmatrix} V_{dc} \quad (22)$$

where $\{d_a, d_b, d_c\}$ is the duty ratio for each phase, $\{m_a, m_b, m_c\}$ is the equivalent transfer ratio and “ $\overline{\quad}$ ” is the averaging operator over one switching cycle.

Furthermore, by defining $\{m_{ab}, m_{bc}, m_{ca}\} = \{m_a - m_b, m_b - m_c, m_c - m_a\}$, the switching averaged AC side equations can be derived as in (23). The Park transformation with the form in (24) is then applied to obtain the equivalent time-invariant system. The decoupling model of the proposed ACVD inverter in SRF can be finally achieved and demonstrated in (25).

$$\begin{cases} L_2 \frac{d}{dt} \begin{bmatrix} \overline{i_{ab2}} \\ \overline{i_{bc2}} \\ \overline{i_{ca2}} \end{bmatrix} = \begin{bmatrix} m_{ab} \\ m_{bc} \\ m_{ca} \end{bmatrix} V_{dc} - r_2 \begin{bmatrix} \overline{i_{ab2}} \\ \overline{i_{bc2}} \\ \overline{i_{ca2}} \end{bmatrix} - \begin{bmatrix} \overline{v_{ab2}} \\ \overline{v_{bc2}} \\ \overline{v_{ca2}} \end{bmatrix} \\ C_2 \frac{d}{dt} \begin{bmatrix} \overline{v_{ab2}} \\ \overline{v_{bc2}} \\ \overline{v_{ca2}} \end{bmatrix} = \begin{bmatrix} \overline{i_{ab2}} \\ \overline{i_{bc2}} \\ \overline{i_{ca2}} \end{bmatrix} - \frac{1}{R} \begin{bmatrix} \overline{v_{ab2}} \\ \overline{v_{bc2}} \\ \overline{v_{ca2}} \end{bmatrix} \end{cases} \quad (23)$$

$$T = \frac{2}{3} \begin{bmatrix} \cos \omega t & \cos(\omega t - 2\pi/3) & \cos(\omega t + 2\pi/3) \\ -\sin \omega t & -\sin(\omega t - 2\pi/3) & -\sin(\omega t + 2\pi/3) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \quad (24)$$

$$\begin{cases} \frac{d}{dt} \begin{bmatrix} \overline{i_{2d}} \\ \overline{i_{2q}} \end{bmatrix} = -\frac{1}{L_2} \begin{bmatrix} \overline{v_{2d}} \\ \overline{v_{2q}} \end{bmatrix} - \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \cdot \begin{bmatrix} \overline{i_{2d}} \\ \overline{i_{2q}} \end{bmatrix} - \frac{r_2}{L_2} \begin{bmatrix} \overline{i_{2d}} \\ \overline{i_{2q}} \end{bmatrix} + \frac{V_{dc}}{L_2} \begin{bmatrix} m_d \\ m_q \end{bmatrix} \\ \frac{d}{dt} \begin{bmatrix} \overline{v_{2d}} \\ \overline{v_{2q}} \end{bmatrix} = \frac{1}{C_2} \begin{bmatrix} \overline{i_{2d}} \\ \overline{i_{2q}} \end{bmatrix} - \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \cdot \begin{bmatrix} \overline{v_{2d}} \\ \overline{v_{2q}} \end{bmatrix} - \frac{1}{RC_2} \begin{bmatrix} \overline{v_{2d}} \\ \overline{v_{2q}} \end{bmatrix} \end{cases} \quad (25)$$

The previous stated second order harmonic distortion problem caused by the IBBC must be treated separately with additional control loops to ensure the pure sinusoidal output voltage and current, which will be covered in later part.

B. The Rectifier Mode

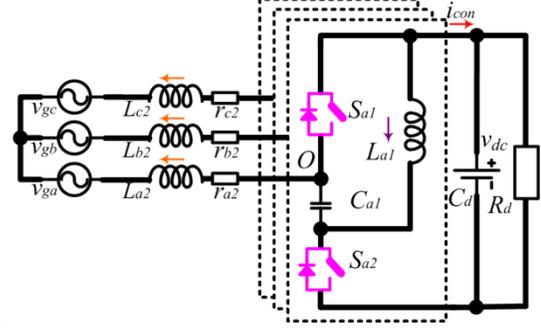


Fig. 9 Rearrangement for the proposed three-phase rectifier.

Fig. 9 shows the proposed ACVD-VSC when it is configured as a rectifier. The AC side and DC side equations are shown in (26), in which $\{v_{gab}, v_{gbc}, v_{gca}\} = \{v_{ga} - v_{gb}, v_{gb} - v_{gc}, v_{gc} - v_{ga}\}$ represents the AC input voltage, v_{dc} is the output voltage, and i_{con} in (27) is the total current feeding from the converter to the DC side.

Based on the previous approximation, the second order current component in IBBC inductor is neglected temporarily. From (9) and by utilizing the switching average operator, equation (27) is to be developed into (28). After substituting (22) and (28) into (26), the standard form of the proposed rectifier model is given as in (29).

$$\begin{cases} L_2 \frac{d}{dt} \begin{bmatrix} \overline{i_{ab2}} \\ \overline{i_{bc2}} \\ \overline{i_{ca2}} \end{bmatrix} = \begin{bmatrix} \overline{v_{ab}} \\ \overline{v_{bc}} \\ \overline{v_{ca}} \end{bmatrix} - r_2 \begin{bmatrix} \overline{i_{ab2}} \\ \overline{i_{bc2}} \\ \overline{i_{ca2}} \end{bmatrix} - \begin{bmatrix} \overline{v_{gab}} \\ \overline{v_{gbc}} \\ \overline{v_{gca}} \end{bmatrix} \\ C_d \frac{dv_{dc}}{dt} = i_{con} - \frac{v_{dc}}{R_d} \end{cases} \quad (26)$$

$$i_{con} = -[u_a \quad u_b \quad u_c] \cdot \begin{bmatrix} \overline{i_{a2}} \\ \overline{i_{b2}} \\ \overline{i_{c2}} \end{bmatrix} - [1-u_a \quad 1-u_b \quad 1-u_c] \cdot \begin{bmatrix} \overline{i_{a1}} \\ \overline{i_{b1}} \\ \overline{i_{c1}} \end{bmatrix} \quad (27)$$

$$\overline{i_{con}} = -[m_a \quad m_b \quad m_c] \cdot \begin{bmatrix} \overline{i_{a2}} \\ \overline{i_{b2}} \\ \overline{i_{c2}} \end{bmatrix} = -[m_{ab} \quad m_{bc} \quad m_{ca}] \cdot \begin{bmatrix} \overline{i_{ab2}} \\ \overline{i_{bc2}} \\ \overline{i_{ca2}} \end{bmatrix} \quad (28)$$

$$\begin{cases} L_2 \frac{d}{dt} \begin{bmatrix} \overline{i_{ab2}} \\ \overline{i_{bc2}} \\ \overline{i_{ca2}} \end{bmatrix} = \begin{bmatrix} m_{ab} \\ m_{bc} \\ m_{ca} \end{bmatrix} \overline{v_{dc}} - r_2 \begin{bmatrix} \overline{i_{ab2}} \\ \overline{i_{bc2}} \\ \overline{i_{ca2}} \end{bmatrix} - \begin{bmatrix} \overline{v_{gab}} \\ \overline{v_{gbc}} \\ \overline{v_{gca}} \end{bmatrix} \\ C_d \frac{d\overline{v_{dc}}}{dt} = -[m_{ab} \quad m_{bc} \quad m_{ca}] \cdot \begin{bmatrix} \overline{i_{ab2}} \\ \overline{i_{bc2}} \\ \overline{i_{ca2}} \end{bmatrix} - \frac{\overline{v_{dc}}}{R_d} \end{cases} \quad (29)$$

Using the Park transformation to achieve (30), which clarifies the model of the proposed ACVD rectifier in SRF.

$$\begin{cases} \frac{d}{dt} \begin{bmatrix} \bar{i}_{2d} \\ \bar{i}_{2q} \end{bmatrix} = -\frac{1}{L_2} \begin{bmatrix} \bar{v}_{gd} \\ \bar{v}_{gq} \end{bmatrix} - \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \cdot \begin{bmatrix} \bar{i}_{2d} \\ \bar{i}_{2q} \end{bmatrix} - \frac{r_2}{L_2} \begin{bmatrix} \bar{i}_{2d} \\ \bar{i}_{2q} \end{bmatrix} + \frac{v_{dc}}{L_2} \begin{bmatrix} m_d \\ m_q \end{bmatrix} \\ \frac{dv_{dc}}{dt} = -\frac{1}{C_d} \begin{bmatrix} m_d & m_q \end{bmatrix} \cdot \begin{bmatrix} \bar{i}_{2d} \\ \bar{i}_{2q} \end{bmatrix} - \frac{v_{dc}}{R_d C_d} \end{cases} \quad (30)$$

Similar with the inverter mode, the o axis is omitted in (30) for three-phase three-wire rectifier mode. And second order harmonic distortion may happen to the line current if no suppression measure is applied. Thus, the eliminating control loop is necessary to calibrate the modulating signal to obtain line current with low total harmonic distortion (THD).

C. The Second Order Distortion

The second order distortion can be explained by using the classical transfer function method. Quasi-static analysis is employed in this part to unveil the system gain scheduling along different operational points.

Taking the single-phase inverter in Fig. 2(b) with resistive load R_o for example, the switching average large signal model is shown in (31). The Taylor Series based linearization method is employed for a fixed operation point to obtained state space equation and transfer function for perturbations near to this selected state. In this way, (31) can be linearized into (32). Using Laplace transformation to obtain the transfer function G_{v2d} , which is shown in (33).

$$\begin{cases} L_1 \frac{d\bar{i}_1}{dt} = d(\bar{v}_1 - V_{dc}) + V_{dc} \\ C_1 \frac{d\bar{v}_1}{dt} = d(\bar{i}_2 - \bar{i}_1) - \bar{i}_2 \\ L_2 \frac{d\bar{i}_2}{dt} = d(V_{dc} - \bar{v}_1) + (\bar{v}_1 - \bar{v}_2) \\ C_2 \frac{d\bar{v}_2}{dt} = \bar{i}_2 - \frac{\bar{v}_2}{R_o} \end{cases} \quad (31)$$

$$\begin{cases} L_1 \frac{d\Delta i_1}{dt} = D_0 \Delta v_1 + (V_1 - V_{dc}) \Delta d \\ C_1 \frac{d\Delta v_1}{dt} = -(1 - D_0) \Delta i_2 - D_0 \Delta i_1 + (I_2 - I_1) \Delta d \\ L_2 \frac{d\Delta i_2}{dt} = (1 - D_0) \Delta v_1 - (V_1 - V_{dc}) \Delta d - \Delta v_2 \\ C_2 \frac{d\Delta v_2}{dt} = \Delta i_2 - \frac{\Delta v_2}{R_o} \end{cases} \quad (32)$$

$$\begin{aligned} G_{v2d} &= \frac{\Delta v_2(s)}{\Delta d(s)} = \frac{V_{dc} + A_1 s + A_2 s^2}{D^2 + B_1 s + B_2 s^2 + B_3 s^3 + B_4 s^4} \\ A_1 &= L_1 (1 - D_0) (I_2 - I_1) \\ A_2 &= L_1 C_1 \frac{V_{dc}}{D_0} \\ B_1 &= \frac{(1 - D_0)^2 L_1 + D_0^2 L_2}{R_o} \\ B_2 &= L_1 C_1 + D_0^2 L_2 C_2 + (1 - D_0)^2 L_1 C_2 \\ B_3 &= \frac{L_1 C_1 L_2}{R_o} \\ B_4 &= L_1 C_1 L_2 C_2 \end{aligned} \quad (33)$$

Assuming the DC input voltage is 1p.u. and modulating index is 1, when the operation point varies sinusoidally, it can be found that the loop gain K_{v2d} is not constant as that in the two-level converter, on the contrary a periodical vibration is observed mainly focused on fundamental and second order components as shown in Fig. 10. Besides, both the zeroes and poles will drift due to the variation of duty cycle. Accordingly, the proposed converter will show some second order distortion and a thimbleful of third order components as by-products when operated in open loop. It is clearly that for the proposed converter with normal PI controller and sinusoidal reference, the output voltage will wane in amplitude and perform some inclination due to the non-uniform distribution of the loop gain and the floating poles/zeroes. Consequently, zero steady state error is difficult to be achieved by instantaneous value control especially under heavy load situations.

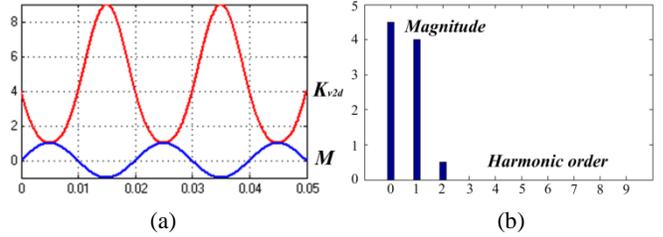


Fig. 10 Loop gain scheduling along sinusoidal operation points: (a). loop gain vs. transfer ratio; (b). FFT analysis of the loop gain vibration.

The reason behind this phenomenon is that the proposed converter shows some inertia inside and cannot be viewed as an ideal amplifier to the modulating signal due to its time variant features. Similar situation happens when investigating the transfer function G_{i2d} for the single-phase ACVD rectifier. Although sizing of the passive components can relax this problem by some extent, the design degree of freedom will be constrained and the passive device installation will be huge. As a result, software solution is preferred to thoroughly fix this issue. The elimination techniques for the distortion problems will be clarified in next section.

V. DESIGN OF THE CONTROL STRATEGIES FOR INVERTER AND RECTIFIER MODES USING STATE SPACE

In this section, the design processes of the controllers under both inverter and rectifier modes are to be facilitated in state space. Based on the decoupling model of proposed converter in SRF, the PI controller is sufficient to achieve zero steady state error. The transfer functions can be investigated by using the root locus analysis to determine the proportional gain and integral rate for the close loop in each control layer.

A. Control Design for Standalone Inverter Mode

The proposed converter is operated as a standalone inverter in voltage control mode, where the main objective to establish stiff AC voltage bus across the load with pre-fined frequency. Based on the SRF model in (25) where the voltage vector is aligned with the d -axis, the decoupling control scheme summarized in Fig. 11(a) is developed. The detailed transfer function is derived as follows.

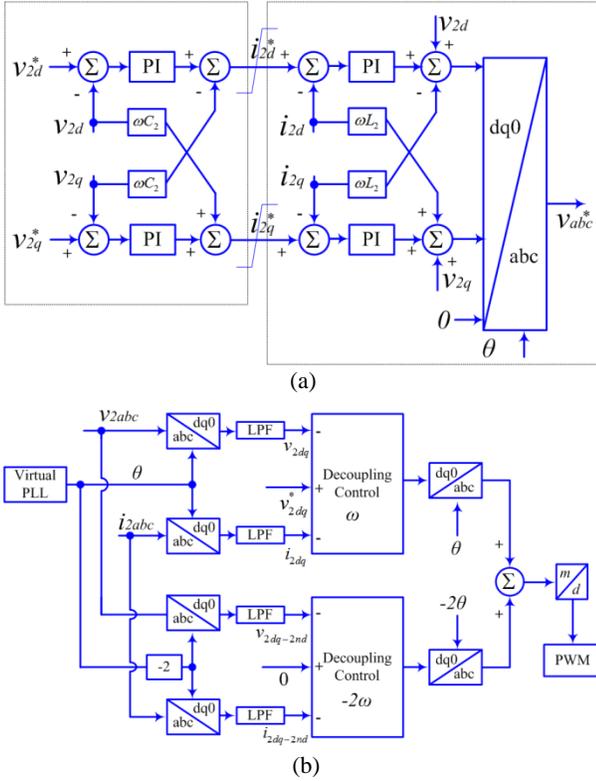


Fig. 11 Control structure in standalone inverter mode: (a). two layers decoupling control; (b) overview of the control diagram including the second order eliminating loop.

Rewrite (25) into (34) for simplification, in which terms $\{\chi_d, \chi_q\}$ and $\{\lambda_d, \lambda_q\}$ can be obtained from the PI controllers in the close loop system.

$$\begin{cases} \frac{d}{dt} \begin{bmatrix} i_{2d} \\ i_{2q} \end{bmatrix} = \frac{1}{L_2} \begin{bmatrix} \chi_d \\ \chi_q \end{bmatrix} - \frac{r_2}{L_2} \begin{bmatrix} i_{2d} \\ i_{2q} \end{bmatrix} \\ \frac{d}{dt} \begin{bmatrix} v_{2d} \\ v_{2q} \end{bmatrix} = \frac{1}{C_2} \begin{bmatrix} \lambda_d \\ \lambda_q \end{bmatrix} - \frac{1}{RC_2} \begin{bmatrix} v_{2d} \\ v_{2q} \end{bmatrix} \end{cases} \quad (34)$$

$$\begin{aligned} \chi_d &= V_{dc} m_d - v_{2d} + \omega L_2 i_{2q} = K_{ip} (i_{2d}^* - i_{2d}) + K_{ii} \int (i_{2d}^* - i_{2d}) dt \\ \chi_q &= V_{dc} m_q - v_{2q} - \omega L_2 i_{2d} = K_{ip} (i_{2q}^* - i_{2q}) + K_{ii} \int (i_{2q}^* - i_{2q}) dt \\ \lambda_d &= i_{2d} + \omega C_2 v_{2q} = K_{vp} (v_{2d}^* - v_{2d}) + K_{vi} \int (v_{2d}^* - v_{2d}) dt \\ \lambda_q &= i_{2q} - \omega C_2 v_{2d} = K_{vp} (v_{2q}^* - v_{2q}) + K_{vi} \int (v_{2q}^* - v_{2q}) dt \end{aligned} \quad (35)$$

From (34), (35) and the definition in (36), the state space equations for the direct axis current and voltage loop can be derived as in (37).

$$\begin{cases} F_{i2d} = \int (i_{2d}^* - i_{2d}) dt \\ F_{v2d} = \int (v_{2d}^* - v_{2d}) dt \end{cases} \quad (36)$$

$$\begin{cases} \frac{d}{dt} \begin{bmatrix} i_{2d} \\ F_{i2d} \end{bmatrix} = \begin{bmatrix} -\frac{K_{ip} + r_2}{L_2} & \frac{K_{ii}}{L_2} \\ -1 & 0 \end{bmatrix} \begin{bmatrix} i_{2d} \\ F_{i2d} \end{bmatrix} + \begin{bmatrix} \frac{K_{ip}}{L_2} \\ 1 \end{bmatrix} i_{2d}^* \\ \frac{d}{dt} \begin{bmatrix} v_{2d} \\ F_{v2d} \end{bmatrix} = \begin{bmatrix} -\frac{K_{vp} R + 1}{RC_2} & \frac{K_{vi}}{C_2} \\ -1 & 0 \end{bmatrix} \begin{bmatrix} v_{2d} \\ F_{v2d} \end{bmatrix} + \begin{bmatrix} \frac{K_{vp}}{C_2} \\ 1 \end{bmatrix} v_{2d}^* \end{cases} \quad (37)$$

In (34), since the quadrature axis holds the same structure with direct axis, the transfer functions can be equivalently achieved as in (38).

$$\begin{cases} G_{i2} = \frac{i_{2d}}{i_{2d}^*} = \frac{i_{2q}}{i_{2q}^*} = \frac{K_{ii} + sK_{ip}}{K_{ii} + s(r_2 + K_{ip}) + s^2 L_2} \\ G_{v2} = \frac{v_{2d}}{v_{2d}^*} = \frac{v_{2q}}{v_{2q}^*} = \frac{K_{vi} + sK_{vp}}{K_{vi} + s(1/R + K_{vp}) + s^2 C_2} \end{cases} \quad (38)$$

Consequently, the current controller reference and the modulating signal into the PWM module can be derived as (39), which is in accordance with Fig. 11(a).

$$\begin{aligned} U_{2d}^* &= \chi_d + v_{2d} - \omega L_2 i_{2q} \\ U_{2q}^* &= \chi_q + v_{2q} + \omega L_2 i_{2d} \\ i_{2d}^* &= \lambda_d - \omega C_2 v_{2q} \\ i_{2q}^* &= \lambda_q + \omega C_2 v_{2d} \end{aligned} \quad (39)$$

The global state space equations for the direct-quadrant decoupling control system can be achieved in (40).

$$\frac{d}{dt} \begin{bmatrix} i_{2d} \\ F_{i2d} \\ v_{2d} \\ F_{v2d} \\ i_{2q} \\ F_{i2q} \\ v_{2q} \\ F_{v2q} \end{bmatrix} = \begin{bmatrix} \frac{K_{ip} + r_2}{L_2} & \frac{K_{ii}}{L_2} & \frac{K_{ip} K_{vp}}{L_2} & \frac{K_{ii} K_{vp}}{L_2} & 0 & 0 & \frac{\omega C_2 K_{vp}}{L_2} & 0 \\ -1 & 0 & -K_{vp} & K_{vi} & 0 & 0 & -\omega C_2 & 0 \\ 0 & 0 & \frac{K_{ip} R + 1}{RC_2} & \frac{K_{vi}}{C_2} & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{\omega C_2 K_{vp}}{L_2} & 0 & \frac{K_{ip} + r_2}{L_2} & \frac{K_{ii}}{L_2} & \frac{K_{ip} K_{vp}}{L_2} & \frac{K_{ii} K_{vp}}{L_2} \\ 0 & 0 & \omega C_2 & 0 & -1 & 0 & -K_{vp} & K_{vi} \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{K_{ip} R + 1}{RC_2} & \frac{K_{vi}}{C_2} \\ 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 \end{bmatrix} \begin{bmatrix} i_{2d} \\ F_{i2d} \\ v_{2d} \\ F_{v2d} \\ i_{2q} \\ F_{i2q} \\ v_{2q} \\ F_{v2q} \end{bmatrix} + \begin{bmatrix} \frac{K_{ip} K_{vp}}{L_2} & 0 \\ K_{vp} & 0 \\ \frac{K_{ip}}{C_2} & 0 \\ 1 & 0 \\ 0 & \frac{K_{ip} K_{vp}}{L_2} \\ 0 & \frac{K_{ii} K_{vp}}{L_2} \\ 0 & K_{vp} \\ 0 & \frac{K_{ip}}{C_2} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} v_{2d}^* \\ v_{2q}^* \end{bmatrix} \quad (40)$$

Recall that the outer loop of the control structure in Fig. 11(a) regulates the AC voltage at load and sets the reference currents (i_{2d}^* and i_{2q}^*) to the inner current loop. The inner current loop regulates the load current and prevents overloading of the converter, and it also generates the first version modulating signals $\{m_{ab}, m_{bc}, m_{ca}\}$, which will be modified to $\{m_a, m_b, m_c\}$ and then $\{d_a, d_b, d_c\}$ for the modulator to generate the gating signals for the switching devices.

Since the proposed converter holds the same structure in the SRF for all frequencies with $n\omega$ (where $n=\pm 1, \pm 2, \pm 3, \dots$) rotational rate under balanced conditions. Thus, the second order distortion problem can be solved by adding an eliminating loop in -2ω SRF that forces its $d-q$ components to zero as shown in Fig. 11(b). Note that the decoupling control block for the eliminating loop is the same as that of the fundamental voltage and current in Fig. 11(a). Low pass filters (LPFs) are employed to achieve the $d-q$ components under each frequency. The output of the supplementary loop that suppresses the second harmonic is added to the fundamental voltage and current loop that responsible for the power transfer between converter AC and DC sides. Based on the proposed design scheme, it is to be expected that the space vector modulation (SVM) method is also applicable to the ACVD converter.

B. Control Design for Rectifier and Grid-connected Inverter Modes

For completeness, the control diagram for the proposed converter in rectifier/grid-connected inverter mode is depicted in Fig. 12(a), where the outer control layers that generate the reference currents for the inner current controllers are to be determined by the operation circumstance and control target. In rectifier mode, unit power factor should be of concerned, thus quadrature current command is set to zero, while the direct current is decided by the DC voltage controller. In distributed energy resource (DER) applications where energy management is necessary, the active power (DC side voltage) and reactive power control layer will generate the references for d -axis and q -axis currents respectively. If the DER interfacing inverter is connected to local microgrid, then voltage support function may be needed. In this case, the AC voltage in the point of common coupling (PCC) should be controlled in outer layer [26, 27].

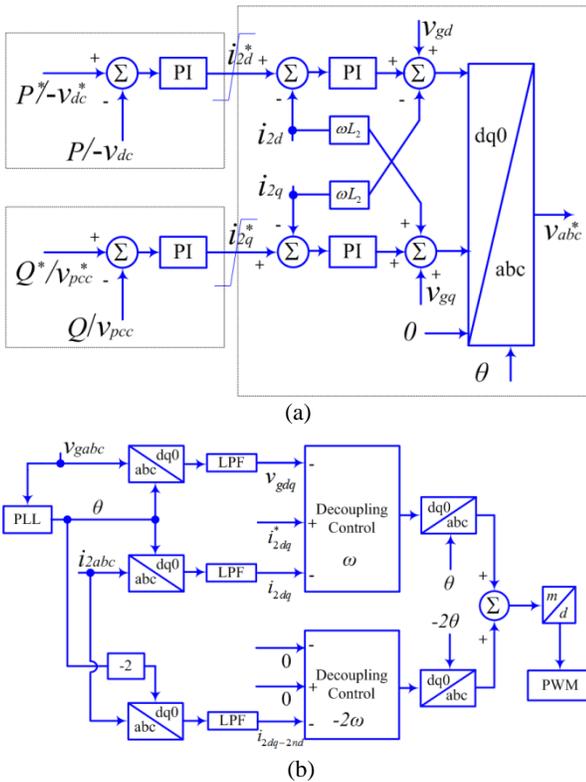


Fig. 12 Control structure in rectifier/grid-connected inverter mode: (a) two layers decoupling control; (b) overview of the control diagram including the second order eliminating loop.

Taking the rectifier mode for example, the transfer functions for the two layers controller can be derived as follows. Rearranging (30) into (41) for simplification, in which terms $\{\gamma_d, \gamma_q\}$ and η can be obtained from the PI controllers in the close loop system.

$$\begin{cases} \frac{d}{dt} \begin{bmatrix} i_{2d} \\ i_{2q} \end{bmatrix} = \frac{1}{L_2} \begin{bmatrix} \gamma_d \\ \gamma_q \end{bmatrix} - \frac{r_2}{L_2} \begin{bmatrix} i_{2d} \\ i_{2q} \end{bmatrix} \\ \frac{dv_{dc}}{dt} = \frac{1}{C_d} \eta - \frac{v_{dc}}{R_d C_d} \end{cases} \quad (41)$$

$$\begin{aligned} \gamma_d &= v_{dc} m_d - v_{gd} + \omega L_2 i_{2q} = K'_{ip} (i_{2d}^* - i_{2d}) + K'_{ii} \int (i_{2d}^* - i_{2d}) dt \\ \gamma_q &= v_{dc} m_q - v_{gq} - \omega L_2 i_{2d} = K'_{ip} (i_{2q}^* - i_{2q}) + K'_{ii} \int (i_{2q}^* - i_{2q}) dt \\ \eta &= - \begin{bmatrix} m_d & m_q \end{bmatrix} \cdot \begin{bmatrix} i_{2d} \\ i_{2q} \end{bmatrix} = K'_{vp} (v_{dc}^* - v_{dc}) + K'_{vi} \int (v_{dc}^* - v_{dc}) dt \end{aligned} \quad (42)$$

From (41), (42) and the definition in (43), the state space equations for the direct current control loop and DC voltage regulation loop can be derived in (44).

$$\begin{cases} F_{i2d} = \int (i_{2d}^* - i_{2d}) dt \\ F_{vdc} = \int (v_{dc}^* - v_{dc}) dt \end{cases} \quad (43)$$

$$\begin{cases} \frac{d}{dt} \begin{bmatrix} i_{2d} \\ F_{i2d} \end{bmatrix} = \begin{bmatrix} -\frac{K'_{ip} + r_2}{L_2} & \frac{K'_{ii}}{L_2} \\ -1 & 0 \end{bmatrix} \begin{bmatrix} i_{2d} \\ F_{i2d} \end{bmatrix} + \begin{bmatrix} \frac{K'_{ip}}{L_2} \\ 1 \end{bmatrix} i_{2d}^* \\ \frac{d}{dt} \begin{bmatrix} v_{dc} \\ F_{vdc} \end{bmatrix} = \begin{bmatrix} -\frac{K'_{vp} R_d + 1}{R_d C_d} & \frac{K'_{vi}}{C_d} \\ -1 & 0 \end{bmatrix} \begin{bmatrix} v_{dc} \\ F_{vdc} \end{bmatrix} + \begin{bmatrix} \frac{K'_{vp}}{C_d} \\ 1 \end{bmatrix} v_{dc}^* \end{cases} \quad (44)$$

In (41), since the quadrant axis has the same structure with direct axis, the transfer functions can be equivalently achieved as in (45).

$$\begin{cases} G'_{i2} = \frac{i_{2d}}{i_{2d}^*} = \frac{i_{2q}}{i_{2q}^*} = \frac{K'_{ii} + sK'_{ip}}{K'_{ii} + s(r_2 + K'_{ip}) + s^2 L_2} \\ G'_{vdc} = \frac{v_{dc}}{v_{dc}^*} = \frac{K'_{vi} + sK'_{vp}}{K'_{vi} + s(1/R_d + K'_{vp}) + s^2 C_d} \end{cases} \quad (45)$$

Since the q -axis reference is to be zero, the actual value of quadrature current is very small. Based on this approximation, the direct current controller reference and the modulating signal into the PWM module is then shown in (46), which is in accordance with Fig. 12(a).

$$\begin{aligned} U_{2d}^* &= \gamma_d + v_{gd} - \omega L_2 i_{2q} \\ U_{2q}^* &= \gamma_q + v_{gq} + \omega L_2 i_{2d} \\ i_{2d}^* &= -\eta \end{aligned} \quad (46)$$

The global state space equations for the d - q decoupling control of the proposed rectifier system are then clarified in (47).

$$\frac{d}{dt} \begin{bmatrix} i_{2d} \\ F_{i2d} \\ i_{2q} \\ F_{i2q} \\ v_{dc} \\ F_{vdc} \end{bmatrix} = \begin{bmatrix} -\frac{K'_{ip} + r_2}{L_2} & \frac{K'_{ii}}{L_2} & 0 & 0 & \frac{K'_{ip} K'_{vp}}{L_2} & -\frac{K'_{ip} K'_{vi}}{L_2} \\ -1 & 0 & 0 & 0 & K'_{ip} & -K'_{ii} \\ 0 & 0 & -\frac{K'_{ip} + r_2}{L_2} & \frac{K'_{ii}}{L_2} & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{K'_{vp} R_d + 1}{R_d C_d} & \frac{K'_{vi}}{C_d} \\ 0 & 0 & 0 & 0 & -1 & 0 \end{bmatrix} \begin{bmatrix} i_{2d} \\ F_{i2d} \\ i_{2q} \\ F_{i2q} \\ F_{vdc} \\ F_{vdc} \end{bmatrix} + \begin{bmatrix} -\frac{K'_{ip} K'_{vp}}{L_2} \\ -K'_{ip} \\ 0 \\ 0 \\ \frac{K'_{ip}}{C_d} \\ 1 \end{bmatrix} v_{dc}^* \quad (47)$$

The outer layer with active power controller, reactive power controller or DER DC voltage controller situations can be solved by the proposed state space approach similarly. The overall control scheme including the second order current elimination is demonstrated in Fig. 12(b).

VI. EXPERIMENTAL VERIFICATION

In attempt to substantiate the discussions and analysis presented in previous sections, a 2.5kVA prototype of the three-phase ACVD converter in Fig. 2(a) is constructed with the following specifications: 200V DC-link voltage; AC side phase voltage of 170V-3 Φ (peak value); 10kHz switching frequency (f_s); 470 μ F DC capacitance (C_d); 2mH IBBC inductance (L_I); 10 μ F IBBC capacitance (C_I); 5mH AC side inductance (L_2); and 10 μ F AC side capacitance C_2 . In this case, the maximum AC output phase voltage is 200V. Compared with the 400V voltage stress for conventional VSC, the IGBT voltage stresses in ACVD converter are fluctuant around 400V with an AC component equal to output voltage (this fluctuant voltage can significantly reduce the capacitor size). The AC side capacitor voltage and AC side inductor current are equal to the output voltage and output current respectively. In this demonstration, the Texas Instrument DSP TMS320F28335 is used for digital implementation of the modulation and control systems in this paper.

Initially, this prototype is operated in inversion mode to demonstrate its ability to cope with different power factors (unity, leading and lagging power factors).

The footprint of the tested prototype is shown in Fig. 13(a). To demonstrate the effectiveness of the integration design of L_I and L_2 as discussed in section III, a low power integrated magnetic inductor is built as shown in Fig. 13(b) and tested when one of its phases is operated as a single-phase standalone inverter from 50V DC-link without incorporation of second harmonic compensation loop. The voltage and current waveforms of the IBBC are shown in Fig. 14(a). The results in Fig. 14(b) have shown that the integrated design of the two inductors L_I and L_2 is able to work independently in one core without any noticeable performance degradation. Therefore, the magnetic integration technique is to be an effective solution in confine space applications where compact hardware design is preferred. Observe that the open loop output voltage and its spectrum in Fig. 15 exhibit certain amount of second order harmonic, which is in line with the previous analysis. In Fig. 15(a), the zero-crossing point drifts by 0.4ms and 3.7% of second harmonic can be observed from Fig. 15(b). This distortion is expected to be aggravated as the power increases, necessitating the incorporation of the second order harmonic mitigation mechanism within the converter control loop.



Fig. 13 Photographs of (a). prototype for the power circuit of the proposed (three-phase) and its drivers and (b). integrated design of magnetic parts (L_I and L_2).

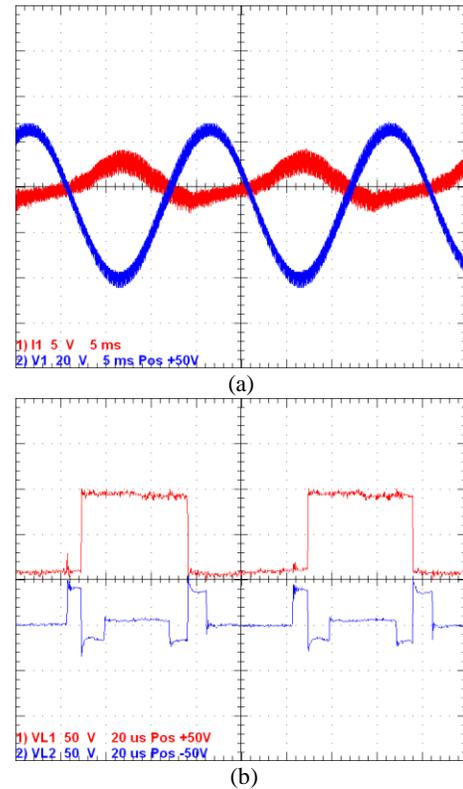


Fig. 14 Voltage and current waveforms of the state variables (5ms/div): (a). IBBC inductor current (5A/div) and IBBC capacitor voltage (20V/div); (b). Voltage across the two windings in the integrated magnetic component (50V/div).

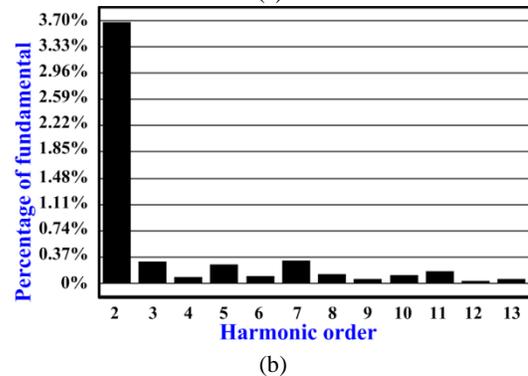
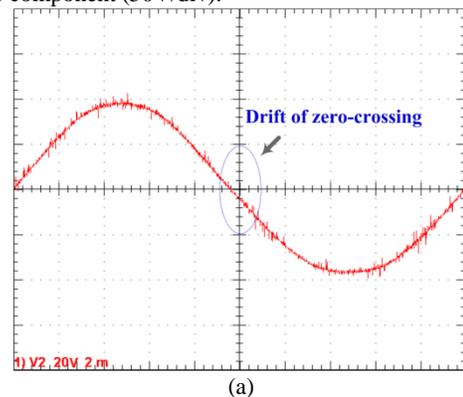


Fig. 15 Open loop output voltage with second order harmonic distortion: (a). output voltage waveform (20V/div, 2ms/div); (b). distribution of the base band harmonics.

In order to eliminate the second harmonic from the output voltage (thus, the output current), the control strategy depicted in Fig. 11 (a) and (b) involving both fundamental regulation

and harmonic elimination is adopted. This time, the proposed converter is operated in a three-phase configuration.

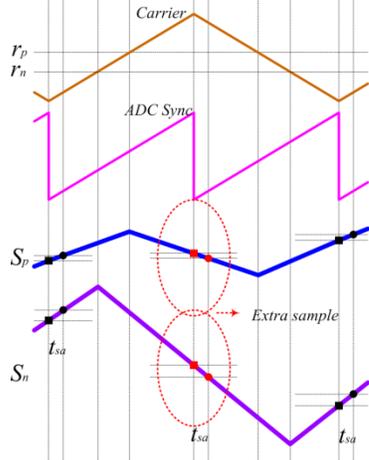


Fig. 16 ADC synchronization for asymmetric ripple compensation.

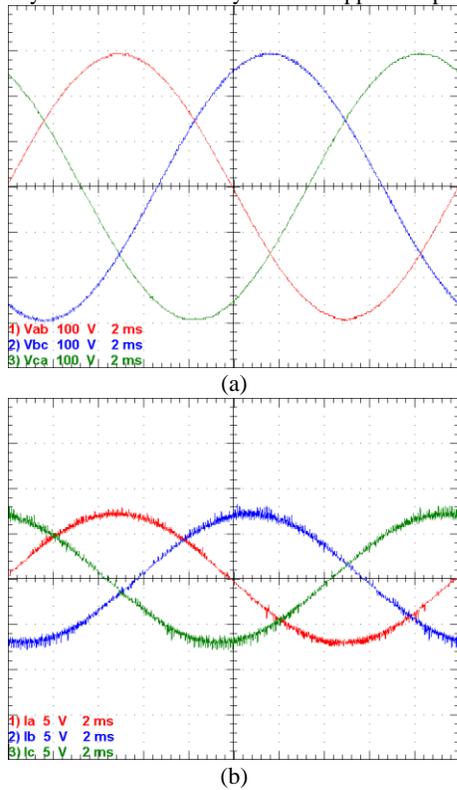


Fig. 17 Output waveforms for Standalone inverter mode (2ms/div): (a). line-to-line voltage (100V/div); (b) line current under 22Ω resistive load (5A/div).

Fig. 16 shows the ADC synchronization scheme employed to compensate the asymmetric deviation from average value during positive and negative half cycles. r_p and r_n are the reference values with 180 degree apart, while S_p and S_n are the state variables accordingly. The ADC time t_{sa} will cause some drift from the mid-point. Since the voltage/current slopes in the positive half cycle and negative half cycle are asymmetric for the proposed ACVD converter, some DC bias will appear when micro-controller samples one point (multi-times) per switching cycle. In another word, sampling process must strictly obey the Shannon principle, which demands the sampling speed to be at least two times of switching frequency. Consequently, the ADC module is suggested to be

synchronized at double frequency of the PWM generator. In this way, the extra samples can compensate the asymmetric deviation from the actual value and eliminate the DC bias.

Fig. 17 shows the output line-to-line voltage and three-phase currents obtained from standalone operation of the proposed converter in inversion mode. The THD for the voltage and current waveforms in Fig. 17 that obtained from the FFT analysis are both lower than 1%, which are expected to meeting the IEEE and IEC harmonic standards. Besides, the peak line-to-line voltage of 295V is achieved from 200V DC-link, which is beyond the DC utilization of 0.866pu for conventional two-level VSC. This confirms the claim made in this paper regarding the extended output voltage range of the proposed converter.

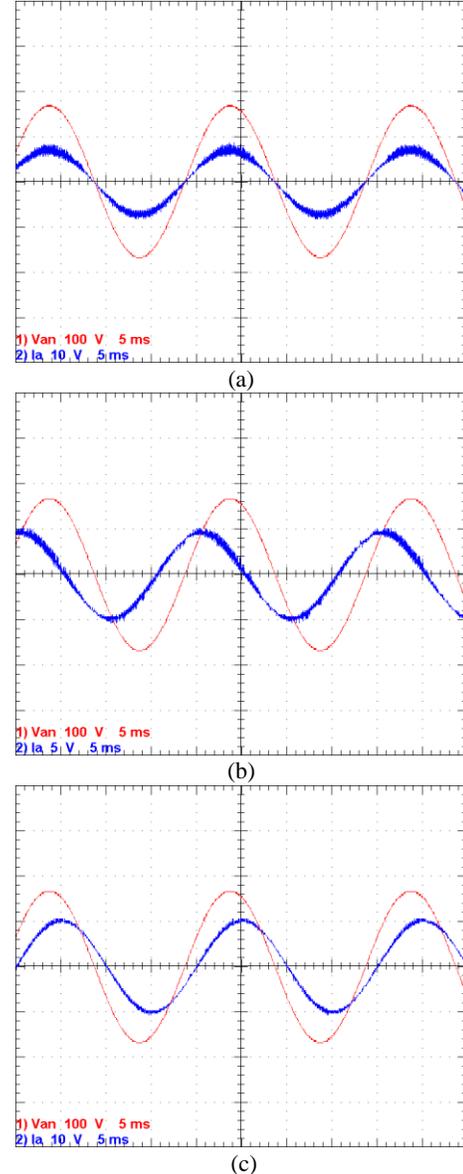


Fig. 18 Phase voltage/current waveforms of the ACVD-VSC under different load conditions (5ms/div): (a). phase voltage (100V/div) and phase current (10A/div) with 22Ω resistive load; (b). phase voltage (100V/div) and phase current (5A/div) with 22Ω +100μF capacitive load; (c). phase voltage (100V/div) and phase current (10A/div) with 15Ω +30mH inductive load.

Fig. 18(a)-(c) are presented to demonstrate the operability of the proposed ACVD converter as islanded inverter with resistive, capacitive and inductive loads. These plots have shown that this converter is able to operate under these operating conditions, without any noticeable difficulty or deterioration in its performance.

Fig. 19(a) presents the snapshot of the load neutral point voltage relative to ground which is fixed at negative DC bus. It is observed that the CM voltage has no DC component and holds bi-polar nature that switches around zero (real ground). This reduces the insulation requirement on the load connected to the AC side of this converter as previously stated. The energy conversion efficiency of the proposed converter as standalone inverter with resistive load is assessed compared with two-level inverter with the same DC-link voltage, modulation index and power rating. Fig. 19(b) has shown the efficiency comparison between the two converters. It is seen that the overall efficiency of the ACVD inverter is marginally lower than the two-level inverter. This is because the current stresses are nearly the same for the two converters in this application.

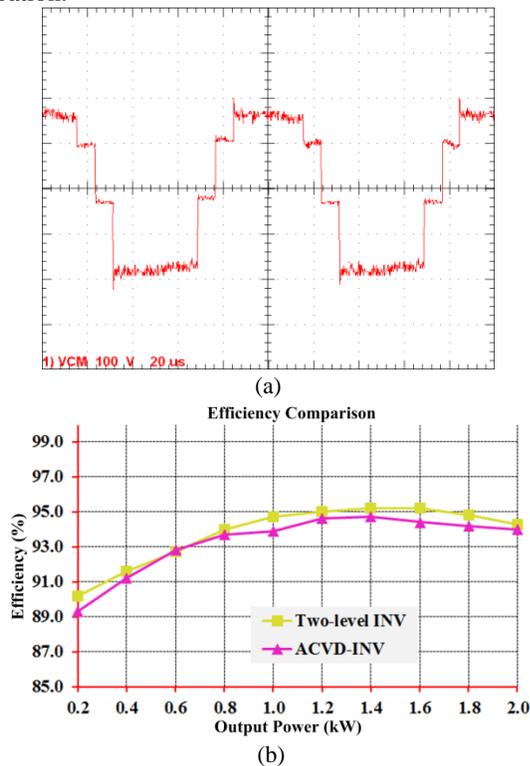


Fig. 19 CM voltage and efficiency examination for proposed converter: (a). CM voltage between DC ground and AC neutral (100V/div, 20μs/div); (b). efficiency performance for standalone inverter mode.

The feasibility of proposed converter for unity power factor rectifier application is also tested using the same prototype in Fig. 13(a). The AC input voltage is 150V-3Φ (peak value), and DC output voltage is regulated at 200V with resistance of 47Ω. In this demonstration, the control system for rectifier operation depicted in Fig. 12 is used. The DC output voltage, input phase current and grid voltage waveform are displayed in Fig. 20. It can be observed that the input AC current is in phase with grid voltage.

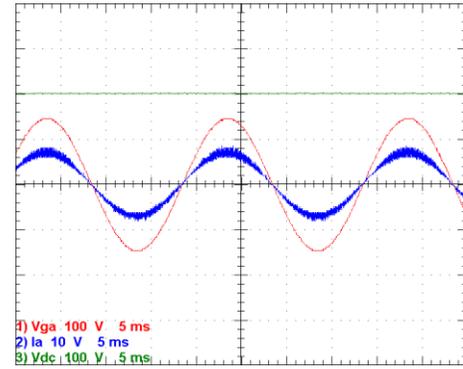


Fig. 20 Grid voltage (100V/div), phase current (5A/div) and DC output voltage (100V/div) for ACVD rectifier with 47Ω load (5ms/div).

Based on the results obtained for inverter and rectifier operations demonstrated in this section, the bidirectional operation ability of the proposed ACVD converter is proved.

It can be summarized that the proposed ACVD converter is qualified as a four-quadrant voltage source converter under various conditions with extended AC voltage output range, high power density (twice of the output of the two-level topology from the same input DC link), and high conversion efficiency. Besides, the CM voltage can be suppressed to zero DC component. Although extra current is generated from IBBC, the output power can be twice of that in two-level converter since the AC output voltage can be doubled, which means there is no appreciable degradation on efficiency performance for the ACVD-VSC.

VII. CONCLUSIONS

In this paper, the three-phase voltage source converter with AC side voltage-doubling and DC common mode voltage suppression features is proposed. Due to the introduced IBBC, the DC-link utilization is extended to 1pu on the phase voltage (twice of that in two-level voltage source converter). Consequently, the sizes of DC-link capacitor and interfacing transformer are greatly diminished. Due to the inherent ground on the negative terminal of DC-link, the DC component in CM voltage seen from the AC side neutral point can be avoided. It has been shown that reliance of the proposed converter on IBBC to synthesize negative half of the output voltage introduces second order harmonics in the AC side voltage and current when operated in open loop. The *d-q* SRF models of the proposed converter when operated in islanding or as a grid connected converter are presented, which are in further used to design the necessary control loops for fundamental power transfer and elimination of the second order harmonic distortions observed during open loop operation. This paper also described the converter operating principle and brief assessments of the voltage and current stresses on the semiconductor switches of the proposed converter. Experimental results have substantiated the claimed attributes of the proposed ACVD-VSC, including its four-quadrant operation.

REFERENCES

- [1] T. Friedli, J. W. Kolar, J. Rodriguez, and P. W. Wheeler, "Comparative Evaluation of Three-Phase AC-AC Matrix Converter

- and Voltage DC-Link Back-to-Back Converter Systems," *Industrial Electronics, IEEE Transactions on*, vol. 59, pp. 4487-4510, 2012.
- [2] J. W. Kolar, T. Friedli, J. Rodriguez, and P. W. Wheeler, "Review of Three-Phase PWM AC-AC Converter Topologies," *Industrial Electronics, IEEE Transactions on*, vol. 58, pp. 4988-5006, 2011.
- [3] X. Changliang, Z. Faqiang, W. Zhiqiang, and H. Xiangning, "Equivalent Switch Circuit Model and Proportional Resonant Control for Triple Line-Voltage Cascaded Voltage-Source Converter," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 2389-2401, 2013.
- [4] S. Rodrigues, R. T. Pinto, P. Bauer, and J. Pierik, "Optimal Power Flow Control of VSC-Based Multiterminal DC Network for Offshore Wind Integration in the North Sea," *Emerging and Selected Topics in Power Electronics, IEEE Journal of*, vol. 1, pp. 260-268, 2013.
- [5] Z. Changzheng, D. Shaowu, and C. Qiaofu, "A Novel Scheme Suitable for High-Voltage and Large-Capacity Photovoltaic Power Stations," *Industrial Electronics, IEEE Transactions on*, vol. 60, pp. 3775-3783, 2013.
- [6] J. Chivite-Zabalza, Rodri, x, M. A. guez Vidal, P. Izurza-Moreno, G. Calvo, *et al.*, "A Large Power, Low-Switching-Frequency Voltage Source Converter for FACTS Applications With Low Effects on the Transmission Line," *Power Electronics, IEEE Transactions on*, vol. 27, pp. 4868-4879, 2012.
- [7] G. P. Adam, K. H. Ahmed, S. J. Finney, K. Bell, and B. W. Williams, "New Breed of Network Fault-Tolerant Voltage-Source-Converter HVDC Transmission System," *Power Systems, IEEE Transactions on*, vol. 28, pp. 335-346, 2013.
- [8] J. Beerten, S. Cole, and R. Belmans, "Modeling of Multi-Terminal VSC HVDC Systems With Distributed DC Voltage Control," *Power Systems, IEEE Transactions on*, vol. 29, pp. 34-42, 2014.
- [9] O. S. Senturk, L. Helle, S. Munk-Nielsen, P. Rodriguez, and R. Teodorescu, "Power Capability Investigation Based on Electrothermal Models of Press-Pack IGBT Three-Level NPC and ANPC VSCs for Multimegawatt Wind Turbines," *Power Electronics, IEEE Transactions on*, vol. 27, pp. 3195-3206, 2012.
- [10] F. Wanmin, R. Xinbo, and W. Bin, "A Generalized Formulation of Quarter-Wave Symmetry SHE-PWM Problems for Multilevel Inverters," *Power Electronics, IEEE Transactions on*, vol. 24, pp. 1758-1766, 2009.
- [11] U. T. Shami and H. Akagi, "Identification and Discussion of the Origin of a Shaft End-to-End Voltage in an Inverter-Driven Motor," *Power Electronics, IEEE Transactions on*, vol. 25, pp. 1615-1625, 2010.
- [12] U. T. Shami and H. Akagi, "Experimental Discussions on a Shaft End-to-End Voltage Appearing in an Inverter-Driven Motor," *Power Electronics, IEEE Transactions on*, vol. 24, pp. 1532-1540, 2009.
- [13] T. Maetani, S. Morimoto, K. Yamamoto, Y. Isomura, A. Watanabe, and K. Nakano, "Shaft voltage comparison between grounded and ungrounded brushless DC motors with insulated rotor driven by PWM inverter," in *Electrical Machines and Systems (ICEMS), 2012 15th International Conference on*, 2012, pp. 1-6.
- [14] Y. Bo, L. Wuhua, G. Yunjie, C. Wenfeng, and H. Xiangning, "Improved Transformerless Inverter With Common-Mode Leakage Current Elimination for a Photovoltaic Grid-Connected Power System," *Power Electronics, IEEE Transactions on*, vol. 27, pp. 752-762, 2012.
- [15] G. Yunjie, L. Wuhua, Z. Yi, Y. Bo, L. Chushan, and H. Xiangning, "Transformerless Inverter With Virtual DC Bus Concept for Cost-Effective Grid-Connected PV Power Systems," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 793-805, 2013.
- [16] J. W. Shin, H. Shin, G. S. Seo, J. I. Ha, and B. H. Cho, "Low-Common Mode Voltage H-Bridge Converter with Additional Switch Legs," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 1773-1782, 2013.
- [17] H. Akagi and T. Doumoto, "An approach to eliminating high-frequency shaft voltage and ground leakage current from an inverter-driven motor," *Industry Applications, IEEE Transactions on*, vol. 40, pp. 1162-1169, 2004.
- [18] Dura, x, M. J. n, J. Prieto, and F. Barrero, "Space Vector PWM With Reduced Common-Mode Voltage for Five-Phase Induction Motor Drives Operating in Overmodulation Zone," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 4030-4040, 2013.
- [19] C. C. Hou, C. C. Shih, P. T. Cheng, and A. M. Hava, "Common-Mode Voltage Reduction Pulsewidth Modulation Techniques for Three-Phase Grid-Connected Converters," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 1971-1979, 2013.
- [20] Y. Otani, T. Isobe, and R. Shimada, "Control and design principle of a soft-switching boost dc to ac converter without smoothing capacitor using a MERS pulse link concept," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, 2011, pp. 2102-2108.
- [21] W. Weimin, H. Yuanbin, and F. Blaabjerg, "An LLCL Power Filter for Single-Phase Grid-Tied Inverter," *Power Electronics, IEEE Transactions on*, vol. 27, pp. 782-789, 2012.
- [22] K. Ilves, A. Antonopoulos, S. Norrga, and H. P. Nee, "Steady-State Analysis of Interaction Between Harmonic Components of Arm and Line Quantities of Modular Multilevel Converters," *Power Electronics, IEEE Transactions on*, vol. 27, pp. 57-68, 2012.
- [23] J. D. Van Wyk, F. C. Lee, L. Zhenxian, R. Chen, W. Shuo, and L. Bing, "Integrating active, passive and EMI-filter functions in power electronics systems: a case study of some technologies," *Power Electronics, IEEE Transactions on*, vol. 20, pp. 523-536, 2005.
- [24] Z. Yi, L. Wuhua, D. Yan, and H. Xiangning, "Analysis, Design, and Experimentation of an Isolated ZVT Boost Converter With Coupled Inductors," *Power Electronics, IEEE Transactions on*, vol. 26, pp. 541-550, 2011.
- [25] L. Wuhua, L. Peng, Y. Huan, and H. Xiangning, "Three-Level Forward-Flyback Phase-Shift ZVS Converter With Integrated Series-Connected Coupled Inductors," *Power Electronics, IEEE Transactions on*, vol. 27, pp. 2846-2856, 2012.
- [26] Q. Shafiee, J. M. Guerrero, and J. C. Vasquez, "Distributed Secondary Control for Islanded Microgrids - A Novel Approach," *Power Electronics, IEEE Transactions on*, vol. 29, pp. 1018-1031, 2014.
- [27] Y. A. R. I. Mohamed, H. H. Zeineldin, M. M. A. Salama, and R. Seethapathy, "Seamless Formation and Robust Control of Distributed Generation Microgrids via Direct Voltage Control and Optimized Dynamic Power Sharing," *Power Electronics, IEEE Transactions on*, vol. 27, pp. 1283-1294, 2012.



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