Ultrafast photonic packet switching with optical control

Ivan Glesk, Koo I. Kang, and Paul R. Prucnal

Department of Electrical Engineering, Princeton University, Princeton, NJ 08544

glesk@ee.princeton.edu

Abstract: We report the demonstration of all-optical multi-bit address recognition at 250 Gb/s using a self-routing scheme. With bit period being only 4 ps, two address bits from each packet header were used for routing. Photonic packets can be removed(dropped) by a routing switch from network traffic at their destination. The packet-switching bit-error rate was measured to be less than 10^{-9}.

OCIS code: (060.0060) Fiber optics and optical communications; (320.7080) Ultrafast devices

Reference and links

1. I. Glesk, K. I. Kang, and P. R. Prucnal, "Ultrafast All-Optically Controlled 2x2 Crossbar Switch", *IEEE/LEOS '96 Annual Meeting*, vol. **2**, Paper WS3, p. 149, Boston, MA, November 18-21, 1996.
2. P.R. Prucnal , "Optically Processed Self-Routing, Synchronization, and Contention Resolution for 1-D and 2-D Photonic Switching Architectures," *IEEE J. Quantum Electron.* **29**, 600 (1993).
3. J.P. Sokoloff, P.R. Prucnal, I. Glesk, and M. Kane, "A Terahertz Optical Asymmetric Demultiplexer (TOAD)," *IEEE Photonics Technol. Lett.* **5** (7), 787 (1993).
4. I. Glesk, J. P. Sokoloff, P. R. Prucnal, "Demonstration of All-Optical Demultiplexing of TDM Data at 250 Gb/s," *Electron. Lett.* **30** (4), 339 (1994).
5. I. Glesk and P. R. Prucnal, "250 Gb/s Self-Clocked Optical TDM with a Polarization-Multiplexed Clock," *Fiber Integr. Opt.* **14**, 71 (1995).
6. I. Glesk, J. P. Sokoloff, and P. R. Prucnal, "All-Optical Address Recognition and Self-Routing in a 250 Gb/s Packet-Switched Network," *Electron. Lett.* **30**, 1322 (1994).
7. I. Glesk, P. R. Prucnal, and B. Wang, "Ultra-Fast Photonic Packet Switching with Optically Processed Control," in *Photonics in Switching*, Vol. **12** of 1995 OSA Technical Digest Series (Optical Society of America, Washington, D.C., 1995), p. 58.
8. D.Cotter, J.K.Lucek, M.Shabeer, K.Smith, D.C.Rogers, D. Nesset, and P. Gunning,: "Self-Routing of 100 Gbit/s Packets using 6-bit 'Keyword' Address Recognition," *Electron. Lett.* **31**, 1475 (1995).
9. L.Thylén, G. Karlsson, and O. Nilsson: "Switching Technologies for Future Guided Wave Optical Networks: Potentials and Limitations of Photonics and Electronics," *IEEE Commun. Magazine* **34**, 106 (1996).
10. M. J. Adams, D.A.O. Davies, M.C.Tatham, and M. A. Fisher,"Nonlinearities in Semiconductor Laser Amplifiers," *Opt. Quantum Electron.* **27**, 1 (1995).

1. Introduction

Today's communication networks, packet- or circuit-switched, are characterized by hybrid architectures. In these architectures, electronics nodes are connected by optical links. Switching is usually performed electronically because of the advanced state of electronic switching technology. High throughput can be achieved in electronic switching architectures through high dimensionality since the transmission bandwidth at each individual channel is limited to a few tens of gigahertz (GHz). However, the relatively low transmission bandwidth of the electronics, the associated optoelectronics interfaces, and the electronics for routing control, present an obstacle to fully utilize the large bandwidth offered by optical fibers. This obstacle can be eliminated if signals remain in optical form during switching, address recognition, and signal processing.

#2225 - $10.00 US Received July 16, 1997; Revised August 28, 1997

The first step to complete the all-optical transmission path is to replace gigahertz bandwidth optoelectronic switches with terahertz bandwidth all-optical photonic switches [1]. All-optical switches also avoid the delays associated with optoelectronic conversion, and if needed, can preserve the phase information carried by the light. Eliminating the optoelectronic interface also decreases the hardware complexity and failure rate of the network nodes. To date, the leading technology for building photonic switches has been integrated optics. The fabrication of large-dimension optical switching architectures using integrated optics is limited by several factors [2]. Therefore, in contrast to electronic switches, large throughput can be achieved in optical switching architectures through very high transmission bandwidth rather than large dimensionality.

The second step in completing the all-optical path is to replace the electronic signal processing associated with switching by all-optical signal processing. This can avoid a data flow bottleneck at the input to the photonic switch and reduce the need for flow control.

The third step in completing all-optical path is to eliminate opto-electronic conversion associated with packet address reading and use all-optical address recognition instead.

We have demonstrated ultrafast optical flow control using a recently developed Terahertz Optical Asymmetric Demultiplexer (TOAD) [3-5]. By encoding data as optical packets, the data were routed through a network of all-optical switches without the need for any electro-optic or opto-electronic conversion [1].

In present fiber-optic packet- or circuit-switched networks, address recognition and routing are handled in electronic domain. As the transmission rates increase it will become more difficult to perform these tasks using electronics. This limitation can be overcome by implementing all-optical address recognition including self routing of photonic packets. Furthermore, with the anticipated development of "opto-optic" switches, switching networks can be all-optical if optical processing is used. We report the demonstration of the all-optical address recognition and self-routing of a photonic packet without the need for any opto-electronic conversion for a case of two bit addressing. The bit rate was 0.25 Tb/s (4 ps spacing between bits). BER measurements of the set switching state were made by modulating bit 2 with a pseudorandom bit stream and monitoring the bit-error rate at the switching element. BER of less than 10^{-9} were measured. This optically-transparent self-routing switching node can serve as a modular building block for 2-connected optical mesh networks.

2. Address recognition and packet dropping at 250 Gb/s

Many functions must be performed to control a switching node. One important function is routing. The routing of incoming packets at a switching node requires first recognizing address information contained in the headers. In ultra-high speed networks, address bits in an optically compressed packet are spaced only picoseconds apart. Address recognition can only be performed by using ultrafast demultiplexers, each reads one address bit in the header. Once the address bits of each packet are read, the routing switch can be set to properly route the packets by a routing controller. One device capable of reading address bits at such high bit rates is the TOAD [6]. This device in principle can demultiplex a picosecond time-slot from a nanosecond address-frame. It requires less than one picojoule of switching energy and can be made small enough to be integrated on a chip. In the next paragraph we will briefly review the TOAD operation.

2.1 Address recognition using an array of TOADs

The TOAD (figure 1a) is composed of a small optical fiber loop mirror, a nonlinear element - Semiconductor Optical Amplifier (SOA), an intraloop 2x2 coupler for injecting control pulses into the SOA, and an adjustable fiber delay line (AD) which positions SOA near the optical midpoint of the loop mirror. When a train of closely spaced address bit pulses enters the TOAD, each address bit splits equally into a clockwise component (CW) and counterclockwise (CCW) component. They counter-propagate around the loop and arrive at

#2225 - $10.00 US Received July 16, 1997; Revised August 28, 1997

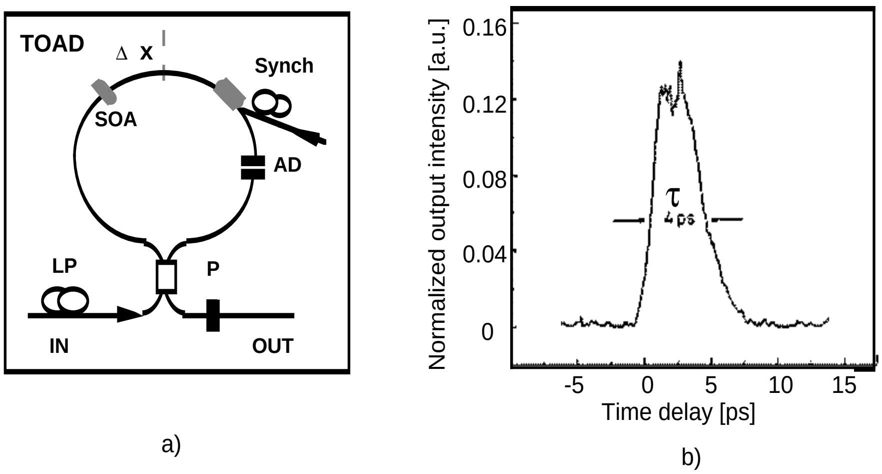

Fig. 1. a) TOAD diagram; b) 4 ps switching window

the SOA at slightly different times as determined by the offset, Δx, of the near edge of the SOA from the midpoint of the loop. A control pulse arrives at the SOA before the CCW component of the signal pulse (address bit) which is to be demultiplexed, but just after its CW counterpropagating component, and induces nonlinearities in the SOA which cause the two components to experience different losses and phase shifts, and consequently recombine and exit the loop at the output port. All other address bit pulses (for which the counterpropagating components do not straddle the control pulse arrival at the SOA) exit the loop at the input port.

As seen in figure 1b), the rising edge of the normalized output intensity, when measured as a function of the delay of the signal pulse relative to the control pulse, is nearly a step function (it "follows" the rising edge of the control pulse). The duration of the falling edge is limited by the transit time through the SOA, nL/c_o, where n and L are the refractive index and length of the SOA respectively. The duration of the flat top is $2n_g\Delta x/c_o$, where n_g is the refractive index of the loop and c_o is the speed of light in vacuum. The switching window is defined here as the full width at half maximum (FWHM) of the normalized output intensity as indicated in figure 1b). This 4 ps switching window was obtained when 500 µm long SOA was placed asymmetrically about the loop midpoint with one end approximately 100 µm from the loop midpoint. The pulse energy in each address bit was 100 fJ. 600 fJ of control pulse energy was needed to induce sufficient nonlinearity for demultiplexing the address bits at 250 Gb/s.

3. Experimental demonstration

To demonstrate two-bit all-optical address recognition and packet dropping in self-routing scheme, one node of a network of 2x2 switches was used which is schematically shown in figure 2. In general, the switching node consists of an electro-optic switching element SW (e.g. 2x2 $LiNbO_3$ cross-bar switch) with two possible states, switched (cross) or unswitched (bar) state, an ultra-fast all-optical address recognition unit (ARU) which decodes the destination address, a routing controller which sets the state of the switching element, and an optical buffer that matches the delay of the input packets to the processing delays of the routing controller.

The full experimental setup is shown in figure 3. One ps pulses at 1.313 µm are generated from a 100 ps, 100 MHz repetition rate Nd:YLF laser followed by an optimized

#2225 - $10.00 US Received July 16, 1997; Revised August 28, 1997

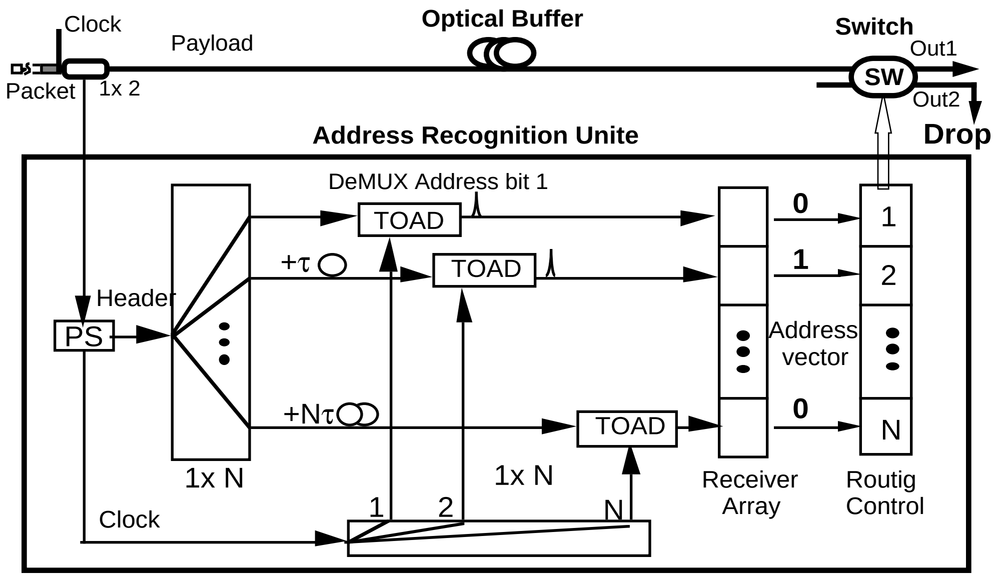

Fig. 2. Node diagram with incoming photonic packets

fiber-grating stage. Each of these pulses is then divided into 4 pulses: three packet bits and an orthogonally polarized clock pulse which is used for synchronization at the demultiplexers. Channel B1 and channel B3 (see figure 3) use adjustable delays, AD, to position 1 ps pulses into 4 ps bit intervals situated on either side of bit 2 (channel B2). Channel B2 is modulated with a "1010..." pattern using a 3 GHz integrated Mach-Zehnder modulator. The channels are set equal in intensity by variable neutral density filters, NDF. In this way packets with two differentheaders, "10" and "11", and identical payloads, "1000...0", are generated (see timing diagram in figure 4a).

The repetition rate of the mode-locked laser (1/T = 100 MHz) determines the packet slot width. The packet length is T_p = (T - GB), where GB is the guardband separating adjacent packets. The size of the guardband is determined by the switching speed of the 2x2 routing switch (SW).

Loop polarizers set the clock and data pulses into orthogonal polarization states, and a polarization combiner was then used to polarization multiplex the clock and the packet header data onto a common transmission line. This is the self-routing feature of the system. Any changes in the length of the transmission line are not critical, since the clock's placement within the packet is not changed. Using an adjustable delay, AD1, the clock pulse was positioned in an arbitrary time slot, *i*, of the packet header (see timing diagram in figure 4b).

Before entering the 2x2 $LiNbO_3$ routing crossbar switch a portion of the incoming signal was split off at the 10:1 polarization splitter, S. A smaller portion of the signal was sent into the array of two TOADs which were used as address recognition unit, ARU. Before entering the ARU, the clock pulse was separated from the packet by using a fiber polarization beam splitter, PS, then split using 50/50 1x2 fiber splitter. Finally, the clock pulse was directed through an adjustable delays, AD_c, into the TOADs control port. Using the same technique, the packet was also split and then injected into input port of the TOAD1 and TOAD2.

By positioning the clock pulse relative to the desired address bit within the packet header frame using AD_c, different address bits were demultiplexed and appeared at the output ports of the TOADs (see figure 4d-f). The outputs of the TOAD1 and TOAD2 were monitored by the photodetectors PD1, PD2 and a fast "AND" gate, &, which upon receiving the demultiplexed address bits triggered a pulse generator, PG, which in turn set the 2x2

#2225 - $10.00 US Received July 16, 1997; Revised August 28, 1997

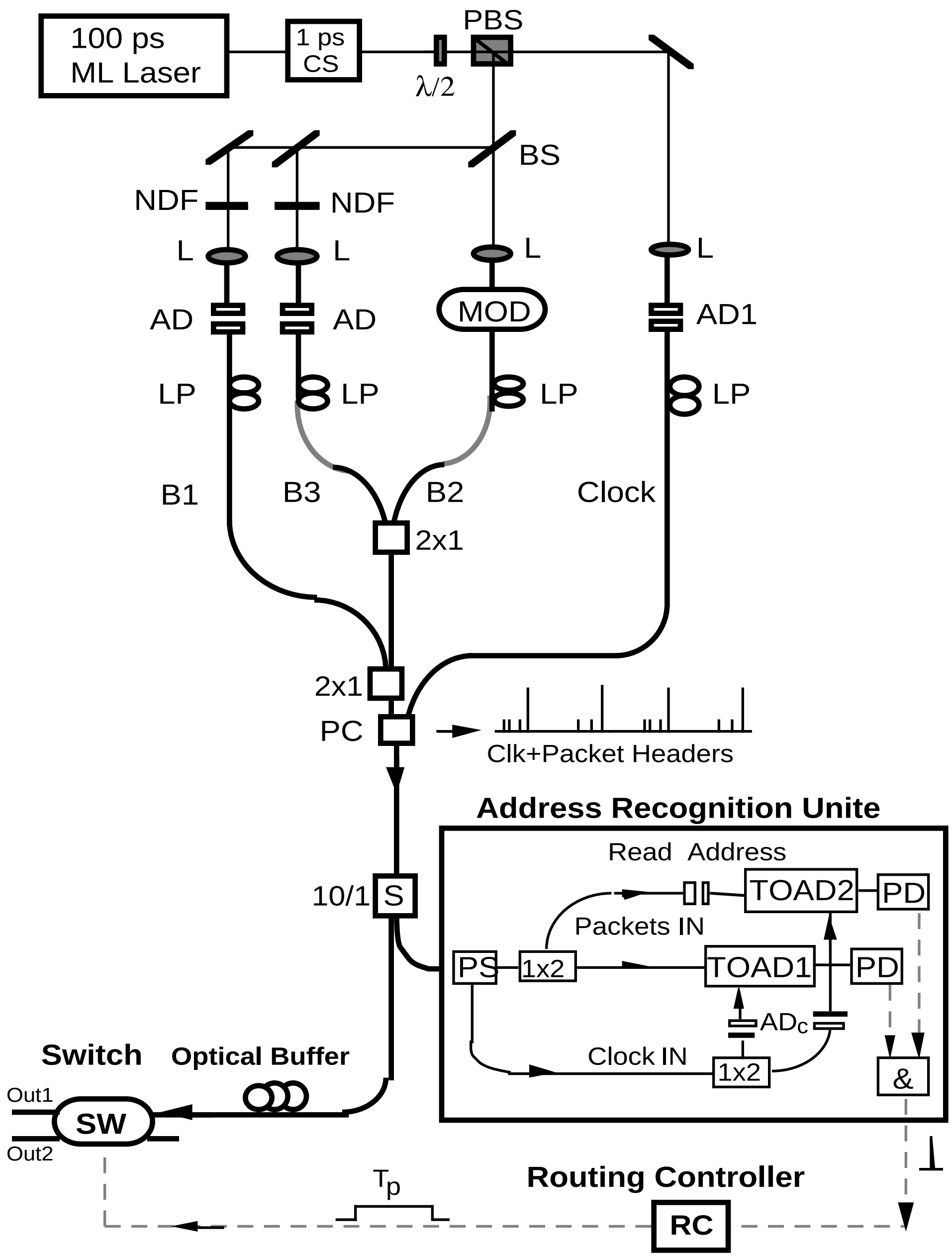

Fig. 3. Experimental setup.

switch to a cross or bar state. In this way packets "1110...0" with destination address "11" were removed from the network traffic(dropped) and exit from output port 2, while packets "1010...0" with destination address "10" passed through the switch SW and exit from output port 1. This is shown schematically in figures 5a, 6a. The experimental demonstration of all-optical packet address recognition, including packet drop, is shown in figures 5b and 6b.

Figure 4c is an oscilloscope photograph of the node input showing the multiplexed 100 MHz clock and two different packets "1110 . . . 0" and "1010 . . . 0". The clock is the highest intensity pulse. The two packets are composed of bits spaced 4 ps apart resulting in an aggregate bandwidth of 0.25 Tb/s. Because the temporal separation of these bits are too

#2225 - $10.00 US Received July 16, 1997; Revised August 28, 1997

small for the 1 GHz oscilloscope to distinguish, different packets appear as cumulative "double height" ("1010...0" bit sequence) and "triple height" ("1110...0" bit sequence) pulses.

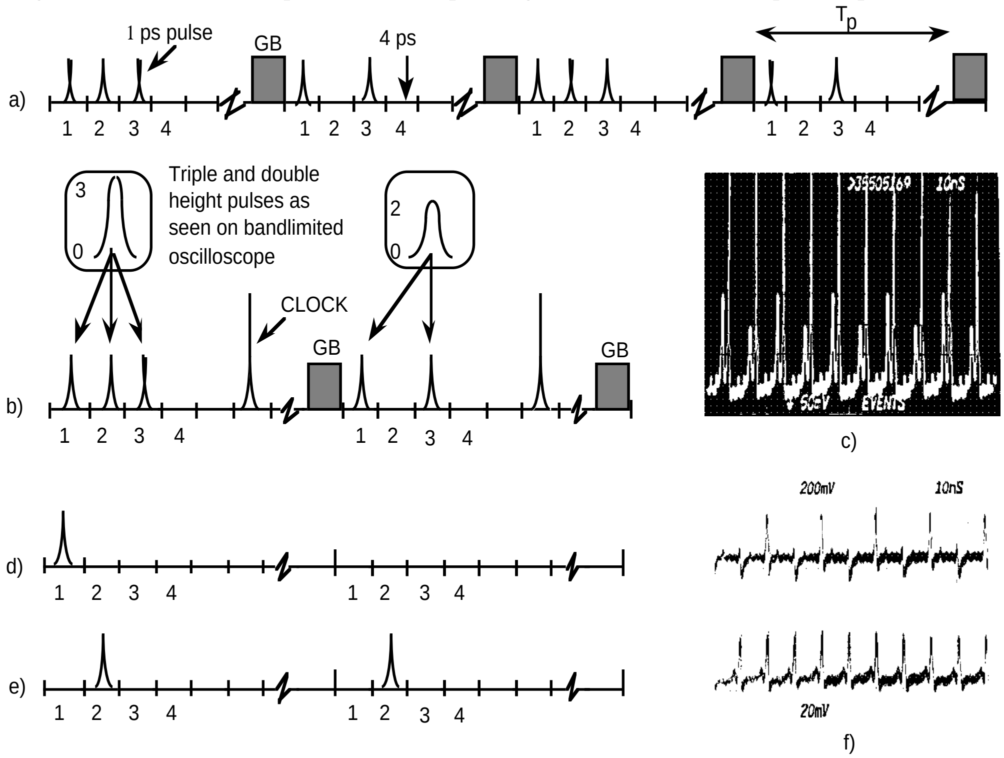

Fig. 4. Timing diagram. a) Two optically compressed packet headers "111" and "101"; b) Polarization multiplexed packets and clock; c) Oscilloscope trace of b); d) TOAD1 output after demultiplexig address bit 1; e) TOAD2 output after demultiplexing bit 2; f) Oscilloscope trace of d) and e).

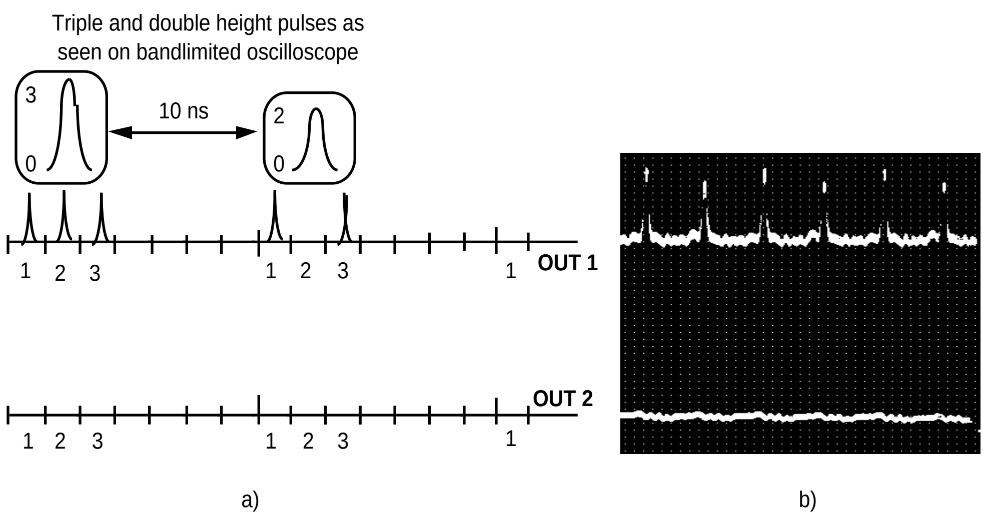

Fig. 5. Switch output - optical node is not receiving data: a) timing diagram - no packets at output port OUT 2, all packets exit at output port OUT 1; b) Experimental demonstration: oscilloscope photograph of both switch outputs as seen on the bandwidth limited oscilloscope (the different packets appear as cumulative "double height" (101 bit sequence) and "triple height" (111 bit sequence) pulses).

#2225 - $10.00 US Received July 16, 1997; Revised August 28, 1997

Figure 5b is an oscilloscope photograph of both outputs of the routing switch SW, when the node is not receiving data. In this case the address recognition unit, ARU, is set not to read the destination address of incoming optical packets. The routing switch SW is always in unswitched (bar) state, therefore all incoming packets “1110...0” and “1010...0” exit from output port 1. On bandwidth limited oscilloscope the different packets appear as cumulative double height and triple height pulses at the output of port 1, and no packets at the output of port 2. The upper trace shows the output port 1 and the lower trace output port2.

Figure 6b is an oscilloscope photograph showing outputs of the routing switch SW, where the packets destine for the node are removed from the network traffic by routing switch. In this case TOAD1 and TOAD2 have been synchronized to simultaneously demultiplex address bits 1and 2 from the packet header. In our experiment, bit 1 is always "1" and bit 2 is "1" or "0”. This way "1110...0" packets with node destination address “11” were removed (dropped) from the network traffic and exit from output port 2, while "1010...0" packets with address “10” stayed intact and exited from output port 1. Again, the different packets appear as cumulative triple height pulses at port 2, and double height pulses at port 1 with doubled spacing between packets at both output ports. The upper trace belongs to the output port 1 and the lower trace to output port 2.

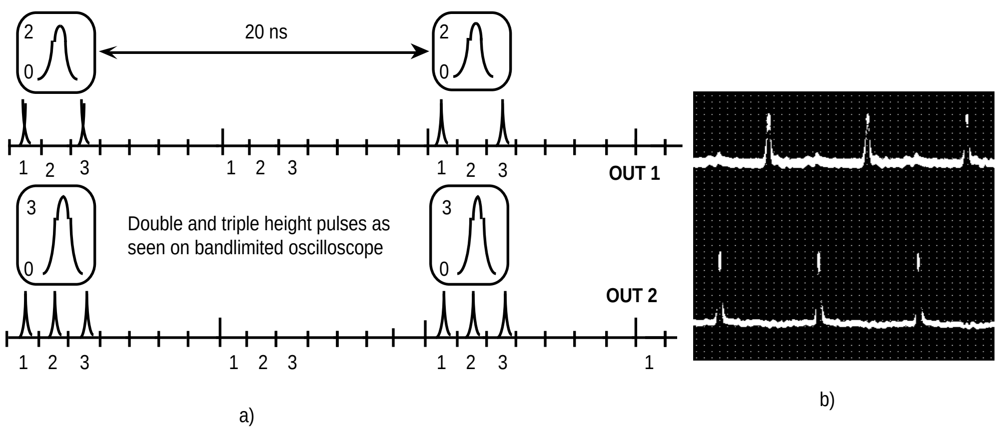

Fig. 6. Switch output - optical packets destine for the node are dropped/removed from the network traffic and exit at the switch output port OUT 2. a) timing diagram: packet "1110...0" destine for the node are removed from the network traffic and exit at the switch output port OUT 2; b) Experimental demonstration: oscilloscope photograph of both switch outputs as seen on the bandwidth limited oscilloscope (the different packets appear as cumulative "double height" (101 bit sequence) and "triple height" (111 bit sequence) pulses).

4. Conclusion

In this paper we report the demonstration of two bits all-optical address recognition and self-routing of packets for a case where the packet bit period is only 4 ps, corresponding to a 0.25 Tb/s bandwidth optical network. The TOADs are used to optically demultiplex two address bits from the packet header. Based on these bit values, the packets are routed through an electro-optic switch. Only those packets which are destined for the node are removed(dropped) from the network traffic. Crosstalk measurements of pseudo-random data in adjacent 4 ps-width time slots of the packet header, which is equivalent to routing errors, exhibit BER less than 10^{-9}, with strong jitter immunity.

#2225 - $10.00 US Received July 16, 1997; Revised August 28, 1997