Optimizing Pentacene Growth in Low-Voltage Organic Thin-Film Transistor Prepared by Dry Fabrication Techniques

S. Gupta[1], K. C. Chinnam[1], M. Zelzer[2], R. Ulijn[2], and H. Gleskova[1]
[1] Department of Electronic and Electrical Engineering, [2] Department of Pure and Applied Chemistry, University of Strathclyde, Glasgow, United Kingdom.

ABSTRACT

We have studied the effect of pentacene purity and evaporation rate on low-voltage organic thin-film transistors (OTFTs) prepared solely by dry fabrication techniques. The maximum field-effect mobility of 0.07 cm^2/Vs was achieved for the highest pentacene evaporation rate of 0.32 Å/s and four-time purified pentacene. Four-time purified pentacene also led to the lowest threshold voltage of -1.1 V and inverse subthreshold slope of ~100 mV/decade. In addition, pentacene surface was imaged using atomic force microscopy, and the transistor channel and contact resistances for various pentacene evaporation rates were extracted and compared to field-effect mobilities.

INTRODUCTION

To turn organic electronic circuits into viable technology platform, transistors require high field-effect mobility and low operating voltage. In addition, technology that can be adapted to roll-to-roll processing is desirable. Here, dry vacuum technologies provide an alternative path to wet printing of organic devices.

Organic thin-film transistors (OTFTs) have been demonstrated in display drivers [1], op-amps [2], and complementary inverters [3]. These circuits take advantage of low processing temperature typically below 180°C which allows their fabrication on a wide range of plastic substrates.

To date, several groups have achieved low voltage OTFTs with high-k aluminium oxide (AlO_x) and a self-assembled monolayer (SAM) based on phosphonic acids [4–7]. Our gate dielectric consists of thin AlO_x and n-octyl phosphonic acid. In contrast to previous research, AlO_x is prepared by UV/ozone oxidation of Al and alkyl-phosphonic acid is vacuum deposited.

Pentacene is the most studied p-type organic semiconductor. Jurchescu et al. [8] showed that impurities and defect states in pentacene lead to lower field-effect mobility. In addition, OTFT performance is dependent on the dielectric-semiconductor interface which is affected by preparation of gate dielectric [9–11], the growth of pentacene, and the channel thickness [12]. In this paper, we studied the effect of pentacene evaporation rate and purity on the performance of fully-dry, low-voltage OTFTs with total thickness of gate dielectric of ~ 20 nm.

EXPERIMENT

All p-channel transistors have a bottom-gate, top source-drain contacts structure as shown in figure 1. The TFTs were fabricated on Eagle 2000 glass in a Mini-Spectros vacuum deposition system (Kurt J. Lesker). Firstly, a 30-nm-thick Al gate line was thermally evaporated at a rate of 1 Å/s. Part of the gate electrode (away from the transistor island) was capped with 10-nm-thick gold to prevent its oxidation. To convert the surface of Al gate line into thin AlO_x, one hour

UV/ozone treatment was performed in UVOCS UV/ozone cleaner enclosed under a Hepa filter. To increase the thickness of AlO_x, six 15-Å-thick Al layers were sequentially evaporated and UV/ozone exposed for 60 minutes, leading to a total AlO_x thickness of 195 Å. Afterwards, a 'monolayer' of n-octyl phosphonic acid was evaporated leading to the total thickness of the gate dielectric of ~ 20 nm, capacitance of ~ 0.28 μF/cm^2, breakdown voltage in excess of 10 V and the gate leakage current density less than 1 x 10^{-7} A/cm^2 [13]. 50-nm-thick pentacene was evaporated in high vacuum (1.5 × 10^{-7} mBar). Two pentacene purities and six different pentacene evaporation rates were investigated. Three (Sigma-Aldrich) and four-time (in-house) purified pentacene was evaporated at rates of 0.02, 0.05, 0.08, 0.16, 0.24, and 0.32 Å/s. Finally, 50-nm-thick gold source and drain contacts were evaporated at a rate of 3 Å/s. Corresponding capacitor structures were fabricated alongside the TFTs. All fabrication steps were completed by using shadow masks. The transistors with channel lengths of 30, 50, 70, and 90 μm and channel width of 1000 μm were fabricated.

Transistor measurement and parameter extraction

Gate dielectric capacitance and the transistor characteristics were measured with Agilent B1500A semiconductor device analyzer. The drain-to-source (I_{DS}) and gate-to-source (I_{GS}) currents of an OTFT in the linear (V_{DS} = -0.1 V) and saturation regimes (V_{DS} = -3 V) as functions of the gate-to-source voltage (V_{GS}) are shown in figure 2. The field-effect mobility μ and the threshold voltage V_{th} were calculated from an ideal MOSFET current-voltage relation in the saturation regime:

$$I_{DS} = \mu C \frac{W}{2L}\left(V_{GS} - V_{th}\right)^2 \quad (1)$$

where C is the capacitance per unit area of the gate dielectric, L the channel length and W the channel width. The mobility is extracted from the slope of the linear fit of square root of I_{DS} versus V_{GS} and the intercept on the voltage axis corresponds to the threshold voltage. The subthreshold slope S is calculated from the exponential slope of I_{DS} versus V_{GS}.

In the linear regime, the total resistance $R_T = V_{DS}/I_{DS}$. This resistance is divided between the channel resistance (R_{ch}) and the contact resistance (R_c) of the source-drain contacts. To extract R_{ch} and R_c, we employ a classical transmission-line method (C-TLM) [14] and modified transmission-line method (M-TLM) [15], respectively. In C-TLM, $R_T.W$ is plotted against L while in M-TLM, $R_T.(W/L)$ is plotted against $(1/L)$. C-TLM and M-TLM follow these mathematical expressions, respectively:

$$R_T W = \frac{L}{\mu C\left(V_{GS} - V_{th}\right)} + R_C W \quad (2)$$

$$R_T \frac{W}{L} = \frac{1}{\mu C\left(V_{GS} - V_{th}\right)} + R_C \frac{W}{L} \quad (3)$$

hence, the slope of C-TLM divided by W corresponds to the channel resistance per unit channel length R_{ch}/L (in Ω/μm) and the slope of M-TLM divided by W to the contact resistance R_c (in Ω).

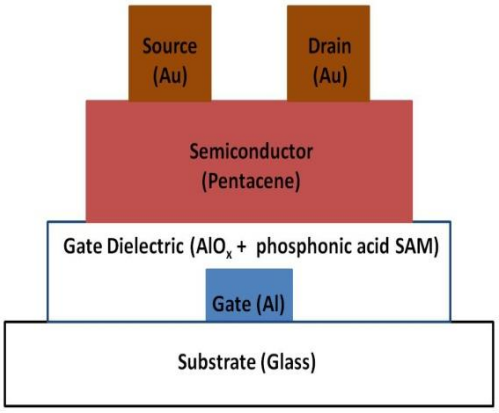

Figure 1. Transistor cross-section.

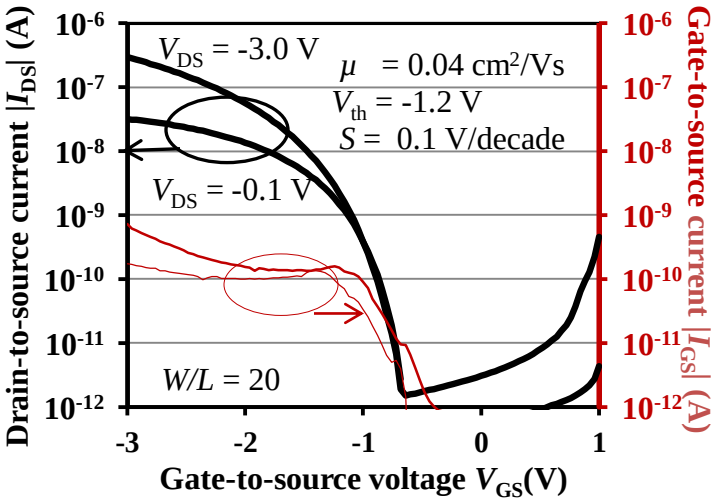

Figure 2. Transfer characteristics of OTFT with four-time purified pentacene.

RESULTS

Figure 3(a) shows the mean mobilities and the standard deviations obtained for transistors with various channel lengths. The field-effect mobility is increasing with increasing evaporation rate for four-time purified pentacene. The field-effect mobility of the transistors with three-time purified pentacene exhibits a maximum at evaporation rate of ~0.24 Å/s. Four-time purified pentacene resulted in higher mobility if compared to three-time purified pentacene. The average threshold voltage for all pentacene purities is shown in figure 3(b). The variation in the threshold voltage with pentacene evaporation rate and purity is much smaller than that for the field-effect mobility. Since the primary factor affecting the threshold voltage is the gate dielectric, which is the same in all transistors, this small variation is expected.

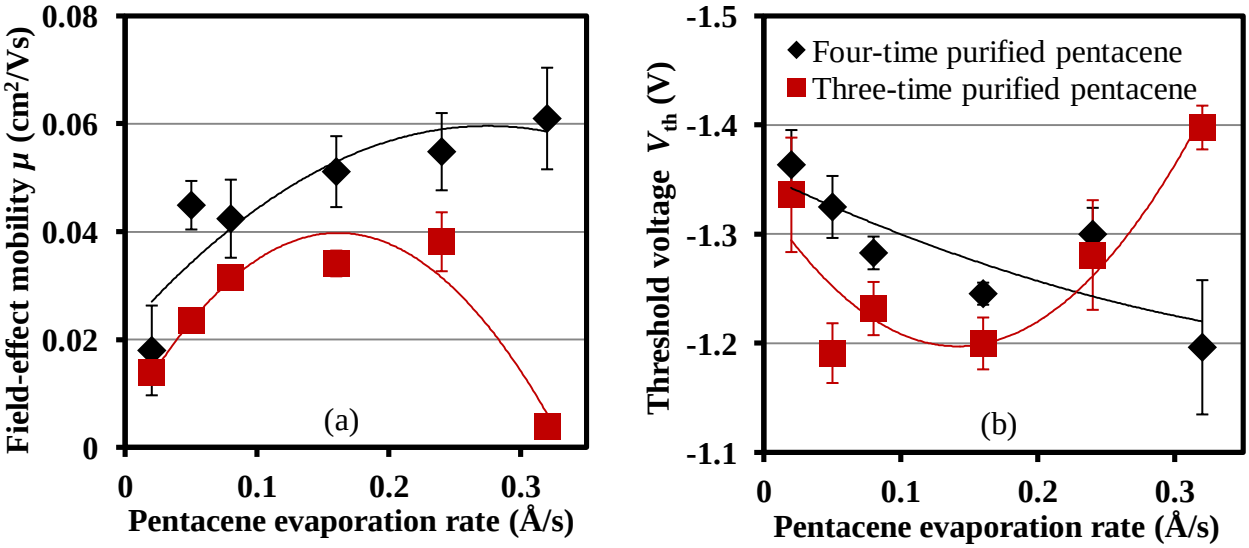

Figure 3. Field-effect mobility (a) and threshold voltage (b) as functions of pentacene purity and evaporation rate. The solid lines are guides for the eye only.

Atomic force microscopy (AFM) height images of four-time purified pentacene at evaporation rates of 0.02, 0.24, and 0.32 Å/s are shown in figures 4(a), (b), and (c), respectively. It is observed that the pentacene grains contain fewer sub-grains and become more tightly connected at higher evaporation rates. At the same time, when the pentacene evaporation rate rises from 0.02 Å/s to 0.32 Å/s, the field-effect mobility increases by a factor of three.

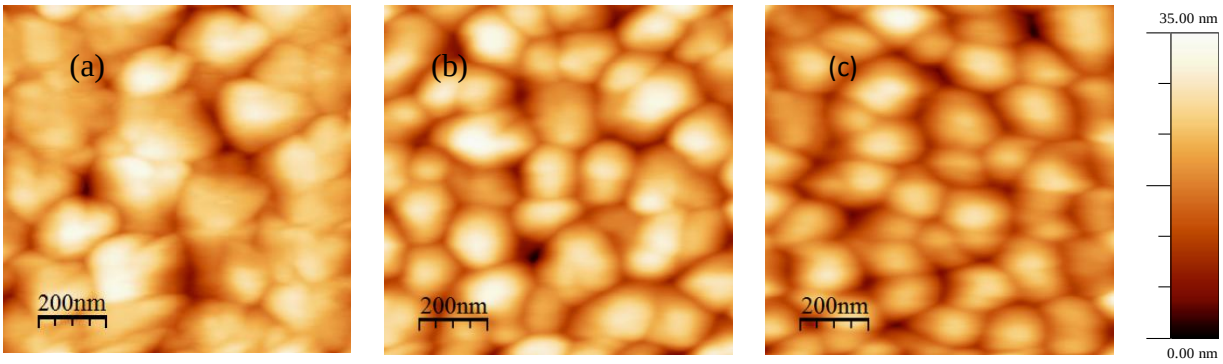

Figure 4. AFM images of four-time purified pentacene deposited at 0.02 (a), 0.24 (b), and 0.32 (c) Å/s.

Figures 5(a) and 5(b) depict the contact and channel resistances of OTFTs with three and four-time purified pentacene, respectively. R_{ch} is smaller for OTFTs with four-time purified pentacene if compared to those with three-time purified pentacene and decreases with increasing pentacene evaporation rate. Also, both R_c and R_{ch} decrease with increasing V_{GS}.

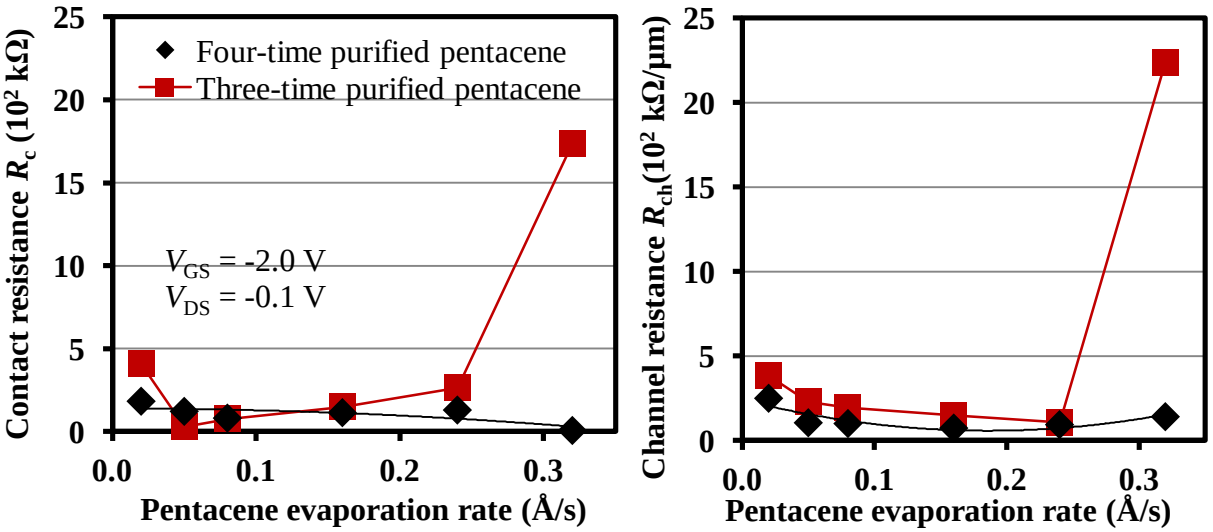

Figure 5. Contact (a) and channel resistance per unit channel length (b) of OTFTs with three and four-time purified pentacene.

DISCUSSION

The OTFTs containing four-time purified pentacene exhibit the highest field-effect mobility of 0.07 cm^2/Vs and the lowest threshold voltage of -1.1 V at the highest pentacene

evaporation rate of 0.32 Å/s. AFM images of four-time purified pentacene deposited at different rates reveal tighter connection between grains and less sub-grain structure for higher evaporation rates, even though the actual grain size becomes smaller. According to Shtein *et al.* [10], the electrical conductivity increases with improved physical contact between the pentacene grains. Knipp *et al.* [16] also showed that the pentacene grain size is not a unique indicator of electronic properties. In their OTFTs with octadecyltrichlorosilane (OTS) SAM and pentacene, they observed higher field-effect mobility in transistors with SAM even though the inclusion of SAM led to pentacene with smaller grain size [9]. Pentacene with higher purity also improved the field-effect mobility. Our field-effect mobilities and AFM results agree with these previous observations. They are also supported by the results of the contact and channel resistances shown in figures 5(a) and 5(b). The larger total resistance values coincide with lower field-effect mobilities.

The inverse subthreshold slope of ~100 mV/decade for four-time purified pentacene is similar to that achieved by Halik *et al.* [17] and Klauk *et al.* [14]. This value indicates low trap density at the semiconductor-dielectric interface when more purified pentacene is used. Also, the channel and contact resistances of OTFTs with four-time purified pentacene are comparable to Klauk *et al.* [14]. The channel resistance becomes lower at higher evaporation rates, indicating better pentacene polycrystalline morphology and possibly improved dielectric-semiconductor interface.

CONCLUSION

We have studied the effect of pentacene purity and evaporation rate on OTFTs prepared by dry fabrication techniques. Higher pentacene purity leads to OTFTs with improved field-effect mobility. The maximum mobility of 0.07 cm^2/Vs was achieved at the highest pentacene evaporation rate of 0.32 Å/s when using four-time purified pentacene. The lowest threshold voltage of ~ -1.1 V and subthreshold slopes of ~100 mV/decade were also obtained for OTFTs with four-time purified pentacene. The AFM results of four-time purified pentacene indicate that although the higher evaporation rate leads to smaller pentacene grain size, the grains exhibit less sub-grain structure and tighter packing. This is in agreement with results published by others. In addition, we observe that lower OTFT contact and channel resistances coincide with higher field-effect mobility.

ACKNOWLEDGEMENTS

Authors thank the School of Engineering of the University of Glasgow for the transistor fabrication support. They also thank G. Brown for help with white light interferometry. This research is supported by Glasgow Research Partnership in Engineering. S. Gupta is a recipient of Scottish Overseas Research Award and University Postgraduate Scholarship.

REFERENCES

1. V. Vaidya, S. Soggs, J. Kim, A. Haldi, J. N. Haddock, B. Kippelen, and D. M. Wilson, IEEE Transactions on Circuit and Systems **55** (5), 1177-1184 (2008).
2. A. Dey, A. Avendanno, S. Venugopal, D. R. Allee, M. Quevedo, and B. Gnade, IEEE Electron Device Letters **32** (5), 650-652 (2011).

3. J. B. Kim, C. Fuentes-Hernandez, D. K. Hwang, W. J. Potscavage Jr., H. Cheun, and B. Kippelen, Organic Electronics **12** (1), 45-50 (2011).
4. A. Jedaa, M. Burkhardt, U. Zschieschang, H. Klauk, D. Habich, G. Schmid, and M. Halik, Organic Electronics **10** (8), 1442-1447 (2009).
5. H. Klauk, U. Zschieschang, J. Pflaum, and M. Halik, Nature **445** (7129), 745-748 (2007).
6. H. Ma, O. Acton, G. Ting, J. W. Ka, H. Yip, N. Tucker, R. Schofield, and A. K. –Y. Jen, Applied Physics Letters **92** (11), 113303 (2008).
7. K. Fukuda, T. Hamamoto, T. Yokota, T. Sekitani, U. Zschieschang, H. Klauk, and T. Someya, Applied Physics Letters **95** (20), 203301 (2009).
8. O. D. Jurchescu, J. Baas, and T. T. M. Palstra, Applied Physics Letters **84** (16), 3061-3063 (2004).
9. D. Knipp, R. A. Street, A. Völkel, and J. Ho, Journal of Applied Physics **93** (1), 347-355 (2003).
10. M. Shtein, J. Mapel, J. B. Benziger, and S. R. Forrest, Applied Physics Letters **81** (2), 268-270 (2002).
11. H. Klauk, M. Halik, U. Zschieschang, G. Schmid, W. Radik, and W. Weber, Journal of Applied Physics **92** (9), 5259-5263 (2002).
12. S. Mun, J. -M. Choi, K. H. Lee, and S. Im, Applied Physics Letters **93** (23), 233301 (2008).
13. K. C. Chinnam, S. Gupta, and H. Gleskova, Journal of Non-Crystalline Solids (DOI: 10.1016/j.jnoncrysol.2012.01.016) (in press)
14. H. Klauk, U. Zschieschang, and M. Halik, Journal of Applied Physics **102** (7), 074514 (2007).
15. Y. Xu, R. Gwoziecki, I. Chartier, R. Coppard, F. Balestra, and G. Ghibaudo, Applied Physics Letters **97** (6), 063302 (2010).
16. D. Knipp, R. A. Street, and A. R. Völkel, Applied Physics Letters **82** (22), 3907-3909 (2003).
17. M. Halik, H. Klauk, U. Zschieschang, G. Schmid, C. Dehm, M. Schütz, S. Maisch, F. Effenberger, M. Brunnbauer, and F. Stellacci, Nature **431** (7011), 963-966 (2004).