Electro-thermal Analysis of Power Converter Components in Low-Voltage DC Microgrids for Optimal Protection System Design

Michal Sztykiel, Steven Fletcher, Patrick Norman, Stuart Galloway and Graeme Burt

Abstract-- **Bidirectional power converters are considered to be key elements in interfacing the low voltage dc microgrid with an ac grid. However to date there has been no clear procedure to determine the maximum permissible fault isolation periods of the power converter components against the dc faults. To tackle this problem, this paper presents an electro-thermal analysis of the main elements of a converter: ac inductors, dc capacitors and semiconductors. In doing this, the paper provides a methodology for quantifying fault protection requirements for power converter components in future dc microgrids. The analysis is performed through simulations during normal and fault conditions of a low voltage dc microgrid. The paper develops dynamic electro-thermal models of components based on the design and detailed specification from manufacturer datasheets. The simulations show the impact of different protection system operating speeds on the required converter rating for the studied conditions. This is then translated into actual cost of converter equipment. In this manner, the results can be used to determine the required fault protection operating requirements, coordinated with cost penalties for uprating the converter components.**

Index Terms-- **Microgrid, DC fault current, AC-DC power conversion, thermal design, power semiconductor diode switches, thermal stress, fault protection requirements.**

NOMENCLATURE

C_{cap}	nominal capacitance of dc capacitor
c_{core}	core specific heat
C_L	cable shunt capacitance
c_s	specific heat of the heatsink
C_{th}	thermal capacitance
$C_{th(core)}$	thermal capacitance, windings to ambient
$C_{th(j-c)}$	thermal capacitance, junction to case
$C_{th(s-a)}$	thermal capacitance, heatsink to ambient
$C_{th(winding)}$	thermal capacitance, core to ambient
$c_{winding}$	windings specific heat
f_{sw}	switching frequency
i_{latch}	current level at which latch-up may occur
I_N	nominal current (RMS)
$I_{limit(\%)}$	current limiting level made by a fault current limiter
L_{busbar}	stray inductance of dc busbar
L_{cap}	equivalent series inductance of dc capacitor
L_L	cable series inductance
L_{sw}	stray inductance of a semiconductor
m_s	mass of the heatsink
P_{AC}	nominal active power
P_d	instantaneous power losses
$P_{d,N}$	nominal power losses
$R_{battery}$	parasitic resistance of a battery
R_{cap}	equivalent series resistance of dc capacitor
R_L	cable series resistance
R_{load}	load resistance
R_{sw}	on-state resistance of a semiconductor
R_{th}	thermal resistance
$R_{th(c-s)}$	thermal resistance, case to heatsink
$R_{th(j-c)}$	thermal resistance, junction to case
$R_{th(s-a)}$	thermal resistance, heatsink to ambient
T_{amb}	ambient temperature
t_{break}	fault breaking time
$T_{C,N}$	nominal (working) case temperature
$T_{hs,max}$	maximum allowed hot-spot temperature
$T_{hs,N}$	nominal (working) hot-spot temperature
T_j	junction temperature
$T_{j,max}$	maximum allowed junction temperature
$T_{j,N}$	nominal (working) junction temperature
V_{core}	volume of core
V_{total}	total volume of ac inductor
$V_{winding}$	volume of windings
$Z_{th(j-c)}$	transient thermal impedance, junction to case
δ_{core}	core density
$\delta_{winding}$	windings density
τ_{RC}	thermal time constant

I. INTRODUCTION

A micro-grid refers to the integration of distributed generation into an isolated and fully functional power system [1]. Micro-grids are designed to flexibly provide a continuous power supply within its range, independent to the interconnected remote supplies. As a result, micro-grid systems are especially attractive to emergency (hospitals, data centers) and mobile end-users (aircraft, traction, vehicles).

The selection of an optimal low voltage micro-grid architecture is based on the types of distributed resources, network and communication systems [2]. Power electronics converters play a key role here, as they interconnect sources with a network to provide an interface for a synchronized and controlled power supply to end-users.

In order to minimize cost, losses and volume, it has been

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proposed that future low voltage micro-grid architectures with a variety of distributed resources will be based on the dc distributed networks [3]. Compared to ac networks, dc micro-grids may provide a simpler and more efficient interface between sources and loads by reducing the number of consecutive power conversion stages and consequently the number of required power converter units [4].

Electrical network protection is an important aspect related to the economic development of future dc architectures. The selection of commercially available protection devices needs to be well coordinated with the selection of the peak rating of network components. In this manner, an optimal compromise can be achieved between reliable fault protection and minimum cost.

On the contrary to ac networks, the appearance of short circuit faults in dc microgrids results in rapid rise of excessive fault current [5]. This has a significant impact on the dc system performance and protection methods of the power electronics converters. According to [1], it is possible to isolate the dc fault with the usage of commercial protection devices, such as fuses and circuit breakers to protect batteries and loads. However, the relative sensitivity of power converters can impose strict protection requirements, as this paper will highlight, hence limiting the use of conventional circuit breaking technologies [6-7].

IEC 61660-1 standard [9] defines methods and empirical formulas for estimating the dc short circuit currents. This provides a generally applicable method of calculation, which produces results of sufficient accuracy on the conservative side for the given application. This allows the calculation of fault current contributions coming from each individual source i.e. lead-acid battery, dc capacitor, etc. Based on the determined dc fault current levels, the IEC describes the procedure to estimate mechanical and thermal effects on rigid conductors e.g. cables and bus bars, which can be used in identifying protection system requirements.

However, the dc microgrids consist not only of the rigid conductors as shown in Fig. 1, but also of power electronics converters built from their own internal components: filters and semiconductors. As a consequence, identification of the

protection system requirements should also include the impact made by the excessive fault current on converter components. Calculations of fault current using the IEC 61660-1 standard can also lead to some inaccuracies where active converters are included in the network [10].

The empirical formulas used to calculate dc short circuit currents flowing through the converter individual components have already been formulated in Laplace domain and described in [11]. However the use of formulas to accurately represent fault current is still challenging in closely coupled, parallel branch networks as analytic expressions can become large and complex [12]. Therefore network simulation remains a key part of the system analysis [13].

Beyond fault current calculation, the natural next step is to develop a technique, which can be used to estimate thermal effects on the converter elements and propose a design rationale for its fault protection system.

This paper presents such a method, which identifies the protection system operating requirements by estimating the relationship between the required fault clearing time and the converter components' ratings.

This paper also describes the development of new transient electro-thermal models of electrical components, which have not been covered in [9] along with the procedure to estimate the thermal effects of faults. As a result, the electro-thermal models of the components presented in this paper can be considered and challenged as a supplement to the models of the rigid components and used to determine the actual thermal effects on power converters during faults.

The fault analysis is based on the estimated transient temperature rise for the given ratings of the power converter components, which are subjected to the thermal stress during dc short-circuit faults. The obtained temperature variations are used to identify the required converter protection system operating times over a range of working temperatures.

Finally, the cost of the components is estimated for the range of working temperatures and operating times of the protection system so that dc fault protection requirements can be directly associated with an actual cost of the power converter components.
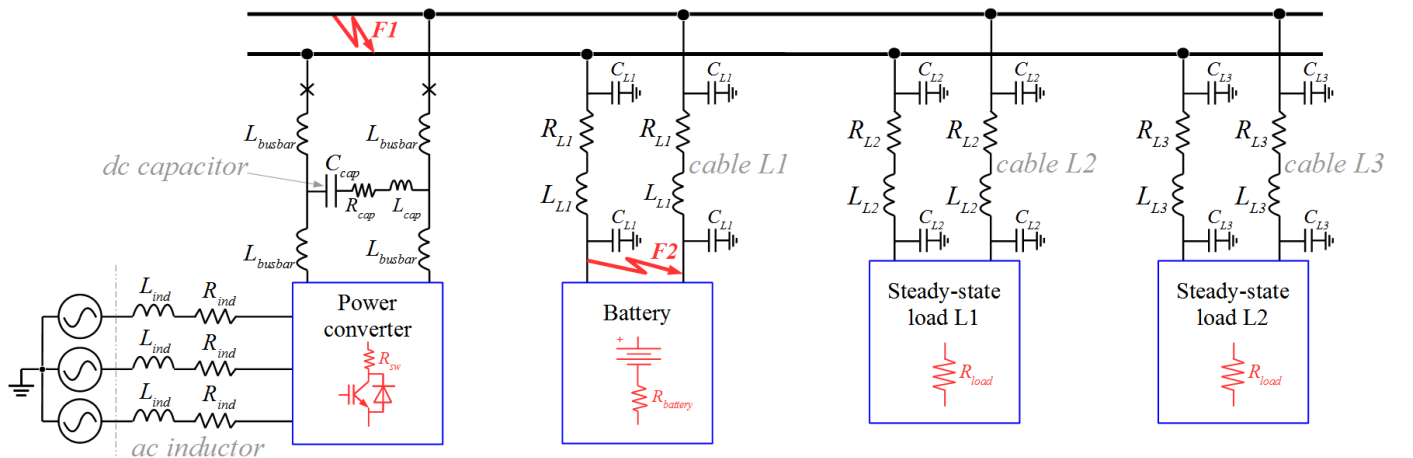

Fig. 1. Detailed network representation of the modelled low voltage dc microgrid.

II. Power Converter Design for LVDC Micro-grids

A. Low Voltage DC Micro-Grid

Fig. 1 illustrates how a low voltage dc micro-grid may incorporate dc or ac source types. The network in Fig. 1, which is based on a design first described in [1], is used as the platform for the analysis presented within this paper. It includes two dc loads: L1 and L2. The loads are supplied by an ac source, which represents a large electrical machine or an interconnected power system capable of providing stiff voltage characteristics at the point of common coupling (PCC).

During emergency conditions, a micro-grid can be directly supplied from the battery interconnected to the dc distribution bus. Within Fig 1, the main point of interest for this paper is the grid connected ac-dc converter. This will be the sub-system upon which the thermal stress analysis will be conducted.

B. Power Converter Topology

The examined ac-dc rectifier circuitry from Fig. 2 represents a six-switch voltage source converter, which is commonly used for low voltage applications [14].
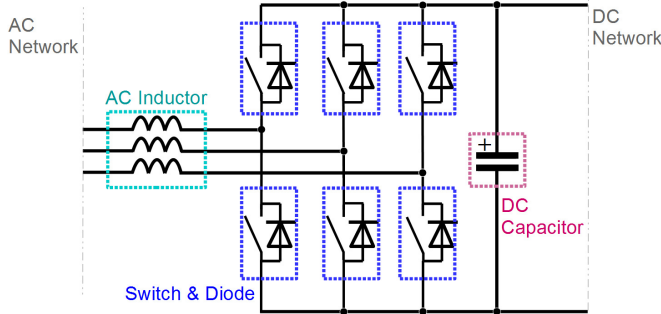

Fig. 2. Main components of six-switch power converter

The presented topology allows decoupling of the dc and ac sides of the electrical system through the common dc link, which simplifies control and switching algorithms.

C. Power Converter Components

As with the six-switch converter shown in Fig. 2, other existing voltage source converter topologies are made of switches, diodes, ac inductors and dc capacitors.

The dc capacitor is used to minimize the dc voltage ripple, whereas the ac inductor is used to minimize ac current ripple that appears due to the switching operation. Semiconductor switches are used to control the power flow between ac and dc sides, whereas the diodes rectify input ac power coming from the source.

Each component is vulnerable to two forms of thermal stress, which the paper will classify as:

1) *Long-term*: During normal operation, where the temperature rise is mainly influenced by ambient conditions, normal system load and the cooling system.

2) *Short-term*: During fault operation, where the temperature rise is mainly influenced by fault characteristics and fault period.

The components need to be rated both against normal and fault conditions in order to perform reliable operation provided with minimum cost and size penalties.

III. Failure Characteristics of Power Converter Components

A. Diodes and Switches

The most common failure mode associated with overheating in semiconductors is bond-wire lift-off [14].

The temperature limit is dictated by the melting temperature, characterized by either the melting point of the semiconductor's mold compound or solder joint. The lower of the two melting points dictates the semiconductor's maximum junction temperature [15-16]. Many commercially available silicon-based high power devices allow operation at junction temperatures up to $T_{j,max} = 150\ ^0C$.

The semiconductor switches can be protected against overheating by a block-mode function. This can be initiated using gate driver control circuitry with integrated over-temperature protection. Fig. 3 illustrates an example sensing circuit which utilizes diodes as temperature sensors [17].

While the switches can be protected with a block-mode during dc short circuit faults, there is always a risk of latch-up when device carries a current substantially higher than rated. A latch-up is a failure mode where the switch can no longer be turned off by the gate driver and remains in on-state condition until its rupture. In order to avoid having a latch-up, a soft turn-off switching is required with increased gate resistance. A risk of latch-up can be also minimized by optimizing the doping levels and geometries of the alternating layers within the switch through manufacturing process.
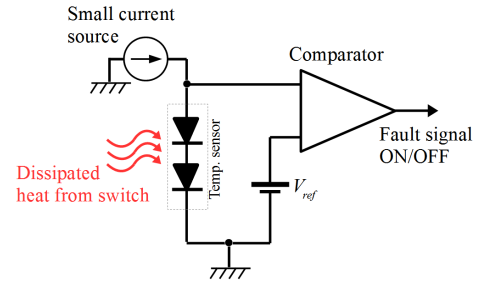

Fig. 3. Sense circuit for over-temperature protection with diode temp. sensors

In case of anti-parallel diodes, unidirectional currents will continue to flow until the converter becomes isolated from the network by the protection system.

B. AC Inductor

In ac inductor designs, the applied winding insulation materials dictate the maximum permissible hot spot temperature rise. Permissible temperature limits are assigned in accordance with IEC 61558 [18], which varies with the type of insulation system used by manufacturer.

For transient processes, transient temperature rise *ΔT* can be characterized by the exponential law defined by the thermal time constant of the component [19]. The same time constant defines the cooling behavior of the component. Over-temperature protection is achieved by isolating or clearing the

fault before the hot-spot temperature exceeds maximum permissible limit defined in [18].

C. DC Capacitor

Under dc fault conditions, stored electrical energy within the dc capacitor is rapidly released and transformed into heat.

Rapid capacitor discharge under the fault conditions results in a characteristic pulse current flow through the capacitor, which can be either aperiodic or damped oscillatory [20].

For thermal analysis, capacitor manufacturers provide maximum hot-spot temperature, thermal resistance and thermal time constant. The thermal time constant can be used to characterize the temperature rise during transient conditions.

Over-temperature short-circuit protection for dc capacitors and semiconductor diodes relies on physical fault isolation (e.g. with the usage of high-speed dc fuses [21]).

IV. DYNAMIC ELECTRO-THERMAL MODELING

This paper investigates the thermal impact of the short-circuit fault currents using dynamic temperature estimation models. These models measure and register the transient temperature rise during the fault period.

A. Diodes and Switches

The developed temperature-dependent electro-thermal model of a semiconductor calculates the transient temperature rise based on the estimated instantaneous power losses from the output current $i(t)$, voltage $v(t)$, temperature $T_{j(t)}$ and datasheet parameters. Fig. 4 illustrates the top-level flow chart of the developed device electro-thermal model. This proposed power loss modelling approach is consistent with that presented in [22], which is a commonly accepted method for loss evaluation of power semiconductor devices.
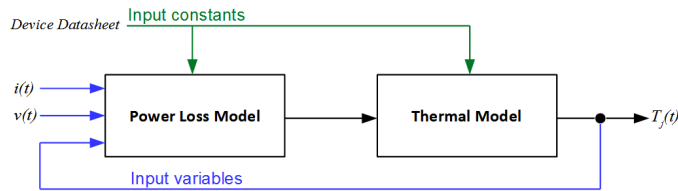
Fig. 4. Top-level flow chart used to estimate junction temperatures.

The Matlab/Simulink [11] implementation of a developed simulation-based IGBT loss model [23] is shown in Fig. 5. Three-dimensional look-up tables are used to determine the dissipated energy values based on the device characterization in manufacturer datasheets.

Loss models of the diodes are of similar design. However, they do not include losses generated during the turn-on, which are considered negligible and are normally neglected [24].

The thermal model of a single device indicates the junction temperature rate of rise $\Delta T(t)$, when the device is subjected to excessive fault current. Fig. 6 illustrates the developed model, in which the thermal impedance from junction to ambient is modelled as a six-layer Foster RC network [25]. Such a network allows accurate estimation of the temperature rise between junction and ambient [26].
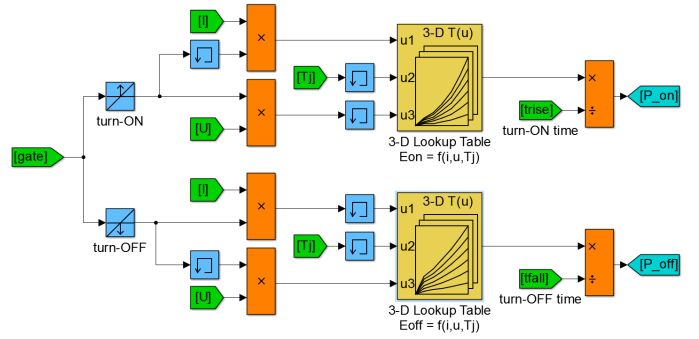
Fig. 5. Matlab/Simulink model for semiconductors switching loss calculation

The thermal resistance R_{th} will determine the steady state value of junction temperature, and the thermal constant τ_{RC}, which can be calculated from

$$\tau_{RC} = R_{th} \cdot C_{th} \quad , \tag{1}$$

(where C_{th} is the thermal capacitance and is defined later) will dictate the dynamic change of the junction temperature T_j. Ambient temperature T_{amb} is assumed constant during the fault period due to its relatively short duration.
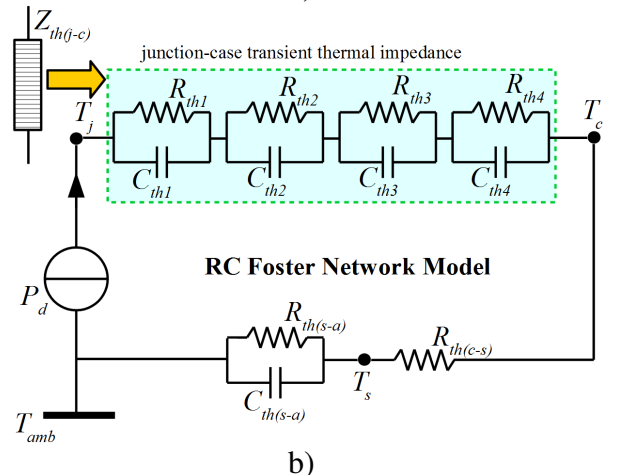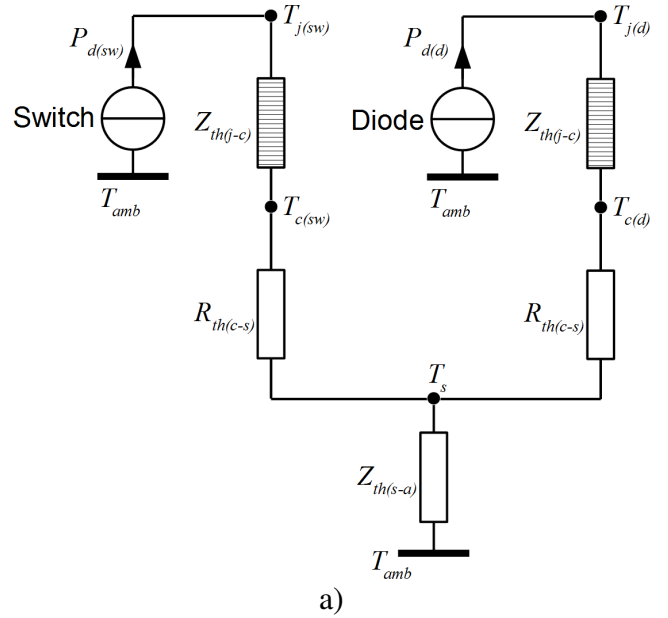
Fig. 6. a) Thermal model of switch and diode used for junction temperature estimation; b) RC Foster network representation C_{th}

The parameter values of semiconductor junction-case transient thermal impedance $Z_{th(j-c)}$ can be found directly from the manufacturer datasheet.

The minimum required thermal resistance of the heatsink $R_{th(s-a)}$ can be calculated from (2) based on the device nominal power losses $P_{d,N}$

$$R_{th(s-a)} = \frac{(T_{C,N} - T_{amb})}{P_{d,N}} - R_{th(c-s)} \tag{2}$$

$$C_{th(s-a)} = m_s \cdot c_s \tag{3}$$

The thermal capacitance $C_{th(s-a)}$ can be approximated from (3), where m_s is mass and c_s is the specific heat of the selected heatsink material. Parameter values for (2, 3) have been listed in Table I, which provides the specification of the selected heatsink from the manufacturer's datasheet. This and subsequent tables also indicate the price of components. This is the advertised price at the respective reference [27]-[31] at the time of writing and is used for cost estimations in later sections of the paper.

TABLE I
HEATSINK SPECIFICATION: ABL COMPONENTS 177AB2000B [27]

Manufacturer	ABL Components
Heatsink material	Aluminum
Working case temp. $T_{C,N}$ [C]	105
Max. thermal resistance $R_{th(s-a)}$ [K/W]	0.07
Thermal capacitance $C_{th(s-a)}$ [W·s/K]	4.31e3
Weight m_s [kg]	5
Specific heat c_s [J/kg·K]	910
Price [$] / Size [dm³]	100 / 4.98

The transient temperature rise $\Delta T(t)$ is estimated from

$$\Delta T(t) = P_d(t) \cdot \sum_{i=1}^{6} R_{th(i)} \cdot \left(1 - e^{-t/R_{th(i)} \cdot C_{th(i)}}\right) \tag{4}$$

Table II lists input values from the semiconductor device manufacturer's datasheet used to model the transient temperature rise.

TABLE II
SWITCH AND DIODE SPECIFICATION: INFINEON BSM 150 GB 60 DLC [28]

Parameter		Value	
Nominal power losses [kW]	$P_{d,N}$	0.68	
Nominal junction temp.	$T_{j,N}$	125	
Maximum junction temp. [°C]	$T_{j,max}$	150	
Ambient temp. [°C]	T_{amb}	40	
Case-sink thermal resistance [K/W]	$R_{th(c-s)}$	0.02	
Price [$] / Size [dm³]		80 / 0.1	
Switch thermal impedance [K·s/W] RC layer factors	$Z_{th(j-c)}$	$R_{th1} = 8.9$ $R_{th2} = 110.0$ $R_{th3} = 74.0$ $R_{th4} = 17.0$	$C_{th1} = 2.0e-4$ $C_{th2} = 2.2e-4$ $C_{th3} = 8.8e-4$ $C_{th4} = 3.9e-2$
Diode thermal impedance [K·s/W] RC layer factors	$Z_{th(j-c)}$	$R_{th1} = 141.0$ $R_{th2} = 135.2$ $R_{th3} = 84.9$ $R_{th4} = 38.9$	$C_{th1} = 3.4e-4$ $C_{th2} = 1.2e-4$ $C_{th3} = 1.3e-3$ $C_{th4} = 2.3e-4$

B. AC Inductor and DC Capacitor

The transient temperature rise in inductive or capacitive components can be approximated by an equivalent one-layer Foster RC network presented in Fig. 7.
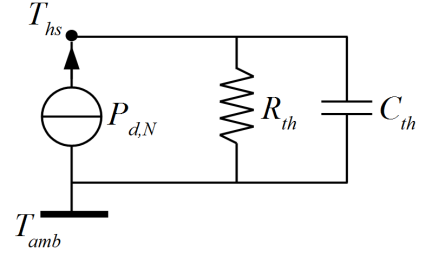

Fig. 7. Thermal model used for hot-spot temperature estimation in ac inductors and dc capacitors

For an inductor design, a classical thermal model [19] can be used to calculate the steady-state equivalent thermal resistance of an inductor R_{th} as a function of the dissipated core (magnetic) and winding (conduction) losses P_{losses}

$$R_{th} = \frac{\Delta T}{P_{losses}}, \tag{5}$$

where ΔT represents the temperature rise from ambient to insulation layer.

The total thermal capacitance C_{th} of the inductor can be approximated from [19]

$$C_{th} \cong C_{th(winding)} + C_{th(core)} = c_{winding} \cdot \delta_{winding} \cdot V_{winding} + c_{core} \cdot \delta_{core} \cdot V_{core} \tag{6}$$

In accordance with Table III, calculated values of specific heat capacitances ($c \cdot \delta$) for the winding and for the magnetic core materials are close to each other.

TABLE III
PARAMETERS OF THERMAL MODEL FOR AC INDUCTOR [29]

Manufacturer	MTE
Core material (3.1% silicon content)	CRGO Silicon Steel M-6
Core losses [W/kg]	1.1
Windings material	Copper
Core specific heat c_{core} [J/kg·K]	460
Windings specific heat $c_{winding}$ [J/kg·K]	383
Core density δ_{core} [kg/m³]	7417
Windings density $\delta_{winding}$ [kg/m³]	8954

In general, the thermal capacitance C_{th} can be determined by the total volume of inductor V_{total}.

$$V_{total} = V_{winding} + V_{core} \tag{7}$$

For capacitor designs, manufacturers typically provide the thermal time constant, the value of which can be used to calculate C_{th} from (1) based on the previously calculated thermal resistance R_{th}

$$R_{th} = \frac{\Delta T}{P_{d,N}} = \frac{T_{hs,N} - T_{amb}}{P_{d,N}} \tag{8}$$

where ΔT is the steady temperature rise between surface $T_{hs,N}$ and ambient T_{amb}.

With known RC thermal network constants, the transient temperature rise $\Delta T(t)$ can be estimated from [19]

$$\Delta T(t) = P_d(t) \cdot R_{th} \cdot \left(1 - e^{-t/R_{th} \cdot C_{th}}\right) \tag{9}$$

Table IV lists input values from manufacturer datasheets, which are used to model the temperature rise in ac inductors and dc capacitors.

TABLE IV
SPECIFICATION OF AC INDUCTOR AND DC CAPACITORS [30]-[31]

	AC Inductor	DC Capacitor
Manufacturer	MTE	EPCOS-TDK
Nominal rating I_N [A]	1000	65
Nominal hot-spot temp. $T_{hs,N}$ [C]	180	70
Maximum hot-spot temp. $T_{hs,max}$ [C]	200	85
Ambient temp. T_{amb} [C]	45	30
Nominal losses $P_{d,N}$ [kW]	1.30	10.8e-3
Core/dielectric losses [kW]	0.165	6.13e-3
Thermal resistance R_{th} [K/W]	0.104	3.8
Thermal capacitance C_{th} [W·s/K]	2.88e5	1.14e3
Size [dm^3]	84.3	0.74
Weight [kg]	152.3	0.88
Price [$]	6,307	90

V. DC FAULT SCENARIOS

A. System Description

The transient temperature rise of the power converter components is investigated using a detailed transient model of the network illustrated in Fig. 1.

Parameters for each component are listed in Table V. During normal operation, the converter output is regulated using a rotating dq0 reference frame based controller to provide 320 kW of active power P_{ac} = 320 kW into the dc network. The switches are continuously PWM modulated at fixed switching frequency of f_{sw} = 2.7 kHz, which is limited by the nominal junction temperature $T_{j,N}$ = 125 ^{0}C.

TABLE V
SYSTEM PARAMETERS OF LOW VOLTAGE DC MICROGRID [1]

Component	Data	R	L	C
ac inductor (x1)	1000 A	0.38 mΩ	43 µH	
dc capacitor (x9)	65 A	1.1 mΩ	40 nH	0.44 mF
Semiconductor (x15)	150 A/2.7 kHz	1 mΩ	40 nH	
Load (x2)	160 kW	1 Ω	-	
Battery (x1)	45 Ah/100 ms	76 mΩ	-	
Cables (L1, L2)	100 m	0.64 Ω/km	0.34 mH/km	0.1 µF/km
Cable (L3)	50 m	0.64 Ω/km	0.34 mH/km	0.1 µF/km
ac network 50 Hz	320 kVA/190 V	0.01 pu	0.1 pu	
dc network / busbar	320 kW/400 V		20 nH	

According to Table V, a total current is shared across five identical parallel-connected semiconductor switches. In order to ensure a uniform current sharing between the modules and maintain a minimal de-rating factor, following technical measures need to be considered [32]:

- Symmetric construction of the power circuit with identical connection impedance values for each paralleled module.
- Homogenous cooling with the same inlet temperature of the cooling medium for paralleled module heatsinks (to maintain a close matching junction temperatures and to avoid possible thermal runaway).
- Common gate-voltage supply and gate driver circuit.
- Usage of common-mode chokes (to mitigate effect of unequal gate driver connection impedance) and active clamps (to mitigate effect of unequal stray inductances).

The two critical fault locations highlighted in Fig. 1 are considered in order to determine the maximum thermal stress on converter components.

Faults F1 and F2 are applied at 0.5 s. Based on the dc capacitor discharge characteristics from [22], fault F1 provides a damped oscillatory response and fault F2 provides an aperiodic response. In order to determine protection system requirements for a power converter components,

The following sub-sections will first illustrate the electrical system response to these faults before the electro-thermal characteristics of the converter components are investigated.

Due to the saturation effect, during the short-circuit period the inductance of an ac reactor changes quasi-linearly in accordance with the linearity curve from Fig. 8, which is obtained from the manufacturer's datasheet [33].
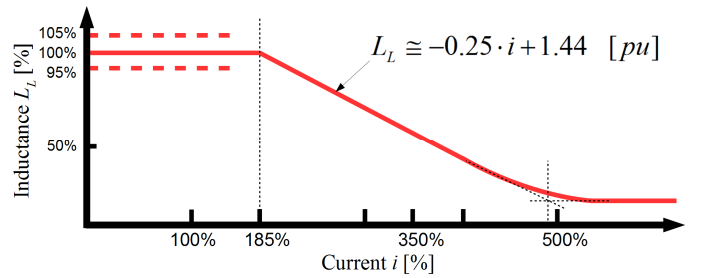

$$L_L \cong -0.25 \cdot i + 1.44 \quad [pu]$$

Fig. 8. AC inductor saturation curve of the nominal inductance changes

B. Damped Oscillatory Fault F1 (Fig. 8)

Fig. 9 shows the total fault current and its contributing components (within the close-up of the initial transient inset on the right hand side of Fig. 8) for a short circuit fault at location F1. The capacitor dictates the maximum peak fault value of 81.9 kA after 26 µs of fault occurrence. The peak fault current level is limited by the parasitic inductance L_{cap} and resistance R_{cap} of the dc capacitor and stray inductances L_{busbar} of a dc busbar.
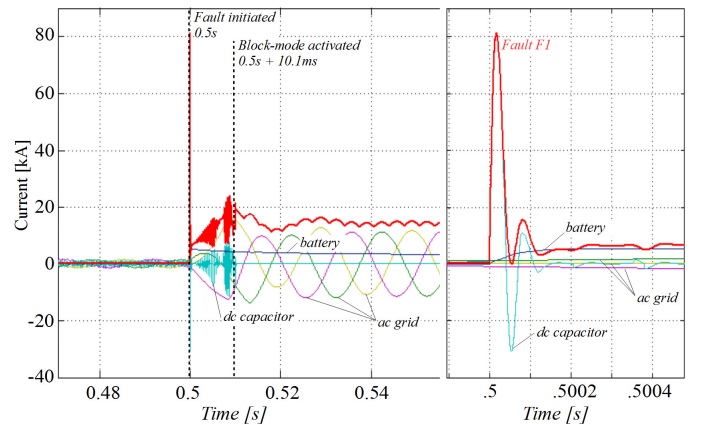

Fig. 9. Damped oscillatory fault F1 after 0.5s in low voltage microgrid

The oscillating characteristics of a dc fault current results in bidirectional flow of the current. During the negative peak of -30 kA, which is reached at 53 µs a fault current flows through parallel branches created by series-connected diodes of a converter. As a consequence, the diodes are thermally stressed within the very first microseconds of fault occurrence by the

energy coming from the dc capacitor. This energy makes the diodes exceed thermal limits before switches are blocked, as illustrated in Fig. 12.

After the capacitors rapid discharge at 0.5s + 100 μs, the interconnected battery provides the largest contribution where the maximum fault current is 5 kA. Due to the over-temperature, the block-mode of a power converter is activated after 10.1 ms of fault occurrence.

The current contribution from the battery is kept constant, as it is being continuously fed by the ac network. After 0.51s, the main fault contribution comes from ac grid and the steady value of the dc fault current becomes 14.55 kA at 0.54s, which is 18 times higher than the nominal value.

C. Aperiodic Fault F2 (Fig. 9)

Fig. 10 shows the total fault current and its contributing components for a short circuit fault at location F2. From this fig., it can be observed that at the initial stage of the fault occurrence, the dominant contribution comes from the dc battery, where current increases exponentially. After 25 ms, the battery discharges and the collapsed dc voltage results in increased ac current flow from the grid.

At 0.69 s, the junction temperature of semiconductor switches reaches 150 ^{0}C. As a consequence, the block-mode of the converter activates and all semiconductor switches are turned off. It results in an increased current flowing from the battery and a reduced current flowing through the capacitor. In accordance with the inductor time constant, ac currents keep increasing exponentially until they reach steady state level of 13.55 kA at 0.92 s.
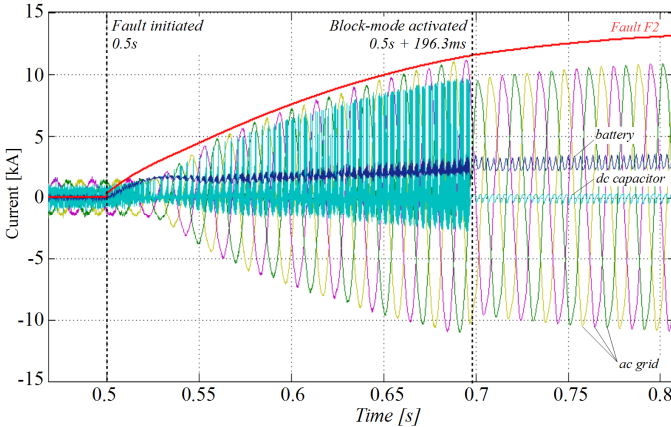

Fig. 10. Aperiodic fault F2 after 0.5s in low voltage dc microgrid.

VI. DYNAMIC ELECTRO-THERMAL ANALYSIS

A. Diodes and Switches

Complex dynamic electro-thermal models are used for the semiconductors in order to accurately represent the dissipated power from the 2.7 kHz switching operation of the converter.

Fig. 11 and Fig. 12 accordingly illustrate the registered junction temperatures and currents for each individual semiconductor switch and diode during fault F1. During normal operation, semiconductor switches operate below T_j = 125 ^{0}C, whereas the diodes operate at T_j = 60 ^{0}C.

The inherent blocking capability of the converter prevents the semiconductor switches from becoming damaged due to over-temperature. However, the diodes remain vulnerable and continue to conduct fault current even after activating the block-mode. In this case, the estimate diode junction temperature T_j exceeds maximum permissible $T_{j,max}$ = 150 ^{0}C value after 4.5 ms and temperature continues to increase until it reaches a peak of T_j = 223 ^{0}C at 15.1 ms.

After approx. 60 ms of fault occurrence, the temperature decreases to remain steady at 150 ^{0}C level, which is the result of the continuous flow of current from the ac grid. The temperature rate of change is determined by transient thermal time constant τ_{RC} and amount of energy released from rapid discharge of dc capacitor.
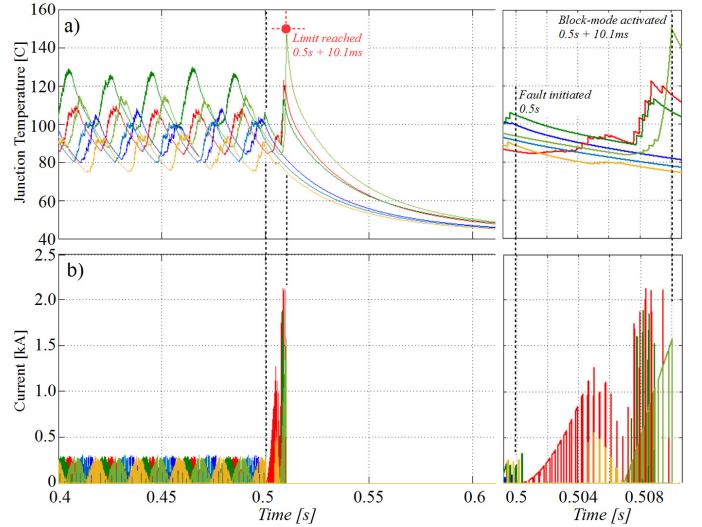

Fig. 11. a) Junction temperature variations $T_j(t)$ under fault F1; b) Currents distribution over semiconductor switches.
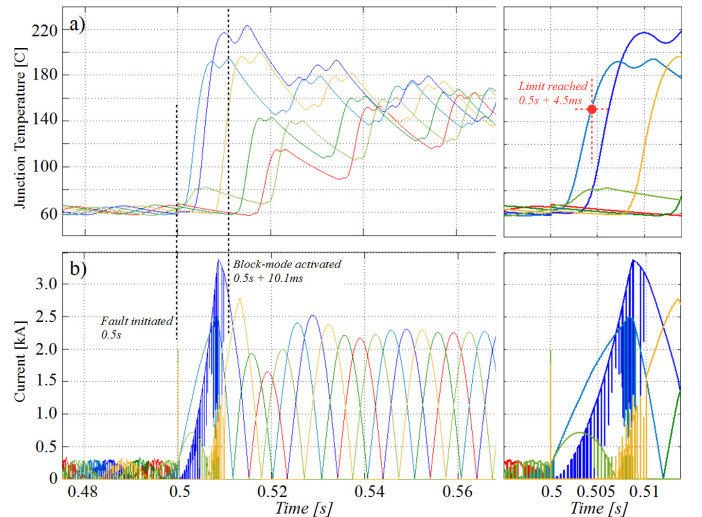

Fig. 12. a) Junction temperature variations $T_j(t)$ under fault F1; b) currents distribution over semiconductor diodes.

Thermal impact on semiconductors during aperiodic fault F2 is visualized in Fig. 13 and Fig. 14. It can be seen that the diodes will not suffer thermal stress, as the maximum junction temperature is $T_{j,max}$ = 134 ^{0}C during entire fault period. However, semiconductor switches must be isolated after 196.3 ms, which prevents the continuous fault-tolerant operation.
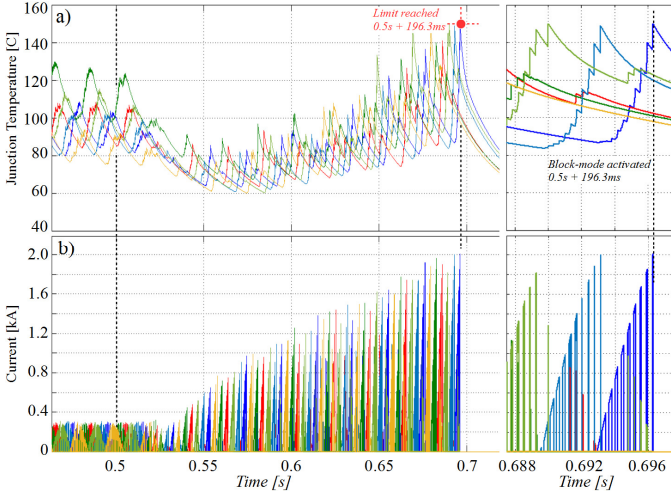
Fig. 13. a) Junction temperature variations $T_j(t)$ under fault F2; b) currents distribution over semiconductor switches.
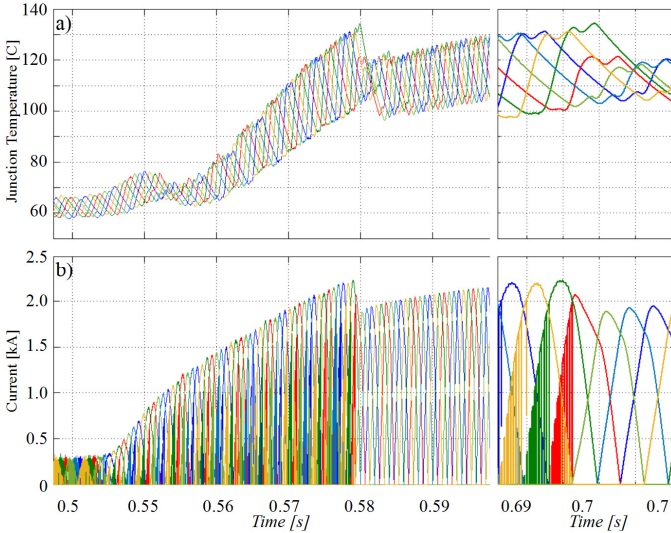

Fig. 14. a) Junction temperature variations $T_j(t)$ under fault F2; b) currents distribution over semiconductor diodes.

B. AC Inductor & DC Capacitor

Fig. 15 illustrates how the transient temperature increases for the ac inductor and dc capacitors during faults F1 and F2 (note that both faults induce a near-identical temperature rise in these passive components).
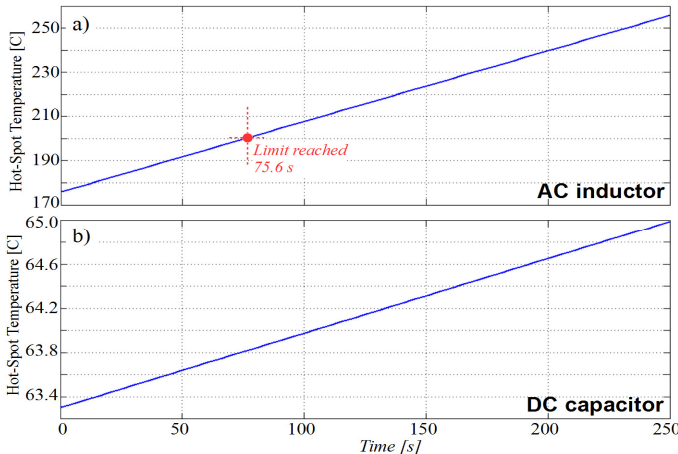

Fig. 15. Hot-spot temperature variations $T_{hs}(t)$ under faults F1 and F2: a) in ac inductor; b) in dc capacitors.

Prior to the fault, the hot-spot temperature of the ac inductor is T_{hs} = 176 ^{0}C. The registered temperature exceeds maximum permissible limit $T_{hs,max}$ = 200 ^{0}C after 75.6s for faults F1 and F2.

The hot spot pre-fault temperature of dc capacitor is 63.3 ^{0}C. After 250s duration of faults F1 and F2, the temperature of the dc capacitors increases by only approximately 1.7 ^{0}C. As a result the dc capacitor temperature

According to the Fig. 12, ac inductor and dc capacitors are not vulnerable to the short-term thermal stress caused by dc short-circuit current, since their thermal time constants are much larger than the time constants of semiconductors.

VII. DC FAULT PROTECTION CONSIDERATIONS OF POWER CONVERTER COMPONENTS

A. Impact of Ambient Conditions

Table VI presents the minimum protection operating times for a range of ambient temperatures T_{amb} = 0-60 ^{0}C, when the components are rated only for operation under normal conditions.

The total cost of dc capacitors and semiconductors from [27], [28] and [31] is estimated by adjusting the required minimum number of parallel-connected units. In this manner, the thermal design is constant and the operating temperature can be decreased by reducing the nominal device power losses $P_{d,N}$. When compared with the generalized component cost models available in [34], the total cost of paralleled-connected components do not exceed 10% of a predicted value obtained from the models.

TABLE VI
PROTECTION OPERATING TIME REQUIREMENTS FOR CONVERTERS DESIGNED FOR DIFFERENT AMBIENT CONDITIONS

Ambient temperature [^{0}C]		0	10	20	30	40	50	60
Component count	semiconductors	9	12	12	12	15	15	18
	dc capacitors	5	6	6	7	9	12	45
	ac inductor	1	1	1	1	1	1	1
Estimated cost [x1000 $]		8.4	9.0	9.0	9.1	9.8	10.1	13.6
Protection op. time [ms]		4.14	5.02	3.78	3.68	4.51	6.21	8.83

The minimum protection operating times are a function of the number of parallel-connected diodes. Table VI shows that in order to remain within the current ratings of the diodes, the fault protection system unit should detect and isolate the fault in less than 4.14 ms at T_{amb} = 0 ^{0}C and 8.83 ms at T_{amb} = 60 ^{0}C. As a result, the protection system requirements may vary with the change of ambient temperatures ΔT_{amb}. It also highlights that although the converter is operating closer to its thermal limit at higher ambient temperature, the need to include additional devices for stable operation during steady state at these ambient temperatures means that the converter is better equipped to carry excess current during fault conditions.

In order to determine the optimal operating speed for the dc fault protection unit, the current rating of converter components can be further translated into an actual cost in order to economically justify the selection of the dc fault

protection system.

Fig. 16 presents the total cost of semiconductors, which is correlated with the ranges of maximum fault breaking times t_{break}. This highlights that for ambient temperatures below T_{amb} < 50 ^{0}C, an approximate cost savings of 20% can be achieved if the protection system is capable of clearing the fault in t_{break} < 2.5 ms. Of course, this would need to be traded off against the cost of such a protection scheme when considering the full system design.
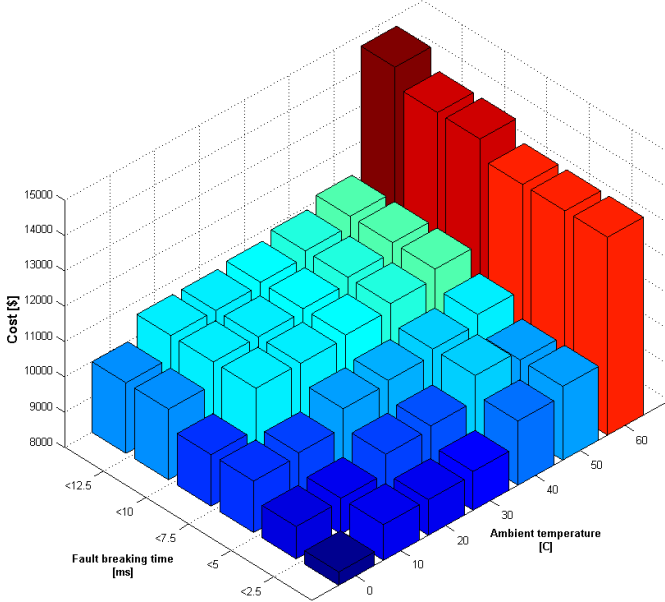

Fig. 16 Approximate cost of the required power converter for reliable operation under fault and ambient conditions.

For ambient temperatures above T_{amb} > 50 ^{0}C, a high number of parallel-connected dc capacitors is required to maintain an operation within the thermal limits. This increases the overall cost of a converter by 45%. In this case, a moderate protection system operating in t_{break} < 7.5 ms can reduce such additional cost down to 30%.

B. Impact of Latch-up Failure Mode

A high currents flowing through the semiconductor switches during the short-circuit period may result in their static latch-up and loss of switching control. In this scenario, the block-mode cannot be effectively activated, as the latched-up switches will remain in on-state mode and generate conduction losses until the converter is disconnected from the supply. This will impact the thermal characteristics of the power devices, and consequently the protection system operating requirements.

Table VII presents the obtained values of required minimum fault breaking times t_{break} for T_{amb} = 40 ^{0}C and for different current levels above the Short Circuit Safe Operating Area (SCSOA), above which a latch-up may occur. The results are performed for a nominal component count listed in Table VI.

Due to rapid discharge of dc capacitors, the currents in switches exceed latch-up limits before triggering the over-temperature protection.

TABLE VII
PROTECTION OPERATING TIME REQUIREMENTS FOR CONVERTERS WITH LATCH-UP POWER DEVICES

Latch-up current i_{latch} [pu]		No latch-up	15 pu	10 pu	5 pu	3 pu
Latch-up time [ms]		n/a	n/a	3.8	1.9	1.4
Protection op. time t_{break} [ms]	Latch-up switch	n/a	n/a	4.1	3.1	3.2
	Diode	4.51	4.51	7.33	7.53	7.42

If a latch-up occurs at low current levels below i_{latch} < 10 pu, the diodes allow a longer time frame of 7ms for fault clearance in comparison to a latch-up free operation. This is due to the parallel short-circuit commutation path formed within a converter phase leg. A path is formed by a latch-up switch, which effectively splits the current from the ac network flowing between the switch and the series-connected diode

A more vulnerable than diodes are the switches that experienced latch-up and generate excessive conduction losses. In order to avoid their rupture, the protection system has to isolate latch-up switches in t_{break} < 3 ms.

Fig. 17 presents the minimum number of additional parallel-connected semiconductors required due to latch-up. The number will vary in accordance with the operating speed of a protection system.
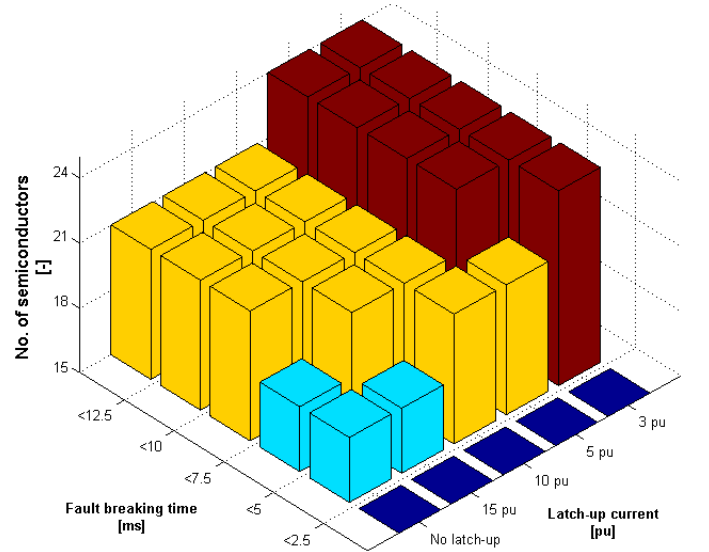

Fig. 17 Minimum number of semiconductors required for safe operation during different latch-up failure modes.

The worst conditions occur for a latch-up at 3pu of a device rated current (i_{latch} = 3·I_N = 450 A). In this scenario, a fast-acting protection is required with t_{break} < 2.5ms. Otherwise, additional semiconductors are required, which account for 16% of a total cost. If a device has a high latch-up free operation up to 10-15pu and t_{break} > 2.5ms, total cost increases by 5%.

C. Impact of Fault Current Limiters

A reliable fast-acting fault current limiter can be considered to optimize a design of fault protection scheme in terms of cost and operating speed. In this paper, impact of fault current limiter on system performance is examined based on current

limiting level. The simulation results have shown, that four current limiting levels $I_{limit(\%)}$ can be identified and associated to different operating conditions. This has been illustrated in Table IV with obtained ranges for current limiting levels, when the fault current limiter is activated immediately after the presence of a fault, which corresponds to the usage of solid state limiters. The results are performed for a nominal component count listed in Table VI for $T_{amb} = 40\ ^0$C.

With fault current limiters capable of a suppressing a short-circuit current up to $I_{limit(\%)} = 40\%$ of its maximum value, no effect has been observed on a dynamic temperature characteristics of power devices. The protection system operating times will remain the same and they will dictate the required minimum number of components to withstand fault conditions.

TABLE VIII
EFFECT OF SOLID STATE FAULT CURRENT LIMITERS ON PROTECTION SYSTEM OPERATING REQUIREMENTS

$I_{limit(\%)}$	Effect	Description
< 40%	Fast-acting protection required	No significant effect is observed on the thermal loading of power devices
40-60%	Slow-acting protection required	Converter is set to block-mode and diodes need to be disconnected after appr. 100ms
60-80%	Block-mode activated	Converter is set to block-mode, but diodes can remain interconnected
> 80%	Continuous operation	Converter maintains continuous fault-tolerant operation

If a fault current limiter has a higher limiting factor $I_{limit(\%)} > 40\%$, a fast-acting fault protection system that operates within a few milliseconds is no longer required. When more effective fault limitation is applied at $I_{limit(\%)} = 80\%$, power converter will maintain a continuous fault-tolerant operation.

VIII. CONCLUSIONS

The understanding of potential thermal stress on power converter components during fault conditions is key to fully defining the protection requirements in future DC microgrids. The type of analysis described in this paper enables more effective system design by articulating the relationship between converter sizing and protection system speed. Ultimately this can then be translated into cost, as has been shown, which helps support design decision making.

The proposed low level component-based electro-thermal modelling approach used in this paper to characterize the thermal effects on power converters is universal in a sense that it can be applied for different converter topologies that operate at different ratings and conditions. Therefore, in a similar manner to cable designs or busbar configurations, a consistent procedure can be used to estimate the thermal effects of large high voltage power converters, where much greater cost can be reduced with appropriate trade-off between the selection of protection system design and size of a converter.

Results have further shown that semiconductors are the most vulnerable components against the short-term thermal stress, which is the consequence of their relatively short thermal time constant. Using nominal ratings, semiconductors may not withstand faults and their ratings may need to be improved. The additional cost of fault-tolerant semiconductors can be compensated with fast-acting dc protection, capable of clearing the faults in less than few milliseconds. Simulation results presented in this paper have also shown that implementation of fast-acting dc fault protection may be economically justified, especially for low ambient operating temperature conditions.

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