Multi-Pole Voltage Source Converter HVDC Transmission Systems

Grain Philip Adam and Barry Wayne Williams

***Abstract*—This paper connects several modular multilevel converters to form multi-pole VSC-HVDC links which are suited for bulk power evacuation, with increased resiliency to ac and dc network faults. The proposed arrangements resemble symmetrical and asymmetrical HVDC links that can be used for bulk power transfer over long distances with reduced transmission losses, and for the creation of multi-terminal super-grids currently being promoted for transitional dc grids in Europe. The technical feasibility of the proposed systems is assessed using simulations on symmetrical and asymmetrical tri-pole VSC-HVDC links, including the case of permanent pole-to-ground dc faults.**

***Key words*—half-bridge and full-bridge modular multilevel converter; line commutating converter; multi-pole high-voltage dc link; and voltage source converter high-voltage dc transmission systems.**

I. INTRODUCTION

Several ultra-high voltage dc (UHVDC) transmission systems based on the current source line commutating converter (LCC) with dc operating voltages up to ±800kV (800kV per pole) and 7200MW rated power have been installed to supply mega cities[1-9]. The choice of LCC is mainly driven by the established track record of LCC in bulk power evacuation over long distances for over 50 years. Proper operation of an LCC-UHVDC link with such large power rating requires the inverter side to be connected to a strong ac network in order to prevent converter commutation failure during ac network disturbances [10, 11]. LCC-HVDC links consumes large reactive power that can reach to 50% or 60% of the transmitted dc power, and it varies with the magnitude of dc power being exchanged between two ac networks [9, 12, 13]. Filter capacitors plus dedicated switched shunt capacitors are widely used to compensate the reactive power of the LCC in a discrete fashion, but this has proven to cause significant instantaneous reactive power mismatch at the filter bus that can create large over-voltages in weak ac networks. This drawback has been avoided in recent LCC-HVDC transmission links installations by replacing the switched capacitors with a line commutating dynamic reactive power compensator that autonomously and seamlessly adjusts its reactive power output in an attempt to maintain constant voltage at the filter bus[6-8, 12, 14-21].

A self-commutated voltage source converter high-voltage dc (VSC-HVDC) transmission system presents a competitive alternative to the LCC-HVDC transmission system, for transmitting power over long distances, without the commutation failure shortcoming of the LCC systems. But converter topologies employed in the early VSC-HVDC transmission systems limit their power rating and dc operating voltage to 500MW and ±200kV (symmetrical mono-pole), which are much lower than that of LCC-HVDC links [9, 22-31]. To increase the power handing and dc operating voltage of VSC-HVDC transmission systems, modular and hybrid multilevel voltage source converters have been adopted in preference to traditional two-level and neutral-point clamped (NPC) converters[32-38]. Modular and hybrid multilevel converters allow dc operating

voltage and power handling per converter to be increased up to ±320kV and 1GW when using commercially available gate insulated bipolar transistors (IGBT). As in LCC-HVDC links, metallic return bi-poleVSC-HVDC links can be used to further increase the transmission capacity and reduce transmission losses. Reference [39] presents a project under construction that uses a new generation bipolar HVDC link that employs an LCC in one pole and a VSC in other pole, but there is no bi-polar VSC-HVDC link currently operational, with both poles being a VSC.

An asymmetric tri-pole HVDC link variation created by connection of a bipolar HVDC link that employs half-bridge modular multilevel converter to a third pole that employs full-bridge modular multilevel converters is presented in [40, 41]. In [40, 41] the bipolar dc voltage capability of the third pole that employs the full-bridge modular converters is used to reduce the transmission losses by ensure zero current in metallic return, independent of loading in its bipolar part. The main drawbacks of this are:

- It restricts the third pole to act as a dc power balancer with limited power transfer and
- a zero current in the metallic return is achieved by manipulating the dc voltage polarities of the third pole, which requires the use mass impregnated dc cables and converter transformers with high insulation in this pole in order to cope with the bipolar dc voltage stresses during dc voltage reversal.

This paper uses tri-pole and quad-pole VSC-HVDC links as examples of multi-pole dc transmission systems that can be used to transmit bulk power over long distance with reduced transmission losses compared to three or four parallel point-to-point HVDC links, with improved resiliency to forced (faults) and schedule (maintenance) outages. Viability of the proposed multi-pole VSC-HVDC link is assessed on illustrative models of symmetrical and asymmetrical tri-pole HVDC links, where each terminal comprises three 21-cell MMCs modelled using the electromagnetic transient simulation approach described and validated in [32]. Despite the advantages of the multi-pole HVDC link, a pole-to-ground dc fault example in this paper shows that its symmetrical version exposes interfacing transformers and dc lines to excessive dc voltage stresses that may lead to insulation breakdown. Thus, it is suitable for overhead lines should appropriate countermeasures to deal with excessive over-voltages on the converter transformers are put in place.

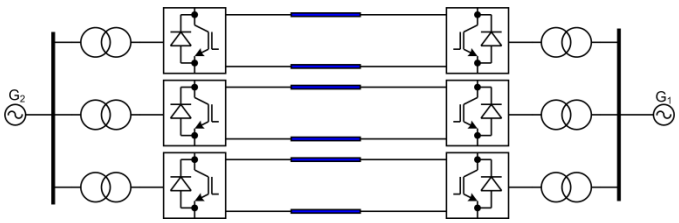
II. MULTI-POLE VSC-UHVDC LINK

Figure 1 shows five network topologies for VSC-HVDC links that can be employed for bulk power evacuation. The topology in Figure 1 (a) uses three parallel monopole HVDC links, with six fully insulated dc cables (expensive); and it has high transmission losses, approximately, $6R_{dc}I_{dc}^2$, where R_{dc} and I_{dc} are resistance and dc current per cable. Figure 1 (b) is a symmetrical tri-pole UHVDC link that uses four fully insulated dc cables, with zero currents in the two inner cables should the total power transfer be evenly shared between the three converters of each terminal. Its transmission losses are $2R_{dc}I_{dc}^2$, which is one third that for Figure 1 (a). However, its main weakness is that the converter interfacing transformers connected to the two outer poles (upper and lower) experience dc stresses of V_{dc} and -V_{dc}, where V_{dc} is the dc voltage across dc link of a single

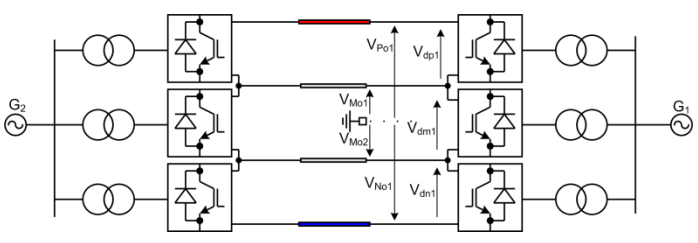
converter. These interfacing transformers are exposed to additional dc voltage stresses during a pole-to-ground dc fault. Figure 1(c) is an asymmetric tri-pole HVDC link that uses three fully insulated dc cables with one metallic return referenced to ground. The main attributes of this configuration are: it exposes all interfacing transformers to limited dc voltage stresses - equal to that of a typical asymmetrical monopole, $½V_{dc}$, and its transmission loss is $3R_{dc}I_{dc}^2$, which is half of that in Figure 1 (a). Theoretically, the multi-pole HVDC link can be extended to any pole number. For example, Figure 1(d) shows a quad-pole VSC-UHVDC link capable of transmitting the rated power of quad-pole in Figure 1 (e) using only two dc cables, with zero current in the two inner cables when the transmitted power is equally shared between the converters of each terminal, with the dc current per cable the same in both cases. However, the dc cables of the outer poles are exposed to higher dc voltage stress relative to ground compared to the two inner cables. Therefore, application of the tri and quad poles in Figure 1 (c) and (d) is expected to be limited to overhead lines since the insulation demand may be too high for under-ground and subsea cables.

The asymmetric quad-pole in Figure 1 (e) can be considered as two independent bi-pole HVDC links. Converters connected to the two upper poles form two asymmetric independent monopoles, with their negative poles grounded, whilst converters connected to the two lower poles form two independent monopoles HVDC, with their positive poles grounded. The quad-pole HVDC link in Figure 1 (e) can be operated with zero current in metallic return even when its two independent bi-polar systems are operated with the same or different dc voltages or powers. Currently application of the quad-pole in Figure 1 (e) is limited to cable systems because the maximum dc operating voltage of commercially available dc cables is limited to 320kV. The attraction of the quad-pole in Figure 1 (e) is that it can carry the rated power of four mono-pole HVDC links using only four dc cables; thus, it halves cable costs and transmission losses. The inherent redundancy of quad-pole in Figure 1 (e) and its modular structure can be used to minimize the power loss due to planned or forced outage of the dc cables or converter stations. Also the quad-pole in Figure 1 (e) exposes its converter transformers to dc voltage stress of $½V_{dc}$, and without any additional dc voltage stresses on dc cables during dc faults, as with the topology in Figure 1 (d).

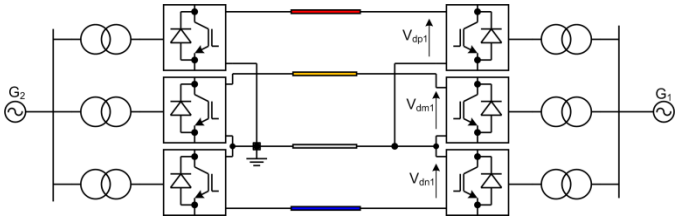
This discussion shows that multi-pole VSC-UHVDC links can facilitate bulk power evacuation over long distances, without the shortcomings of LCC-UHVDC links. A benefit of the multi-pole VSC-UHVDC links in Figure 1 (b) to (e) is that any dc fault impact is constrained to the affected pole; which may make this approach attractive for multi-terminal dc networks; especially as the risk of system collapse due to a dc fault could be avoided. Additionally, the attributes of the half-bridge modular multilevel converter, such as modularity and internal fault management, may simplify practical realization of the multi-pole VSC-UHVDC links being advocated in this paper.

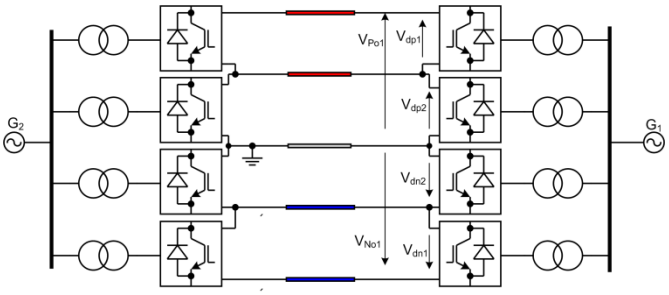


(a) Three parallel monople VSC-HVDC links



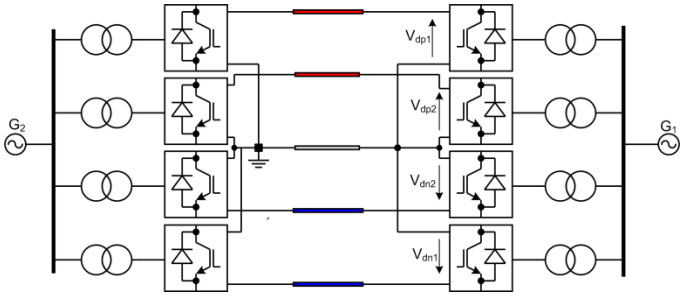
(b) Topology A: symmetrical tri-pole UHVDC link





(c) Topology B: asymmetrical tri-pole HVDC link

(d) Topology A: asymmetrical quad-pole UHVDC link



(e) Topology B: asymmetrical quad-pole HVDC link

Figure 1: Some possible connections for multi-pole HVDC links for bulk power evacuation.

III. REVIEW OF THE MODULAR MULTILEVEL CONVERTER AND ITS CONTROL

Figure 2 shows one-phase of half-bridge modular multilevel converter (HB-MMC) that employs N cells per arm. HB-MMC is widely accepted converter topology for HVDC applications with rated power and dc operating voltage up to 1000MW and ±320kV respectively. At present there are several methods being used to control HB-MMC [32, 42-47] and to suppress the 2nd harmonic currents in its arms. Although there are noticeable differences in complexity and dynamic performance of these methods, the majority offer stable operation in balanced, unbalanced and ac fault conditions. With adequate arm reactors and interfacing transformer leakage impedance, HB-MMC switching devices experience lower current stresses during dc faults compared two-level and NPC converters due to absence of concentrated dc capacitor at its input dc link[32, 48, 49]. Also, its distributed cell capacitors that do not contribute fault current when converter switches are blocked during dc faults[32]. These attributes make HB-MMC a suitable candidate for multi-pole HVDC links that will be explored in this paper. Basic differential equations that describe HB-MMC ac and dc side dynamics on per phase basis are (for phase a, and applicable for remaining phases)[32, 50]:

$$(L_T + \tfrac{1}{2}L_d)\frac{di_{a0}(t)}{dt} = -(R_T + \tfrac{1}{2}R_d)i_{a0}(t) + \tfrac{1}{4}(v_{cap1}(t) + v_{cap2}(t))\bar{u}_a(t) - v_a(t) \qquad (1)$$

$$L_d\frac{di_{com}(t)}{dt} = -R_d i_{com}(t) + \tfrac{1}{2}V_{dc}(t) - \tfrac{1}{4}(v_{cap1}(t) + v_{cap2}(t)) \qquad (2)$$

The voltages developed across the HB-MMC upper and lower arms are $v_{a1}(t) \approx \frac{1}{4}(v_{cap1}(t)+v_{cap2}(t))(1-\bar{u}_a(t))$ and $v_{a2}(t) \approx \frac{1}{4}(v_{cap1}(t)+v_{cap2}(t))(1+\bar{u}_a(t))$; phase '*a*' output current, which is equal to differential-mode current is given by $i_{a0} = i_{a1} - i_{a2}$, where i_{a1} and i_{a2} are upper and lower arm currents; common mode or circulating current shared between upper and lower arm of phase '*a*' is $i_{com}(t) = \frac{1}{2}(i_{a1}(t)+i_{a2}(t))$; the modulation signal for phase is $\bar{u}_a(t) = m\sin(\omega t+\delta)$; the sum of the upper and lower cell capacitor voltages are $v_{capl}(t) = \sum_{j=1}^{N} v_{c1j}(t)$ and $v_{cap2}(t) = \sum_{j=1}^{N} v_{c2j}(t)$; and the average cell capacitor voltages for the upper and lower arms of phase '*a*' are $\bar{V}_c(t) = \frac{1}{2}(v_{cap1}(t)+v_{cap2}(t))$.

Considering phase '*a*', the voltage developed across upper and lower arms (v_{a1} and v_{a2}) can be approximated in terms of individual cell capacitor voltages and the state of the auxiliary switch in series with each cell capacitor:

$$\begin{aligned} v_{a1}(t) &= \sum_{j}^{N} v_{c1j}(t) S_{x1j} \approx \tfrac{1}{2}\bar{V}_{c1}(1-\bar{u}) \\ v_{a2}(t) &= \sum_{j}^{N} v_{c2j}(t) S_{x2j} \approx \tfrac{1}{2}\bar{V}_{c2}(1+\bar{u}) \end{aligned} \qquad (3)$$

Similarly, the upper and lower arm individual cell capacitor voltages are:

$$\begin{aligned} C\frac{dv_{c1j}(t)}{dt} &= S_{x1j}(t) i_{a1}(t) \\ C\frac{dv_{c2j}(t)}{dt} &= S_{x2j}(t) i_{a2}(t) \end{aligned} \qquad (4)$$

In addition to (4), the differential equations that describe the entire dynamics of the upper and lower arm cell capacitor voltages are:

$$\begin{aligned} \frac{C}{N}\frac{d}{dt}\sum_{j=1}^{N} v_{c1j}(t) &= i_{a1}(t) \times \frac{1}{N}\sum_{j=1}^{N} S_{x1j}(t) \\ \frac{C}{N}\frac{d}{dt}\sum_{j=1}^{N} v_{c2j}(t) &= i_{a2}(t) \times \frac{1}{N}\sum_{j=1}^{N} S_{x2j}(t) \end{aligned} \qquad (5)$$

Assuming the individual cell capacitor voltages of the upper and lower arms are regulated at $v_{c11}(t) = v_{c12}(t) = ... = v_{c1N}(t) = V_{c1}/N$ and $v_{c21}(t) = v_{c22}(t) = ... = v_{c2N}(t) = V_{c2}/N$ (practically, $V_{c1} \approx V_{c2} \approx V_{dc} \pm \frac{2}{3} R_d I_{dc}$, where R_d represents the equivalent resistance that accounts for on-state dc voltage drop in the semiconductor switching devices and arm reactor internal resistance, and I_{dc} is the dc link current), then the switching function of the upper and lower arms can be deduced from equation (3) as:

$$\begin{aligned} \frac{1}{N}\sum_{j}^{N} S_{x1j}(t) &\approx \tfrac{1}{2}(1-\bar{u}(t)) \\ \frac{1}{N}\sum_{j}^{N} S_{x2j}(t) &\approx \tfrac{1}{2}(1+\bar{u}(t)) \end{aligned} \qquad (6)$$

Using (6), the voltage developed across the upper and lower arms of the HB-MMC reduced to:

$$v_{a1}(t) \approx \tfrac{1}{2} V_{c1}(1-\bar{u}(t))$$
$$v_{a2}(t) \approx \tfrac{1}{2} V_{c2}(1+\bar{u}(t)) \quad (7)$$

Also by using (6), equation (5) reduces to:

$$C_e \frac{dv_{cap1}(t)}{dt} = \tfrac{1}{2} i_{a1}(t)(1-\bar{u}(t))$$
$$C_e \frac{dv_{cap2}(t)}{dt} = \tfrac{1}{2} i_{a2}(t)(1+\bar{u}(t)) \quad (8)$$

where $C_e=C/N$ is the equivalent cell capacitance.

In this paper, each MMC uses control that regulates the output phase currents in the *d-q* synchronous reference frame, with decoupling between the *d* and *q* channels using feed-forward terms to improve the system immunity against disturbance, and the outer loops of the *d* and *q* channels regulate active power/dc voltage and ac voltage/reactive power respectively[32, 43]. So, the inner fundamental current controller in the *d-q* reference frame is designed based on equation (1), as in [32]. The controller for 2nd harmonic current suppression in each converter arm is designed based on (2) as in [32]. However, in this paper, each phase uses a proportional resonant (PR) controller instead of a proportional-integral (PI) controller. To facilitate PR controller design for 2nd harmonic suppression, the following change of variable is made in equation (2): $u_x(t) = \tfrac{1}{2} V_{dc} - \tfrac{1}{4}(v_{cap1}(t) + v_{cap2}(t))$ and $u_x(t)$ becomes:

$$u_x(s) = k_p\left[i^*_{com}(s) - i_{com}(s)\right] + \frac{k_r}{s + \omega_0^2/s}\left[i^*_{com}(s) - i_{com}(s)\right] \quad (9)$$

After replacing the second term of (9) by *z(s)*, $u_x(t)$ can be transformed back to the time domain as $u_x(t) = k_p\left[i^*_{com}(t) - i_{com}(t)\right] + z(t)$ and *z(s)* temporarily remains in s-domain and is rearranged as:

$$\left[s + \omega_0^2/s\right] z(s) = k_r\left[i^*_{com}(s) - i_{com}(s)\right] \quad (10)$$

After splitting (10) into two state space equations, and $u_x(t)$ is substituted in (2), the following equations result:

$$\frac{di_{com}(t)}{dt} = -\frac{(R_d + k_p)}{L_d} i_{com}(t) + \frac{z(t)}{L_d} + \frac{k_p}{L} i^*_{com}(t) \quad (11)$$

$$\frac{dz(t)}{dt} = -k_r i_{com}(t) + w(t) + k_r i^*_{com} \quad (12)$$

$$\frac{dw(t)}{dt} = \omega_0^2 z(t) \quad (13)$$

Laplace transformation and algebraic manipulation of (11), (12) and (13), gives:

$$\frac{i_{com}(s)}{i^*_{com}(s)} = \frac{k_p}{L_d} \times \frac{s^2 + k_r/k_p\, s + \omega_0^2}{s^3 + (R_d + k_p)/L_d\, s^2 + (\omega_0^2 + k_p/L_d)s + \omega_0^2 (R_d + k_p)/L_d} \quad (14)$$

The transfer function (14) is used to select the gains for the PR controller that supresses the 2nd harmonic current in each converter arm. This controller is incorporated as a supplementary controller that modifies the modulating signals from the fundamental current controller. The reserved modulation index dedicated for 2nd harmonic current suppression is limited to 5% as shown in Figure 3, and this means when modulation index reserved for 2nd harmonic current suppression exceeds 5%, priority is given to active and reactive power exchange. This paper uses the generic MMC control approach summarised in Figure 3 [32], (rather than the per arm approach with the average arm or cell capacitor voltage regulation discussed in [43, 51-54]), due to its simplicity and robustness, as the modulation stage has minimal dependency on the control.

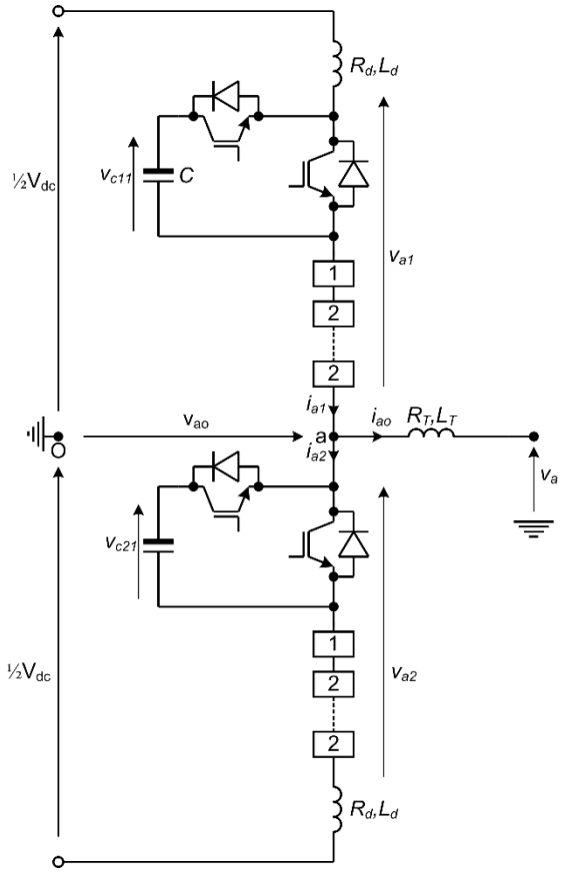


Figure 2: Half-bridge modular multilevel converter (HB-MMC)

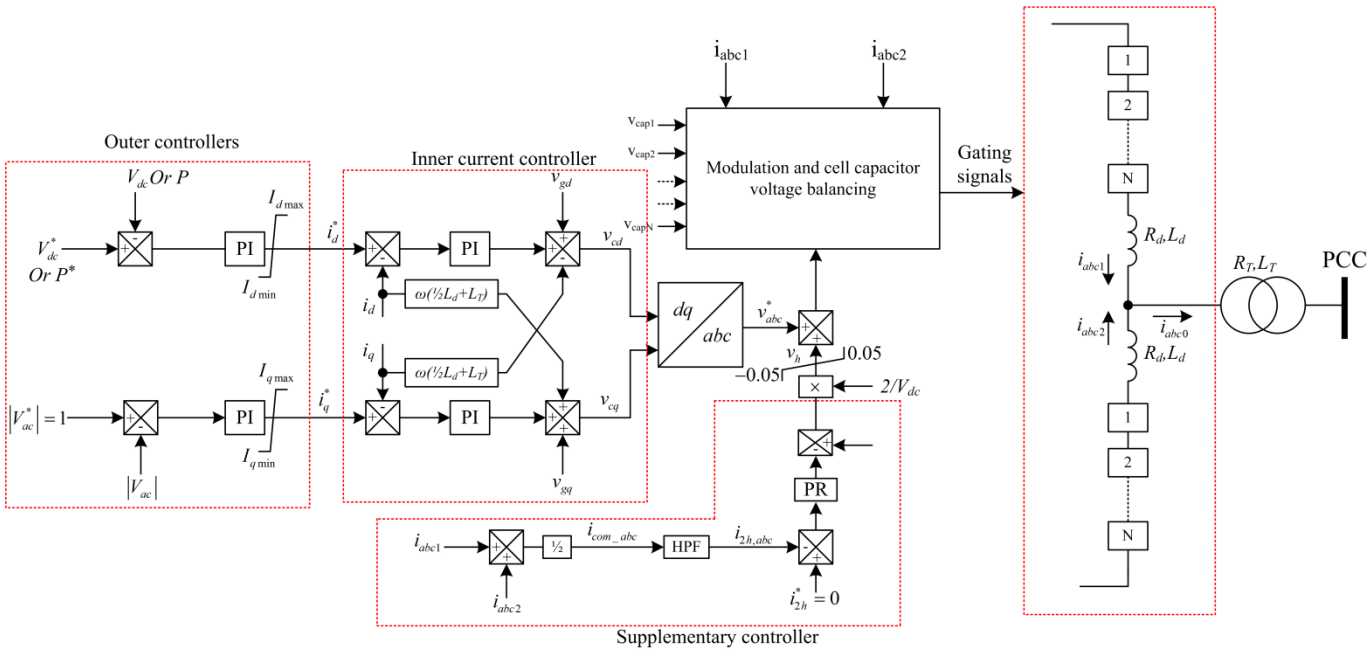


Figure 3: Generic control system employed in the converter stations of the test system in Figure 4.

IV. TEST SYSTEMS AND ILLUSTRATIVE SIMULATIONS

A) Network description

Figure 4 shows an illustrative tri-pole UHVDC link with a ±600kV dc operating voltage, rated at 1200MW (400MW per pole). Each UHVDC link terminal in Figure 4 has three HB-MMCs, with 21 cells per arm, each rated at 450MVA with a 400kV dc link voltage, and each sub-converter is connected to a 400kV ac network using a 200kV/400kV Y/Y interfacing transformer. Each MMC of station 1 (MMC_{11}, MMC_{12} and MMC_{13}) is configured to exchange one third the total power being exchanged between G_1 and G_2; while each MMC of station 2 (MMC_{21}, MMC_{22} and MMC_{23}) regulates its dc link voltage at 400kV. The MMCs of both converter stations are modelled using the electromagnetic transient simulation model validated in [32], and controlled using amplitude modulation. CB_{11} and CB_{12}, CB_{21} and CB_{22}, CB_{31} and CB_{32}, and CB_{41} and CB_{42} represent the dc circuit breakers in each line end; and GSB_1 and GSB_2 are the ground transfer switches used to define ground when the system is reconfigured as a typical bi-pole HVDC link following loss of symmetry due to a dc fault or scheduled maintenance. V_{P01}, V_{M01}, V_{M02} and V_{N01} represent pole-to-ground dc voltages, measured at points P_1, M_1, M_2 and N_1, at the terminals of station 2; while $V_{dp1,2}$, $V_{dm1,2}$and $V_{dn1,2}$ are pole-to-pole dc voltages at the MMCs of stations 1 and 2, see Figure 4. Table I summarizes the main test system parameters.

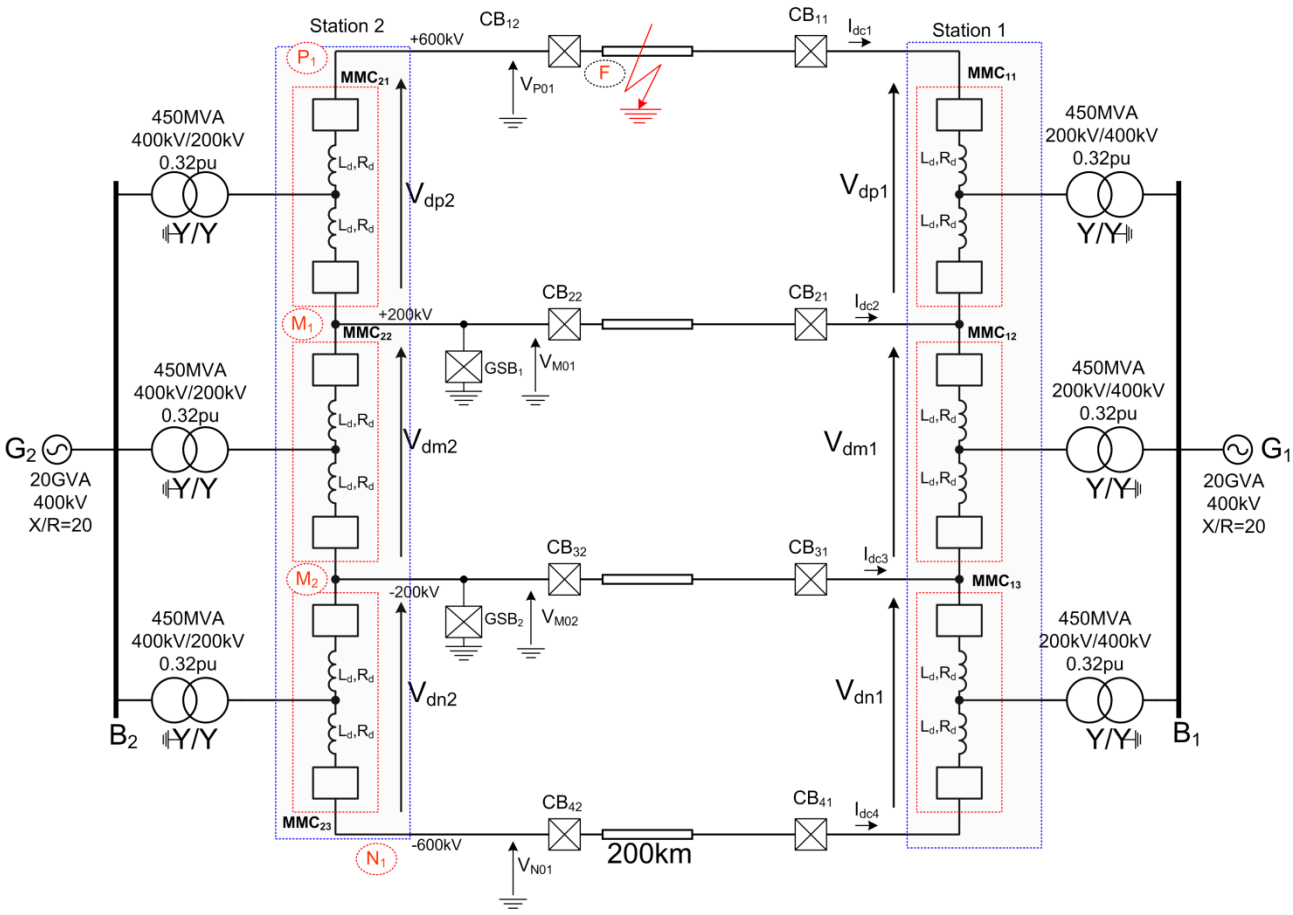


Figure 4: Two-terminal symmetrical tri-pole UHVDC link (Topology A).

Table I: Summary of system parameters

Parameters	Value	Parameters	Value
Converter rated power	450MVA	Interfacing transformer leakage reactance per phase	0.32pu
Converter rated dc link voltage	400kV	Interfacing transformer winding resistance per phase	0.002pu
Converter rated ac terminal voltage	200kV	Interfacing transformer nominal voltage ratio	200kV/400kV
Number of cells in each converter arm (N)	21	DC cable resistance	10mΩ/km
Cell capacitance (C_m)	1.4mF (71ms)	DC cable inductance	0.8mH/km
Arm inductance (L_d)	30mH	DC cable capacitance	0.25μF/km
Lumped on-state resistance of the switching devices plus arm reactor internal resistance (R_d)	0.35Ω	Line length	200km

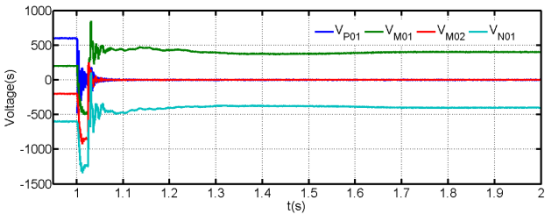
B) Topology A - tri-pole UHVDC link

This section uses simulation results from the illustrative two-terminal symmetrical tri-pole UHVDC link in Figure 4, to examine the transient response of multi-pole dc transmission systems. Figure 5 displays the simulation results when the UHVDC link in Figure 4 is initially operated as a symmetrical triple pole, with ground transfer breakers GSB_1 and GSB_2 open, when each Station 1 MMC is commanded to exchange 360MW with G_1 (total of 3×360MW), while they autonomously participating in ac voltage regulation at PCC_1. At time t=1s, a permanent pole-to-ground dc fault is applied at point 'F' and is cleared after 20ms having opened dc circuit breakers CB_{11} and CB_{12}. MMC_{11} and MMC_{21} which are connected to the faulty pole are permanently blocked at t=1s and MMC_{11} output power is reduced to zero. To avoid exposing the dc lines and converter transformers to excessive voltage stresses for an extended period, ground transfer breaker GSB_2 is closed at t=1.025s

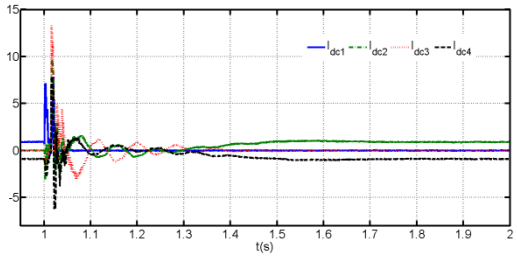
(25ms from the fault initiation) to allow the healthy part of the link to operate as a typical bi-pole HVDC link with the metallic return grounded at Station 2.

Figure 5 (a) shows the pole-to-ground dc voltages measured at the terminals of Station 2. The UHVDC link being studied operates as symmetrical triple pre-fault with each dc line (cable) experiencing its nominal dc voltage stress, as explained and as depicted in Figure 4. Before closing of the ground transfer breaker during the pole-to-ground dc fault, the dc voltage stresses on the dc lines and converter transformers increase significantly. This indicates that without adequate countermeasures, such as closing GSB_2, insulation failure of the dc lines and converter transformers is imminent. Following fault clearance by opening the faulty line, the healthy part operates as a typical bi-pole HVDC system with a ±400kV dc voltage. The plot for dc link currents measured at the terminal of Station 2 in Figure 5 (b) show that no currents are observed in the two middle dc cables (lines) in the pre-fault period (I_{dc2} and I_{dc3}) when the system operates as a symmetric triple. During the fault period, the faulty dc cable exhibits a large transient discharge current from its distributed stray capacitors, and this current drops to zero rapidly as the stray capacitors discharge, see the plot of I_{dc1} in Figure 5 (b). When the fault is cleared, the remaining part operates as a typical bi-pole HVDC link with zero current in metallic return, see plot for I_{dc3} in Figure 5 (b). Although the power exchange between G_1 and G_2 is reduced to zero, forced grounding of the dc cable which is designated as the metallic return by closing of the ground transfer breaker (GSB_2) has created large transient over-currents at t=1.025s , see Figure 5 (b). Figure 5 (c) to (f) shows current waveforms of the converters connected to the faulty and the healthy poles exchange with G_1 and G_2. The action taken during the fault are sufficient to prevent the converters connected to the faulty pole from being exposed to excessive current or voltage stresses, while those connected to the healthy poles continue to operate but with zero power exchange with the ac grids G_1 and G_2. The upper and lower arm currents in Figure 5 (g) to (j) show that all the converters connected to the faulty and healthy poles experience transient over-currents because they share the same component of the common-mode current that forms the dc link current. Large time constant due to sizable arm and line inductances of the fault current path will not allow rapid fall of the common-mode current component to zero as ac power and current. Figure 5 (k) to (n) show that voltage balancing of the cell capacitors of the converters connected to the faulty and healthy poles is maintained, but the cell capacitor voltages of the unblocked converters which are connected to the healthy poles, exhibit significant transients. Figure 5 (m) and (n) show that some of the cell capacitor voltage of MMC_{12} and MMC_{22} have drifted beyond the desired settling point (increased and decreased) to the levels that may trigger emergency control action such as forced bypassing of the affected cells or blocking of the entire converter. The phase voltages MMC_{11} and MMC_{12} present to the low-voltage windings of their interfacing transformer in Figure 5 (o) and (p) show that the dc components of the phase voltages, measured relative to the dc ground, vary significantly from pre-fault to post-fault. These results indicate that the dc stress levels impressed on converter transformers during a pole-to-ground dc fault may cause insulation breakdown if appropriate actions are not quickly initiated. This discussion highlights that the proposed multi-pole UHVDC link offers possibilities for increasing the power handling and reliability of VSC based HVDC links using existing converter and semiconductor technologies, but also presents operational

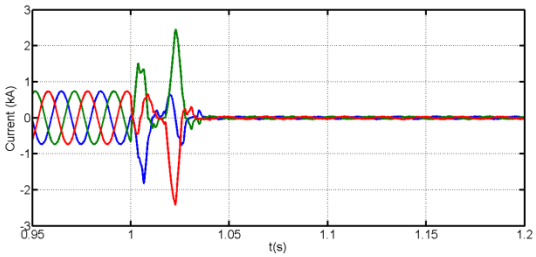
challenges during major network disturbances. Additional results in the appendix illustrate the internal dynamics of the symmetric tri-pole UHVDC link in Figure 4 when active power is commanded to vary from 0.5pu to 0.8pu.



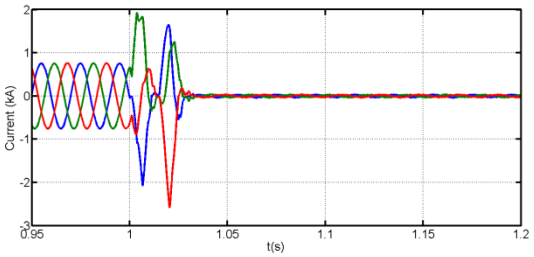
(a) Samples of pole-to-ground dc voltages measured at the terminals of Station 2 (V_{P01}, V_{M01}, V_{M02} and V_{N01})



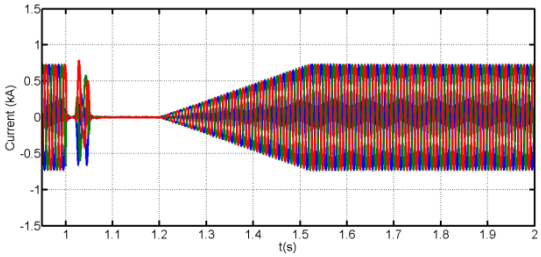
(b) DC link current measured at the terminals of Station 2



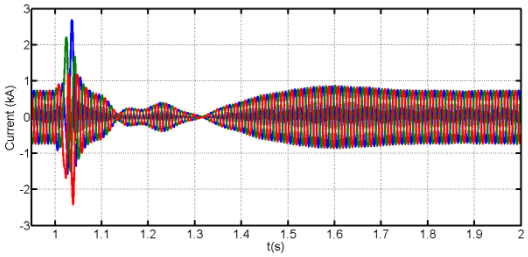
(c) Current waveforms MMC_{11} (upper converter of Station 1) exchanges with AC grid G_1



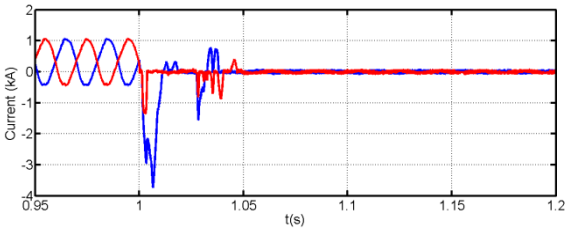
(d) Current waveforms MMC_{21} (upper converter of Station 2) exchanges with AC grid G_2



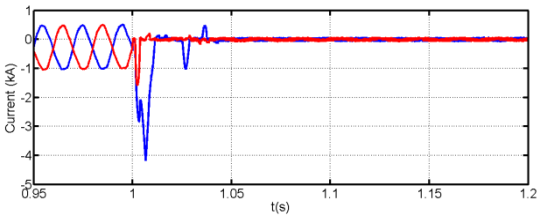
(e) Current waveforms MMC_{12} (middle converter of Station 1) exchanges with AC grid G_1



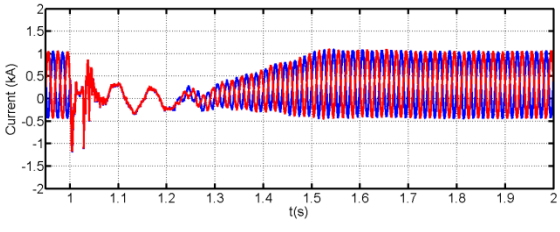
(f) Current waveforms MMC_{22} (middle converter of Station 2) exchanges with AC grid G_2



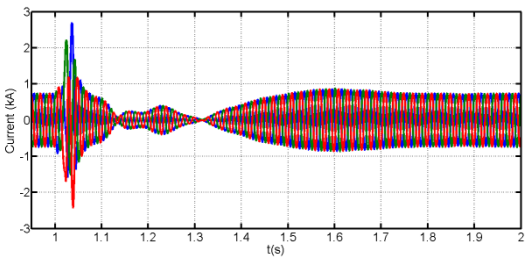
(g) MMC_{11} upper and lower arm currents (phase *a*)



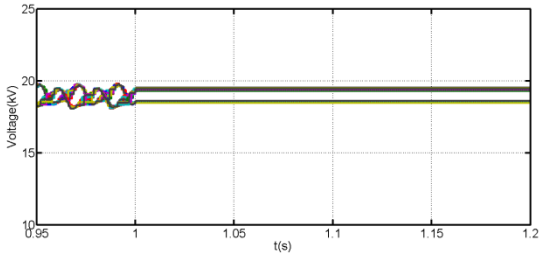
(h) MMC_{21} upper and lower arm currents (phase *a*)



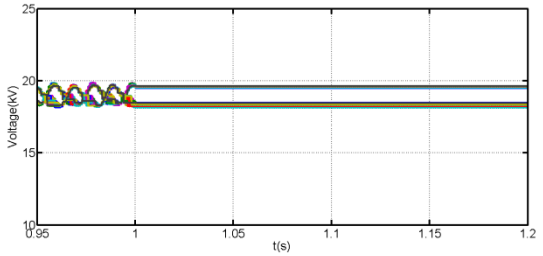
(i) MMC_{12} upper and lower arm currents (phase *a*)



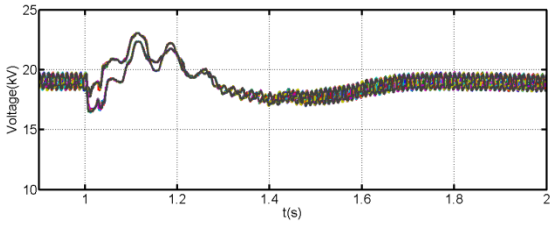
(j) MMC_{22} upper and lower arm currents (phase *a*)



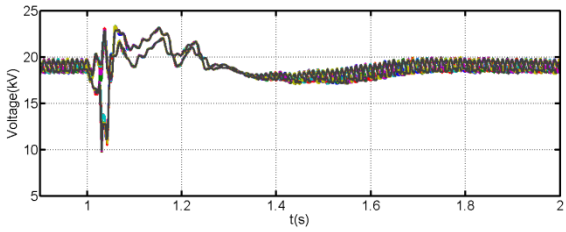
(k) MMC_{11} cell capacitor voltages (phase *a*)



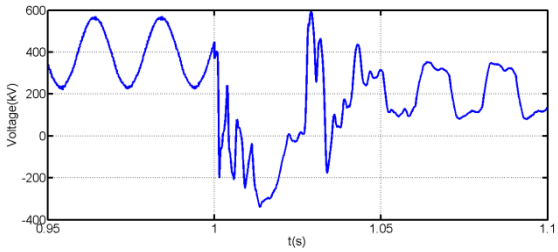
(l) MMC_{21} cell capacitor voltages (phase *a*)



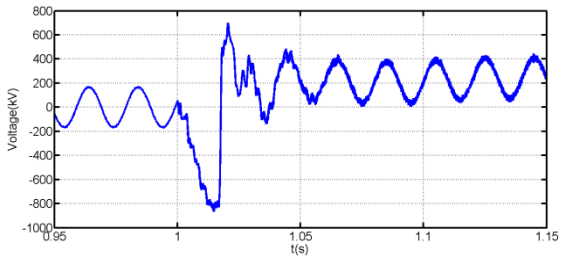
(m) MMC_{12} cell capacitor voltages (phase *a*)



(n) MMC_{22} cell capacitor voltages (phase *a*)



(o) MMC_{11} phase '*a*' output voltage measured relative to ground



(p) MMC_{12} phase '*a*' output voltage measured relative to ground

Figure 5: Waveforms for the tri-pole UHVDC link in Figure 4 during a permanent pole-to-ground dc fault at point 'F'.

C) Topology B - tri-pole HVDC link

Figure 7 show results when a point-to-point tri-pole HVDC link with a common metallic return in Figure 6, is subjected at a pole-to-ground dc fault at t=1s and is cleared after 20ms by opening of dc circuit breakers CB_{11} and CB_{12}. MMC_{11} and MMC_{21} are blocked immediately when the fault is detected and output power of MMC_{11} is reduced permanently to zero. Pre-fault operating conditions of the test system in Figure 6 are identical to those in Figure 4.

Figure 7 (a) shows pole-to ground dc voltages (V_{dp2}, V_{dm2} and V_{dn2}) measured at the terminals of Station 2 relative to ground. Topology B, a tri-pole HVDC link, does not expose the dc lines to excessive dc voltage stresses as observed with topology A, but exposes converter switches to higher current stress due to the asymmetric structure (there is no difference between pole-to-pole and pole-to-ground dc faults). Figure 7 (b) shows that the dc link currents measured at the terminals of station 1 have high peaks as during a typical pole-to-pole dc short circuit. With topology B, the current in the metallic return (I_{dc3}) is $-(I_{dc1}+I_{dc2}-I_{dc4})$ during normal operation, and falls to zero after topology B is reconfigured to a typical bi-pole HVDC link after the fault is cleared by opening dc circuit breakers CB_{11} and CB_{12} connected in the dc line of the upper pole (most positive pole). Figure 7 (c) to (f) and Figure 7 (g) to (j) show the output phase currents, and the upper and lower arm currents of the sub-converters

connected to the faulty and healthy poles of stations 1 and 2. These waveforms show that the converters connected to the healthy poles continued to exchange power between ac networks G_1 and G_2, including during the fault. The converters connected to the faulty pole survive with the current and voltage stresses on their active and passive components below that which would impose risk of damage, and this having been achieved with slow dc circuit breakers (current breaking time is assumed to be 20ms). Figure 7 (k) to (n) show that the cell capacitor voltages of all the sub-converters of the faulty and healthy poles are maintained and settle around the nominal steady state settling point. The phase voltages of the faulty and healthy poles converters displayed in Figure 7 (o) and (p) show that all the sub-converters of the healthy and faulty poles expose the interfacing transformer to a fixed dc voltage stress of half the dc link voltage as in typical asymmetric mono-pole HVDC links, even during the dc fault.

This discussion highlights that topology B of the tri-pole of HVDC link offers a suitable means for bulk power evacuation, without incurring high dc link voltages and without the risk of interfacing transformer insulation breakdown during a dc fault, unlike topology A; but it has higher transmission losses than topology A.

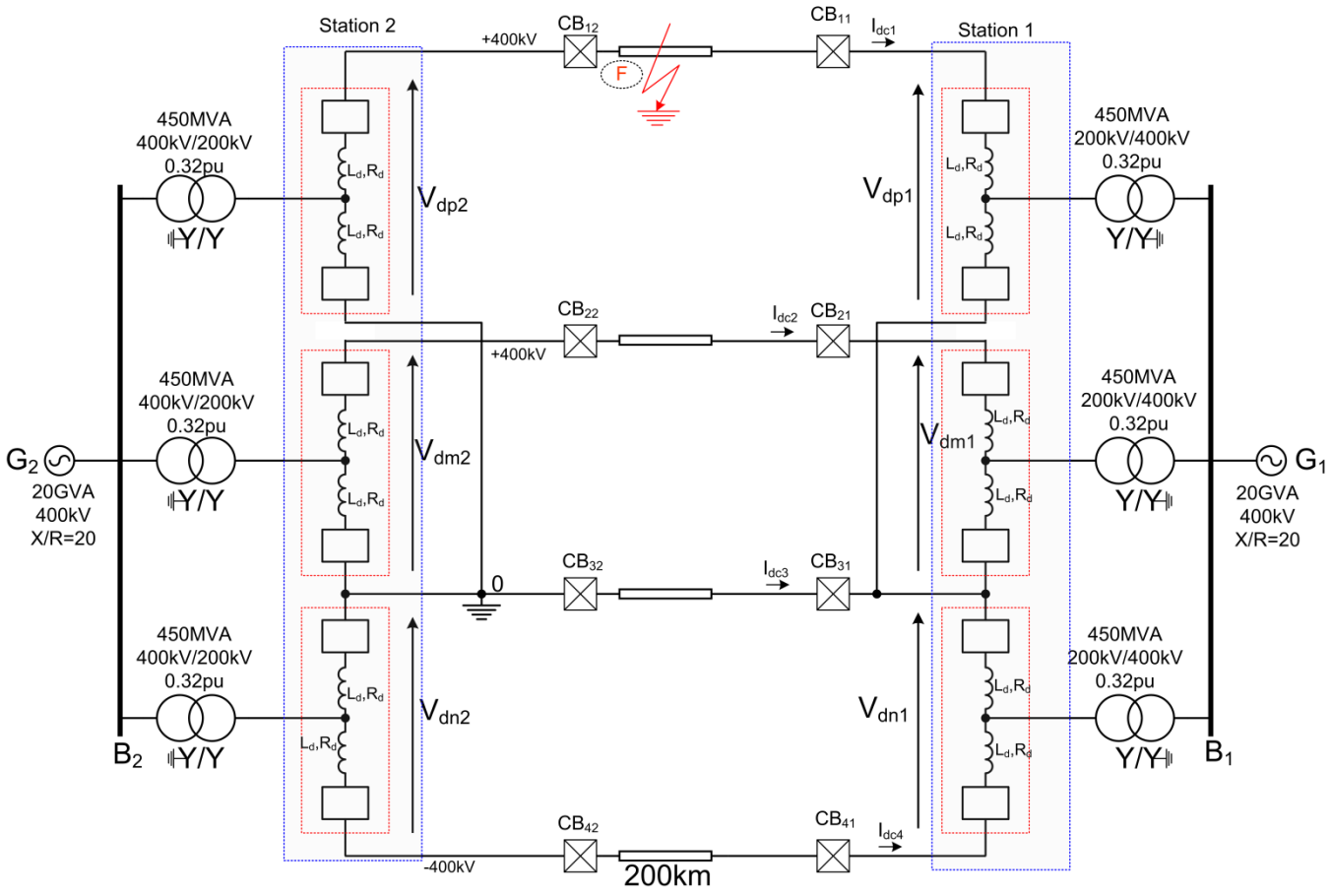
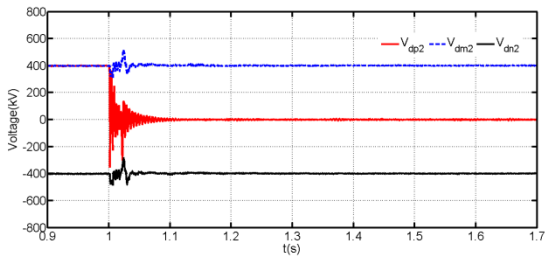
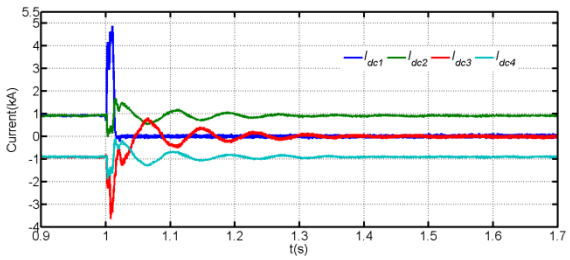


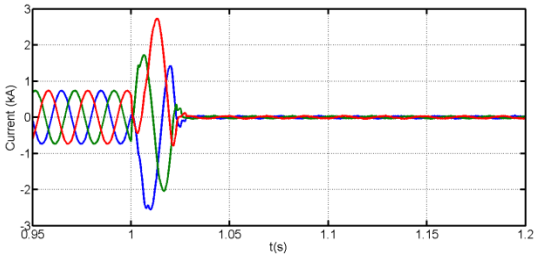
Figure 6: Point-to-point tri-pole HVDC link (Topology B).



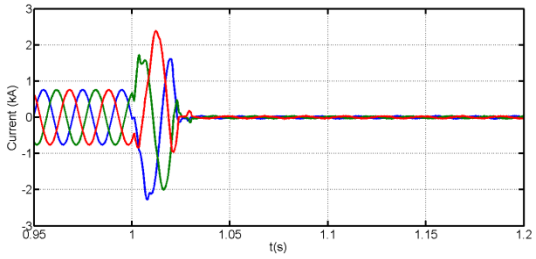
(a) DC link voltages (V_{dp2}, V_{dm2} and V_{dn2}) measured relative to ground



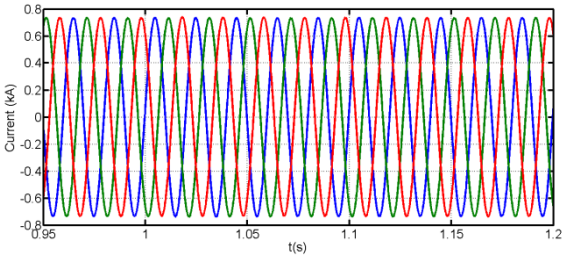
(b) DC link currents measured at the terminals of Station 2



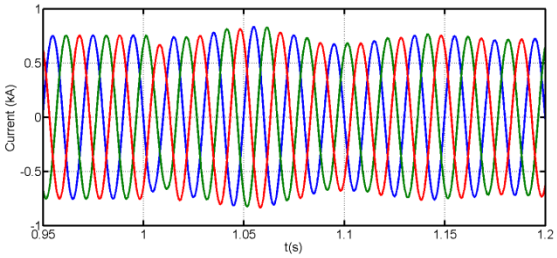
(c) Current waveforms sub-converter MMC_{11} exchanges with ac grid G_1



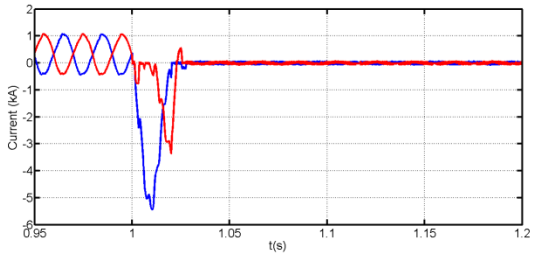
(d) Current waveforms sub-converter MMC_{21} exchanges with ac grid G_2



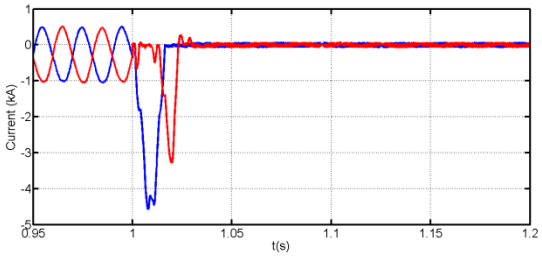
(e) Current waveforms sub-converter MMC_{12} exchanges with ac grid G_1



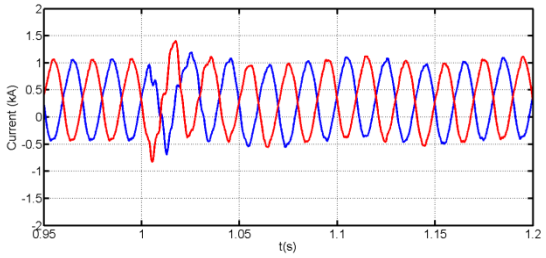
(f) Current waveforms sub-converter MMC_{22} exchanges with ac grid G_2



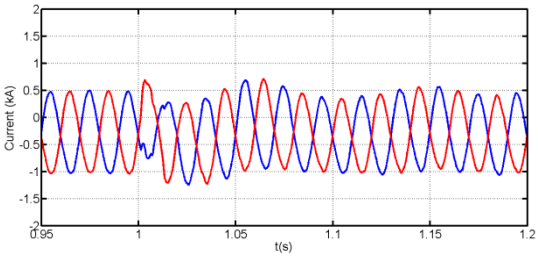
(g) MMC_{11} upper and lower arm currents



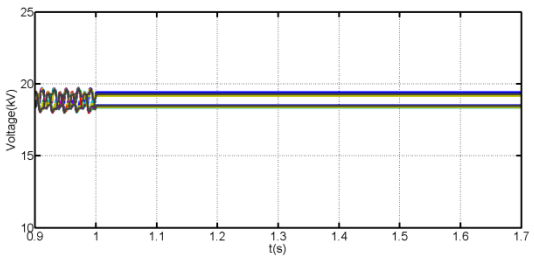
(h) MMC_{21} upper and lower arm currents



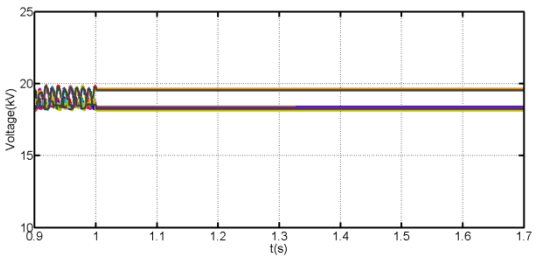
(i) MMC_{12} upper and lower arm currents



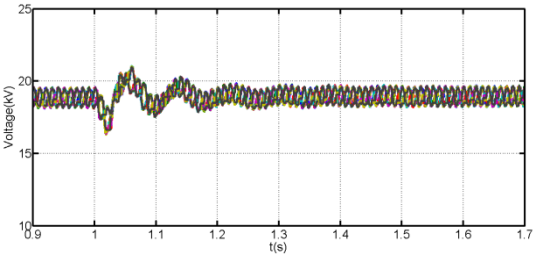
(j) MMC_{22} upper and lower arm currents



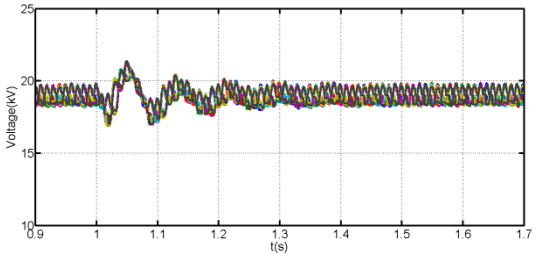
(k) MMC_{11} cell capacitor voltages



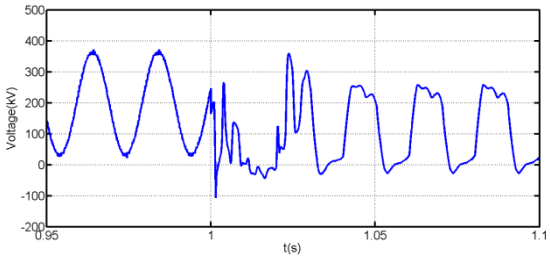
(l) MMC_{21} cell capacitor voltages



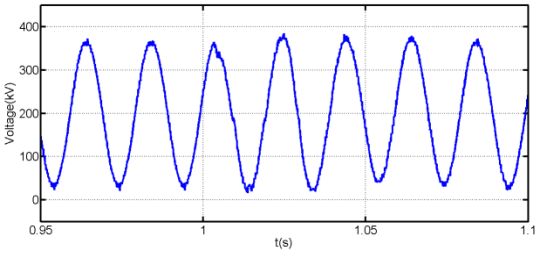
(m) MMC_{12} cell capacitor voltages



(n) MMC_{22} cell capacitor voltages



(o) Sample of the phase output voltage MMC_{11} presents to low-voltage side of its interfacing transformer



(p) Sample of the phase output voltage MMC_{12} presents to low-voltage side of its interfacing transformer

Figure 7: Waveforms of the tri-pole UHVDC link in Figure 6 during a permanent pole-to-ground dc fault at point 'F'.

V. CONCLUSIONS

This paper presented two multi-pole VSC-HVDC link network topologies, which are suitable for bulk power transmission over long distances, which offer system resilience to ac and dc network faults. The proposed network topologies resemble a symmetrical UHVDC link and asymmetrical HVDC link, suitable for overhead lines and subsea/underground cable transmission systems respectively. The technical feasibility of both network topologies were assessed on symmetrical and asymmetrical tri-pole HVDC links using Matlab-Simulink simulations. Beside bulk power evacuation, both network topologies offer reduced transmission losses compared to multiple parallel point-to-point VSC-HVDC links. The proposed multi-pole systems are suited for transnational multi-terminal HVDC grids as they offer the following features:

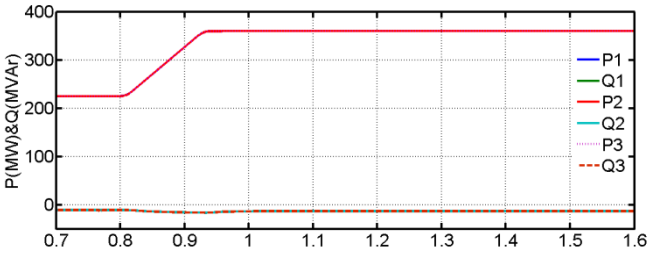
- Seamless dc network reconfiguration, with arbitrary possibility to re-route dc power between different poles;
- Inner poles of the symmetrical version offer the possibility for line tapping, without a dc voltage matching device, such as dc transformer.
- Prevention of uncontrolled fault propagation within the dc grid during a dc fault; and

- Loss of total power transfer due to a dc fault or (dc line or converter) outage is avoidable, except in exception situations such as simultaneous faults.

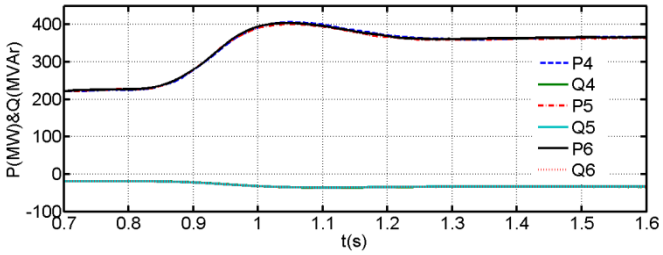
VI. APPENDIX

This appendix illustrates the internal dynamics of the symmetric tri-pole UHVDC link in Figure 4 when the active power set-points of the sub-converters of Station 1 are varied. Figure 8 shows waveforms when the active power set-point of each sub-converter of Station 1 is increased from 225MW (0.5pu) and 360MW (0.8pu), with the active power rate of change limited to 2.5pu/s. Figure 8(a) and (b) show the active and reactive powers each sub-converter of stations 1 and 2 exchange with their points of common coupling B_1 and B_2. The sub-converters of each station contribute equal reactive power to support the voltages at B_1 and B_2. But small differences are observed in the reactive power contribution of each sub-converter, should their interfacing transformers have different leakage inductances. Figure 8(c) and (d) show phase '*a*' upper and lower arm currents of the sub-converters of stations 1 and 2, with their corresponding common-mode currents in Figure 8(e) and (f).

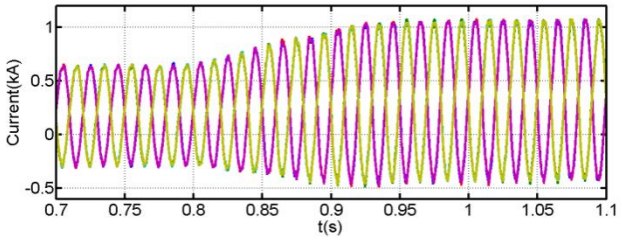
The common-mode currents of the sub-converters of stations 1 and 2 (normalised by peak phase current) and the dc currents in the four dc cables of the symmetric tri-pole UHVDC in Figure 8(g), (h) and (i) show that the instantaneous errors between the common-mode currents of sub-converters of this topology do not lead to significant circulating currents in the two middle dc cables. The maximum error in the common-mode currents between the sub-converters of both stations is less than 5%, with practically zero current in the two middle dc cables (before and after change of set-points). These results show that the inclusion of an additional control loop for current balancing between the poles, as with bipolar LCC-HVDC links is over-regulation, with no benefits; especially as the main benefit of the proposed symmetric tri-pole UHVDC link being discussed is its ability to use the two outer dc cables to transmit the total power, with zero current in the two inner dc cables. This discussion show that unequal loading of the individual poles of the symmetric tri-pole UHVDC link being studied contradicts its main purpose and compromises its utilization as a power corridor for bulk power evacuation.



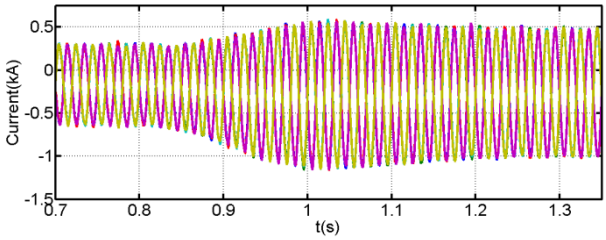
(a) Active and reactive powers sub-converters of Station 1 exchange with ac grid G_1 measured at B_1 (sub-converters that control active power)



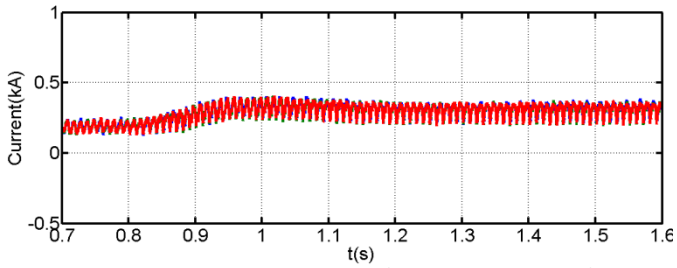
(b) Active and reactive powers sub-converters of Station 2 exchange with ac grid G_2 measured at B_2 (sub-converters that control dc voltage)



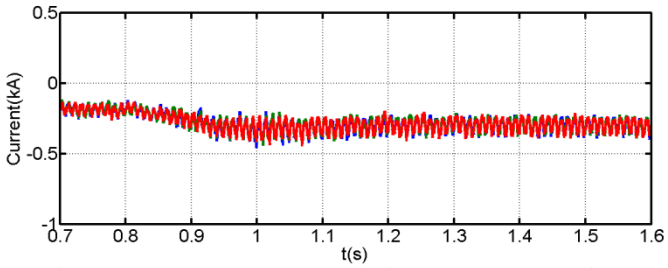
(c) Phase a upper and lower arm currents of three sub-converters of Station 1



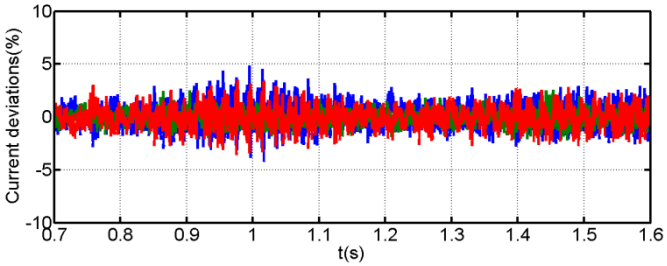
(d) Phase a upper and lower arm currents of three sub-converters of Station 2



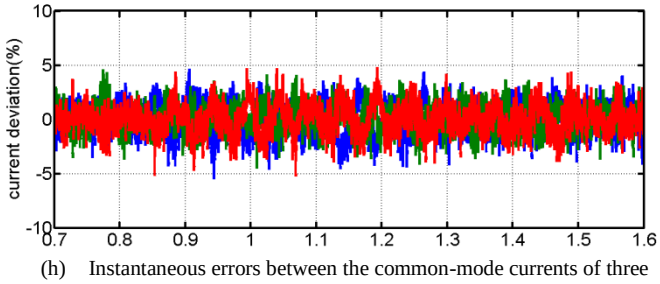
(e) Phase a common-mode currents of three sub-converters of Station 1 (i_{com1}=½(i_{a11}+i_{a12}), i_{com2}=½(i_{a21}+i_{a22}) and i_{com3}=½(i_{a31}+i_{a32}))



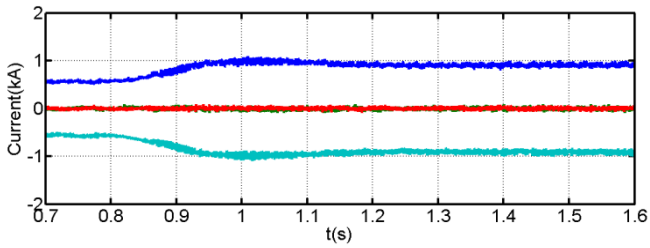
(f) Phase a common-mode currents of three sub-converters of Station 2 (i_{com4}=½(i_{a41}+i_{a42}), i_{com5}=½(i_{a51}+i_{a52}) and i_{com6}=½(i_{a61}+i_{a62}))



(g) Instantaneous errors between the common-mode currents of three sub-converters of Station 1 normalized by peak of the phase current ($\Delta i_{com12}=(i_{com1}-i_{com2})/I_{m1}\times100\%$, $\Delta i_{com23}=(i_{com2}-i_{com3})/I_{m1}\times100\%$and $\Delta i_{com31}=(i_{com3}-i_{com1})/I_{m1}\times100\%$)



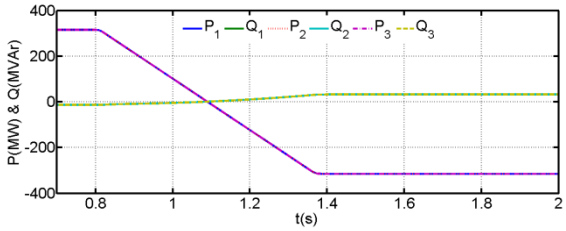
(h) Instantaneous errors between the common-mode currents of three sub-converters of Station 2 normalized by peak of the phase current ($\Delta i_{com45}=(i_{com4}-i_{com5})/I_{m2}\times100\%$, $\Delta i_{com56}=(i_{com5}-i_{com6})//I_{m2}\times100\%$and $\Delta i_{com64}=(i_{com6}-i_{com4})/I_{m2}\times100\%$)



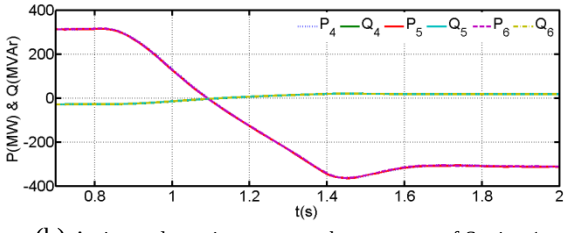
(i) DC currents in the four cables of the symmetrical tri-pole UHVDC link

Figure 8: Waveforms when the active power set-point of each sub-converter of Station 1 is increased from 225MW (0.5pu) to 360MW(0.8pu), where i_{aj1} and i_{aj2} represent phase '*a*' upper and lower arm currents of sub-converter '*j*' and '*j*' is a positive integer 1 to 6.

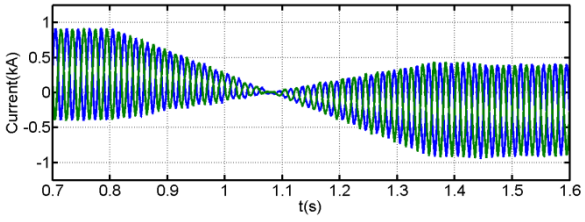
Figure 9 presents selected waveforms that illustrate internal dynamics of symmetric tri-pole UHVDC link when station 1 initiates a power reversal at *t=0.8s*, with magnitude and direction of initial power flow are 315MW and from G_1 to G_2. These waveforms show that the symmetric tri-pole UHVDC link being studied exhibits satisfactory performance during power reversal, and these results are in line with initial results of step change in power command of station 1 presented in Figure 8, see Figure 9 (a) to (e).



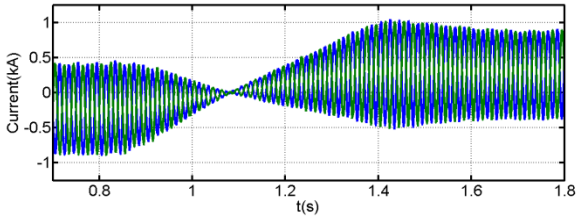
(a) Active and reactive powers sub-converters of Station 1 exchange with ac grid G_1 measured at B_1



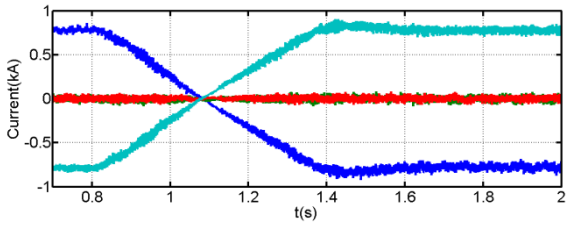
(b) Active and reactive powers sub-converters of Station 1 exchange with ac grid G_2 measured at B_2



(c) Phase a upper and lower arm currents of three sub-converters of Station 1



(d) Phase a upper and lower arm currents of three sub-converters of Station 2



(e) DC currents in the four cables of the symmetrical tri-pole UHVDC link

Figure 9: Waveforms when illustrate internal dynamics of the symmetrical tri-pole UHVDC during power reversal (the active power set-point of each sub-converters of Station 1 is changed from 315MW (0.7pu) to -315MW(0.7pu)

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