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Generation, Performance Evaluation and Control Design of Single-phase Buck-boost Differential-mode Current Source Inverters

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Abstract: Differential-mode inverter topologies are promising for renewable energy generation as they offer merits such as reduced size of passive elements, high power density, and reduced total cost. Single-phase buck-boost differential-mode current source inverters (DMCSI) can provide flexible output voltage above or below the input dc voltage, which is necessary for higher efficiency of modern renewable energy applications. The continuous input current of a DMCSI is appropriate for maximum power point tracking operation (MPPT) of photovoltaic applications. However, the performance and control of such converters has not been discussed in detail. As a drawback, the total dc side input current of a single-phase inverter consists of a desired dc component and an undesirable ac component. This ac current component frequency is double the output voltage frequency and thus, affects MPPT resulting in reduced total efficiency. In this paper, five possible DMCSIs are proposed and compared in terms of total losses, maximum ripple current, total harmonic distortion, devices and passive element ratings. In addition, the sliding mode controller's design and possible methods of eliminating the input 2nd harmonic current are discussed. A 2.5kW bidirectional inverter is used to validate the design flexibility of the five inverters topologies.

1. Introduction

There is mounting international proclivity to reduce the cost and improve the efficiency of energy conversion systems through modular structured renewable/distributed systems [1]. Therefore, the need for reducing converter size and passive component values is pressing. Moreover, the cost of photovoltaic (PV) systems is affected considerably by installation and maintenance costs [2]. The inverter initial and running costs may reach about half the initial PV system cost [3].

Most dc-ac converters installed in PV systems require large input filtering capacitance, typically wet electrolytic types. Replacing this electrolytic capacitor with a plastic type increases reliability significantly as it is at least thirty times more reliable than electrolytic types, at the same operating conditions [4]. At rated operating conditions, the life time of an electrolytic filter capacitor is short compared with other inverter components [5]. Thus, using this capacitor hampers increased overall system reliability. The life time of a capacitor is halved for every 10^{o}C increase in the operating temperature [6].

For dc-ac conversion, the voltage source inverter (VSI) is the most common converter topology where the output ac voltage peak is always lower than the input dc voltage and the output ac current peak is always greater than the input dc current [7, 8]. Because of the VSI buck nature, a boost dc-dc converter may be installed between the PV and the inverters input for voltage matching and maximum power point tracking (MPPT) control. Consequently, system volume, weight, power losses, and cost are increased [9,

10]. Myrzik [11] classified the single-stage buck and boost inverter topologies, while in [12], buck-boost Z-source inverter topologies were proposed and explained.

If two power converters are connected in a parallel-series configuration, they form a differential-mode inverter. Some of these differential mode inverters types are shown in [9], [13, 14]. The basic structure of a differential-mode buck-boost single-phase inverter is shown in Fig.1. The differential-mode inverter initially appeared in [13] as a boost inverter, while a differential buck inverter is presented in [15]. Knight et al. [2] proposed the differential six-switch buck-boost inverter based on the Ćuk converter, but its performance was not evaluated.

Of the known two-switch two-diode buck-boost reversible converters, there are five converters that can provide continuous input currents and hence, mitigate the need for large electrolytic input capacitors. These buck-boost converters are shown in [16] as C5, D1, D2, F5 and G5 and can be used as building blocks in a differential-mode current source inverter (DMCSI). Besides eliminating an unreliable large electrolytic capacitor, continuous input current switched mode power supplies (SMPS) enable safe and reliable converter-grid connection and they are attractive solutions for energy conversion systems in terms of: 1) voltage buck-boost operation with a flexible output voltage range, 2) continuous input current, 3) high efficiency, and 4) high frequency transformer coupling possibilities.

Generally, continuous input current converters are time variant systems where the overall transfer function describing the relation between the input and output voltages and currents depend on the switching periods of its switches. This results in a complex stable design because the converter poles and zeros travel through a long Nyquist trajectory [9], [17, 18].

In single-phase inverters, the output power demand reflects into the input side and implies that the input current or voltage, or both, carry a 2^{nd} harmonic component [19]. For renewable energy sources, this component would affect MPPT performance and decreases the average power from the system. The conventional solution for the harmonics in the input dc current is to use a large inductor which attenuates the even-order harmonics [20]. However, this is not a practical solution as the inverter produces high dc current which requires a large, bulky input inductor. Research has been conducted into eliminating the oscillating input current of a single-phase PV inverter, and can be classified into two categories: 1) passive elimination with passive circuits and 2) active elimination circuits with semiconductor devices [21]. An example of passive elimination is presented in [22] where a second order LC circuit is used as a notch filter. Although such circuits can reduce the even harmonics from the input side, they have two main drawbacks. Firstly, in time, deviation in the passive element component values results in reduced even harmonic attenuation. Secondly, the capacitor in the PV current path results in a discontinuous current

component which requires another stage of filtering. An active harmonic suppression technique is presented in [23], where the 2nd order harmonic of the input current is eliminated by a series buffer converter topology.

This paper presents the generation of single-phase buck-boost DMCSIs from their building dc-dc blocks, proposes proper control design for each topology, and compares the possible DMCSI topologies in terms of features such as efficiency, input current ripple, output current total harmonic distortion (THD), and device and capacitor ratings. Also the paper presents possible methods for decoupling the 2nd order harmonic current components in the proposed DMCSIs with and without extra power electronic switches and discusses their effect on passive element sizes.

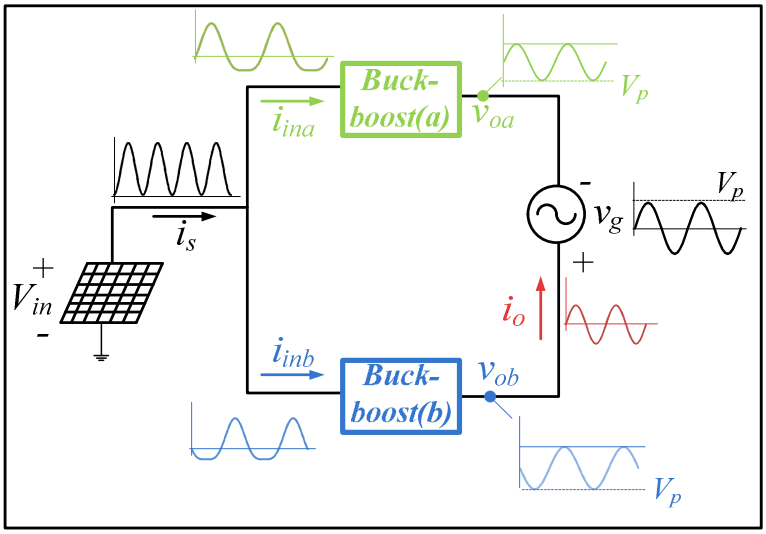


Fig.1. *Basic structure of a buck-boost DMCSI.*

2. System description

The input voltage dc source is connected to two bidirectional buck-boost converters as shown in Fig.1. Most buck-boost converters produce an output voltage which has an opposite polarity to the input voltage. Each converter produces unipolar voltage where:

$$v_{oa}(t) = -h_a V_{in}$$
$$h_a = H_{dc} + H_{ac}\sin\omega t \qquad (1a)$$
$$v_{oa}(t) = -\tfrac{1}{2}\ V_p\ [1+\sin\omega t]$$

$$v_{ob}(t) = -h_b \cdot V_{in}$$
$$h_b(t) = H_{dc} + H_{ac}\sin(\omega t - \pi) \qquad (1b)$$
$$v_{ob}(t) = -\tfrac{1}{2}\ V_p\ [1+\sin(\omega t - \pi)]$$

The output voltage v_g and current i_o are:

$$v_g(t) = v_{ob} - v_{oa} = V_p \sin \omega t$$
$$i_o(t) = I_o \sin(\omega t + \gamma) \quad (1c)$$

The basic dc-dc converters with continuous input currents are shown in Fig. *2*. All are reversible when using two switch-diode pairs. For all these converters, the power is transferred from the input to the output side (or in the opposite direction) through a capacitor *C* while storing energy in the input and output inductors $L_1$and L_2. For converters C5, D1 and D2, the output shunt capacitor C_o is optional (converters the output to a voltage source) as the output current is continuous. However, C_o is mandatory for converters G5 and F5 (in order to average the output voltage). For all the converters, the switch and diode (S_1 and D_2) operate alternately when the power is transferred from the input to the output and the switch and diode (S_2 *and* D_1) operate alternately when power is transferred in the opposite direction. t_{on} is the period when S_1 *or* D_1 conduct current while t_{off} is the period where S_2 *or* D_2 conduct.

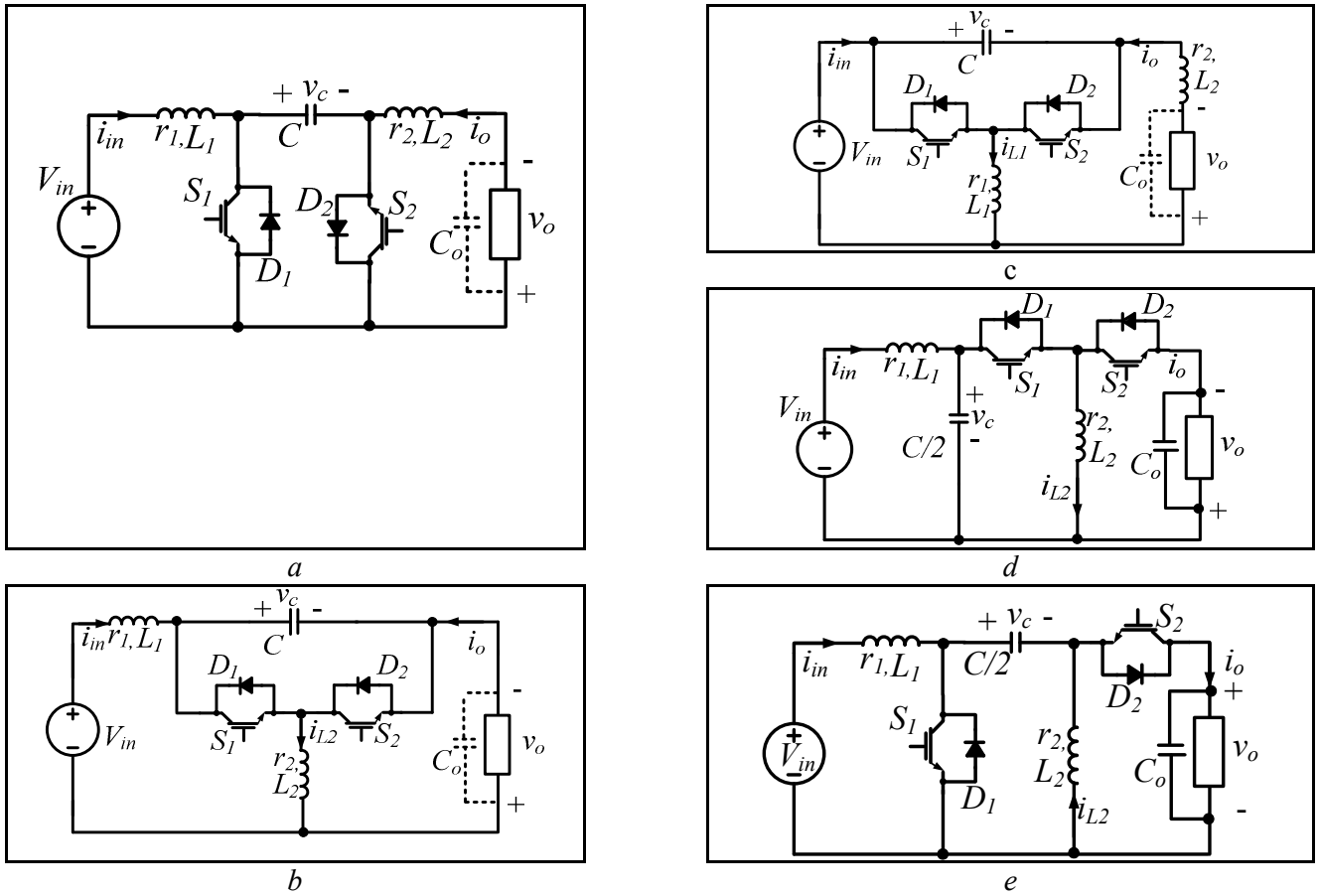


Fig. 2. *Buck-boost converters with continous input current:* **(a) C5 (*Ćuk*), (b) D1, (c) D2, (d) F5, and (e) G5 (sepic).**

The switch on-state duty ratio of the converters δ is:

$$\delta = \frac{t_{on}}{t_s} \quad (2a)$$

The voltage conversion ratio between the output and input voltages (h) can be expressed as:

$$h = \frac{v_o}{V_{in}} = \frac{\delta}{1-\delta} = \frac{i_{in}}{i_o} \tag{2b}$$

The five buck-boost converters can be inserted into the configuration blocks in Fig.1. The time varying duty ratios of the converters can be deduced from the desired output voltages as:

$$\delta_a(t) = \frac{h_a}{h_a + 1} \text{ and } \delta_b(t) = \frac{h_b}{h_b + 1} \tag{3}$$

3. Converter performance comparison

In this section, the five single-phase buck-boost DMCSIs are discussed and compared in terms of: 1) overall efficiency, 2) input current ripple, 3) switch and diode currents and voltages, 4) output current THD, and 5) capacitors voltage stresses. To avoid duplication and prolongation, the mathematical analysis for only the C5 (*Ćuk*) converter will be presented in detail while the final conclusions for the remaining four converters will be summarised.

3.1. Power Losses

Two significant loss sources will be considered in this analysis. The first is the copper (I^2R) loss in the input and output inductors and the second is converter semiconductor device losses. Consequently, the root mean square (rms) currents in the inductors as well as the average current in the diodes should be derived. The currents through inductors L_1 and L_2 can be expressed as functions of the output current, voltage and duty ratios as shown in Table 1.

Table 1 Currents through the converter's inductors

Topology	Current through L_1	Current through L_2
C5	$i_{in} = \frac{\delta}{1-\delta} i_o$	i_o
D1	$i_{in} = \frac{\delta}{1-\delta} i_o$	$i_{L2} = \frac{1}{1-\delta} i_o$
D2	$i_{L1} = \frac{1}{1-\delta} i_o$	$i_{L2} = i_o$
F5	$i_{in} = \frac{\delta}{1-\delta} i_o$	$i_{L2} = \frac{1}{1-\delta} i_o$
G5	$i_{in} = \frac{\delta}{1-\delta} i_o$	i_o

$\frac{1}{1-\delta}$ is always greater than 1 while $\frac{\delta}{1-\delta}$ is greater than 1 when δ> 0.5 and less than 1 when δ< 0.5.

For C5 converters, as an example, the instantaneous input current i_{ina} and i_{inb} of each converter is:

$$\frac{i_{ina}(t)}{i_o(t)} = \frac{v_{oa}}{V_{in}} = \frac{\delta_a}{1-\delta_a}, \quad \frac{i_{inb}(t)}{i_o(t)} = \frac{v_{ob}}{V_{in}} = \frac{\delta_b}{1-\delta_b} \tag{4a}$$

$$\begin{aligned} i_{ina}(t) &= \tfrac{1}{2}[\frac{V_p}{V_{in}} + \frac{V_p}{V_{in}}\sin\omega t\,]\, I_o \sin(\omega t + \gamma) \\ &= \frac{V_p I_o}{2V_{in}}\{\tfrac{1}{2}\cos\gamma + \tfrac{1}{2}\cos(2\omega t + \gamma) + \sin(\omega t + \gamma)\} \end{aligned} \tag{4b}$$

$$\begin{aligned} i_{inb}(t) &= \tfrac{1}{2}[\frac{V_p}{V_{in}} + \frac{V_p}{V_{in}}\sin(\omega t + \pi)]\, I_o \sin(\omega t + \pi + \gamma) \\ &= \frac{V_p I_o}{2V_{in}}\{\tfrac{1}{2}\cos\gamma + \tfrac{1}{2}\cos(2\omega t + \gamma) + \sin(\omega t + \gamma + \pi)\} \end{aligned} \tag{4c}$$

The inputs current i_{ina} and i_{inb} are rewritten as:

$$\begin{aligned} i_{ina}(t) &= \bar{I}_{in} + I_{in1}\sin(\omega t + \gamma) + I_{in2}\cos(2\omega t + \gamma) \\ i_{inb}(t) &= \bar{I}_{in} + I_{in1}\sin(\omega t + \gamma + \pi) + I_{in2}\cos(2\omega t + \gamma) \\ \bar{I}_{in} &= \tfrac{1}{4}\frac{V_p I_o}{V_{in}}\cos\gamma \\ I_{in1} &= \tfrac{1}{2}\frac{V_p I_o}{V_{in}} \\ I_{in2} &= \tfrac{1}{4}\frac{V_p I_o}{V_{in}} \end{aligned} \tag{5}$$

If the parasitic resistances of the inductors (L_1 and L_2) are assumed as r_1 and r_2, the copper losses are:

$$\begin{aligned} P_{loss\_in} &= (\bar{I}_{in}^{\,2} + \tfrac{1}{2}I_{in1^2} + \tfrac{1}{2}I_{in2^2})r_1 \\ P_{loss\_out} &= \tfrac{1}{2}I_o^2 r_2 \end{aligned} \tag{6}$$

The power losses through the switches can be approximated as:

$$P_{sw} = V_{DF}\bar{i}_D + R_{on}I_{rms}^2$$

where

$$I_{rms} \approx \sqrt{\frac{3\delta_{av}I_o^{\,2}}{2}(\frac{H_{dc}^{\,2}}{4} + \frac{3H_{ac}^{\,2}}{16})}, \quad \delta_{av} \approx \frac{1.3H_{dc}}{H_{dc} + H_{ac} + 1} \tag{7}$$

$$\bar{i}_{D1} = \frac{I_{in1}}{\pi} - \tfrac{1}{2}\bar{I}_{in}, \qquad \bar{i}_{D2} = \frac{I_o}{\pi}$$

where V_{DF} is the diode forward threshold voltage and R_{on} is the device dynamic resistance.

The total power loss of each inverter is:

$$P_{total} = 2[P_{loss\_in} + P_{loss\_out} + P_{sw}] \quad (8)$$

and the inverter efficiency is:

$$\eta = \frac{V_p I_o}{V_p I_o + P_{total}} \times 100 \quad (9)$$

The switches power losses in the five inverter types are the same as they all have identical current and voltage waveforms. The copper losses as well as device average voltage and current are summarized in Table 2.

Table 2 Copper losses and switch operating conditions

Type	Copper losses x r		Switch averages			
			S_1 and D_1		S_2 and D_2	
	L_1	L_2	Voltage	Current	Voltage	Current
C5	$\frac{3V_p^2 I_o^2}{16V_{in}^2}$	$\frac{I_o^2}{2}$	V_{in}	$\frac{V_p I_o}{2\pi V_{in}} - \frac{V_p I_o}{8V_{in}}$	$\frac{2V_p}{\pi}$	$\frac{I_o}{\pi}$
G5	$\frac{3V_p^2 I_o^2}{16V_{in}^2}$	$\frac{I_o^2}{2}$	″	″	″	″
D1	$\frac{3V_p^2 I_o^2}{16V_{in}^2}$	$\frac{V_p^2 I_o^2}{8V_{in}^2} + I_o^2(\frac{V_p}{2V_{in}} + 1)$	″	″	″	″
D2	$\frac{V_p^2 I_o^2}{8V_{in}^2} + I_o^2(\frac{V_p}{2V_{in}} + 1)$	$\frac{I_o^2}{2}$	″	″	″	″
F5	$\frac{3V_p^2 I_o^2}{16V_{in}^2}$	$\frac{I_o^2}{2}$	″	″	″	″

Table 3 Parasitic component values and circuit conditions

Parameter	Value
Rated power	2.5 kW
Switching frequency	f_s = 50 kHz
Input inductor	L_1 = 1mH, r_1 = 80 mΩ
Output inductor	L_2 = 1mH, r_2 = 80 mΩ
Input voltage	V_{in} = 100 V
Output voltage	V_p = 200 V
Output current angle	γ = 0º
Diode forward voltage	V_{DF} = 2V
Transfer capacitor	C = 20μF
Output capacitor (G5 and F5)	C_o = 10μF

A MATLAB simulation for the efficiencies of the five inverters at different input voltages and output currents with the inverter parasitic values is shown in Fig. 3a. C5 and G5 inverters have the highest efficiency. The efficiencies of D1 and F5 are better than D2 in the high input voltage region while D2 is

better than both when the input voltage is low. Generally, the efficiency of all inverters decreases as the input voltage decreases (since semiconductor voltage drops become more significant).

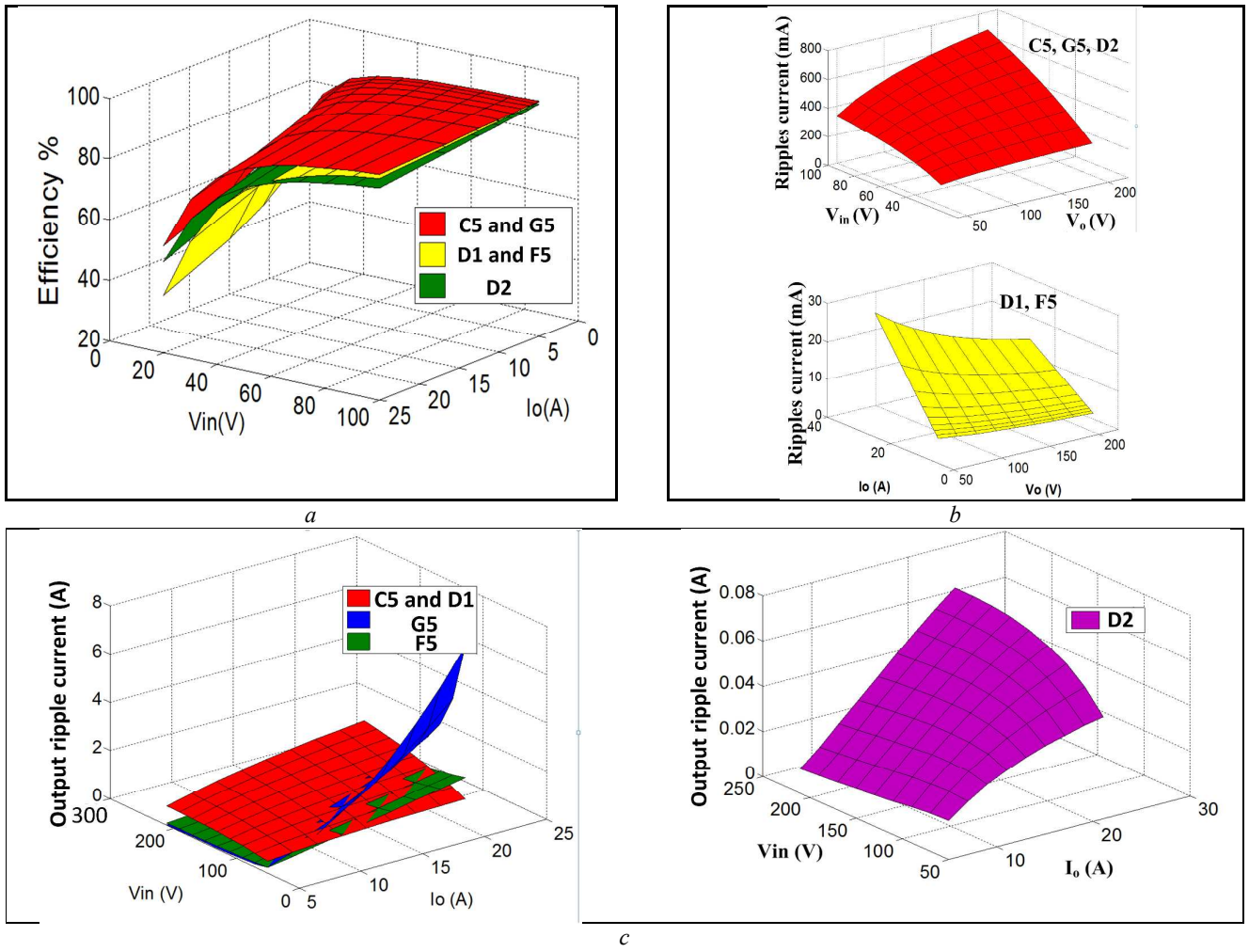


Fig. 3. *MATLAB simulation of DMCSIs:* **(a) efficiency, (b) input current ripple ΔI_{in}, and (c) output current ripple ΔI_o**

3.2 Input current ripple

Input current ripple is the maximum change of the instantaneous current around its average value. For energy conversion applications like PV, fuel cells, etc., ripple causes harmonics and power loss in the overall system, so should be reduced. Ref [24] demonstrates that input current and voltage ripple inversely affects the total power extracted from PV systems. In the structure in Fig.1, the input current ripple is not constant and changes during the 50/60Hz current cycle. The maximum current ripple occurs at the peak value of the converter's duty ratio. The maximum ripple current for the different inverters are presented in Table 4. Fig. 3b shows plots of maximum ripple currents at different operating conditions. C5, G5 and D2 converters have the same input current ripple versus input and output voltage. Both D1 and F5 have the

same input current ripple versus output current and voltage. As an important advantage, the ripple contents of the input current i_{in} in D1 and F5 are small compared with the other DMCSIs.

Table 4 Maximum Input current ripple

Topology		normalised
C5	$\frac{V_p V_{in} t_s}{L_1(V_p + V_{in})}$	1
D1	$\frac{V_p V_{in} I_o {t_s}^2}{4L_1 C(V_p+V_{in})^2}$	$\frac{I_o t_s}{4C(V_p + V_{in})}$
D2	$\frac{V_p V_{in} t_s}{L_1(V_p + V_{in})}$	1
F5	$\frac{V_p V_{in} I_o {t_s}^2}{4L_1 C(V_p+V_{in})^2}$	$\frac{I_o t_s}{4C(V_p + V_{in})}$
G5	$\frac{V_p V_{in} t_s}{L_1(V_p + V_{in})}$	1

3.3 Output current ripple

The output current distortion can be classified into low frequency and high frequency distortion. Low order current distortion appears because of the non-linear nature and high system order of the proposed inverters and can be removed with appropriate control loops as discussed in [9]. The high frequency current and voltage ripple in the output side is because of the switching action. These high frequency ripple components are dependent on the converter topology the differential-inverter descends from. For the same passive element component values, the output current ripple can be expressed as in Table 5. The peak output current ripple ΔI_o of the different inverters are simulated in Fig. 3c. The high frequency ripple component of the output current I_o in D2 is insignificant compared with the other converters, with the same passive element values. This leads the DMCSI emerging from the D2 converter having lower total harmonic distortion (THD) than the other inverters, provided the low order current components are eliminated with proper controllers.

Table 5 Output current ripple

Topology		normalised
C5	$\frac{V_p V_{in} t_s}{L_2(V_p + V_{in})}$	1
D1	$\frac{V_p V_{in} t_s}{L_2(V_p + V_{in})}$	1
D2	$\frac{V_p V_{in} I_o {t_s}^2}{4L_2 C(V_p+V_{in})^2}$	$\frac{I_o t_s}{4C(V_p + V_{in})}$
F5	$\frac{V_{in} {I_o}^2 t_s}{C_o(V_p+V_{in})V_{in}}$	$\frac{I_o L_2}{4C_o V_{in}}$
G5	$\frac{V_p {I_o}^2 t_s}{C_o(V_p+V_{in})V_{in}}$	$\frac{I_o L_2}{4C_o(V_p + V_{in})}$

3.4 Capacitor C voltage stress

Knowledge of the voltage stresses on the energy transfer capacitor *C* is important for its selection. For some inverters, the voltage across *C* consists of a dc-bias plus a sinusoidal voltage component (fundamental) while for other converters, the voltage across *C* is only dc. Inverters using F5 and G5 have lower capacitor voltages stresses than C5, D1 and D2. Table 6 summarize the capacitor voltages stresses for each converter, in terms of the source voltage and differential sinusoidal output maximum voltage, V_p.

Table 6 Voltage stress across capacitor C (see Fig. 1)

Topology	dc-bias	Sinusoidal voltage (fundamental)	Peak Voltage
C5	$V_{in} + \frac{1}{2}V_p$	$\frac{1}{2}V_p \sin \omega t$	$V_{in} + V_p$
D1	$V_{in} + \frac{1}{2}V_p$	$\frac{1}{2}V_p \sin \omega t$	$V_{in} + V_p$
D2	$V_{in} + \frac{1}{2}V_p$	$\frac{1}{2}V_p \sin \omega t$	$V_{in} + V_p$
F5	V_{in}	≈0	V_{in}
G5	V_{in}	≈0	V_{in}

4. Control design

For several applications, buck-boost DMCSIs require robust, efficient and fast control methods. This is because each phase converter produces ac voltage superimposed on a dc bias voltage. Thus, the deviation of the output dc voltage component may cause output dc current components which are undesirable in the inverter systems. Because the proposed systems are of high order, variable structure control [25] (VSR) is an attractive control solution. In this section, sliding mode control (SMC) [25], which belongs to the family of VSR techniques, will be discussed when applied to the proposed DMCSIs. The mathematical

analysis will be presented in detail for the C5 based system and following the same approach, the final block diagrams and control equations will be stated for the other four inverter types. SMC forces the system states to track predefined trajectories which lie on the desired reference values [25]. SMC having fast dynamics and its robustness to system parameter and states variations are important features. The control structure aims to drive the inverter's output current i_o on a specified surface. First, the large signal average model of C5 converter can be obtained from the converter's differential equations in the *on* and *off* modes as follows (continuous conduction mode (CCM) of all passive reactive components is ensured because the converters are reversible):

i) S_1 *OFF* and S_2 *ON* ($0 < t < t_{off}$)

$$\begin{aligned} \frac{di_{in}}{dt} &= \frac{1}{L_1}V_{in} - \frac{r_1}{L_1}i_o - \frac{1}{L_1}v_c \\ \frac{dv_c}{dt} &= \frac{1}{C}i_{in} \\ \frac{di_o}{dt} &= -\frac{r_2}{L_2}i_o - \frac{1}{L_2}v_o \end{aligned} \tag{10}$$

ii) S_1 *ON* and S_2 *OFF* ($t_{off} < t < t_s$)

$$\begin{aligned} \frac{di_{in}}{dt} &= \frac{1}{L_1}V_{in} - \frac{r_1}{L_1}i_{in} \\ \frac{dv_c}{dt} &= \frac{1}{C}i_o \\ \frac{di_o}{dt} &= -\frac{1}{L_2}v_c - \frac{r_2}{L_2}i_o - \frac{1}{L_2}v_o \end{aligned} \tag{11}$$

The equations can be averaged over the switching time t_s as:

$$\begin{aligned} \frac{di_{in}}{dt} &= \frac{1}{L_1}V_{in} - \frac{r_1}{L_1}i_{in} - \frac{1-u}{L_1}v_c \\ \frac{dv_c}{dt} &= \frac{u}{C}i_{in} + \frac{1-u}{C}i_o \\ \frac{di_o}{dt} &= -\frac{u}{L_2}v_c - \frac{r_2}{L_2}i_o - \frac{1}{L_2}v_o \\ u &= \begin{cases} 1 & S_1 \text{ on} \\ 0 & S_1 \text{ off} \end{cases} \end{aligned} \tag{12}$$

By averaging the discrete variable u on t_s as $u_{eq} = \delta$, the average state space model in the continuous conduction mode CCM is:

$$\begin{bmatrix} \frac{di_{in}}{dt} \\ \frac{dv_c}{dt} \\ \frac{di_o}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{r_1}{L_1} & -\frac{(1-\delta)}{L_1} & 0 \\ \frac{(1-\delta)}{C} & 0 & \frac{\delta}{C} \\ 0 & \frac{\delta}{L_2} & -\frac{r_2}{L_2} \end{bmatrix} \begin{bmatrix} i_{in} \\ v_c \\ i_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & 0 \\ 0 & -\frac{1}{L_2} \end{bmatrix} \begin{bmatrix} V_{in} \\ v_o \end{bmatrix} \quad (13)$$

The C5 converter is not able to be controlled directly from the output current; only the input current can be directly controlled. This can be understood from the effect of the two switches S_1 and S_2 on the converters currents. For all the converters in Fig. 2, S_1 affects the input current i_{in} directly while S_2 has no direct effect on i_o. For this reason, the reference value of the converter output current is written in terms of i_{in}. The sliding surface 'S' can be chosen as:

$$S = \alpha_1 e_1 + \alpha_2 e_2 + \alpha_3 e_3 \quad (14a)$$

$$\dot{S} = \alpha_1 \dot{e}_1 + \alpha_2 \dot{e}_2 + \alpha_3 \dot{e}_3 = 0 \quad (14b)$$

where α_1, α_2 and α_3 are constants and e_1, $e_2$and e_3 are the controller error signals, written as:

$$\begin{aligned} e_1 &= i_{in}^* - i_{in} \\ e_2 &= i_o^* - i_o \\ e_3 &= \int (e_1 + e_2) dt \end{aligned} \quad (15a)$$

$$\begin{aligned} \dot{e}_1 &= \frac{di_{in}^*}{dt} - \frac{di_{in}}{dt} \\ \dot{e}_2 &= \frac{di_o^*}{dt} - \frac{di_o}{dt} \\ \dot{e}_3 &= e_1 + e_2 \end{aligned} \quad (15b)$$

For the pre-stated controllability issues, the reference input current i^*_{in} is re-written as:

$$i_{in}^* = K(i_o^* - i_o) \quad (16)$$

where K is a control constant. If the frequency of i^*_o is assumed small compared to the switching frequency, i^*_o can be considered constant during one switching period and its derivative can be considered as zero. Substituting (13) and (16) into (15a) yields:

$$\begin{aligned} \dot{e}_1 &= \frac{-1}{L_1} V_{in} + i_{in} \frac{r_1}{L_1} + v_c \left(-\frac{K\delta}{L_2} + \frac{(1-\delta)}{L_1}\right) + i_o \frac{K r_2}{L_2} + v_o \frac{K}{L_2} \\ \dot{e}_2 &= -\frac{\delta}{L_2} v_c + i_o \frac{r_2}{L_2} + v_o \frac{1}{L_2} \\ \dot{e}_3 &= (K+1)(i_o^* - i_o) - i_{in} \end{aligned} \quad (17)$$

Substituting (17) into (14a) and solving for δ gives:

$$u_{eq} = \delta = \frac{-V_{in} + i_{in}(r_1 - K_1) + v_c + i_o(K_2 r_2) + v_o K_2 + K_3(i^*_o - i_o)}{v_c(1 + K_2)}$$

$$K_1 = \frac{\alpha_3}{\alpha_1} L_1, \quad K_2 = \frac{K\alpha_1 + \alpha_2}{L_2 \alpha_1} L_1, \text{ and } K_3 = \frac{(K+1)\alpha_3}{\alpha_1} L_1 \quad (18)$$

The resultant sliding mode controller from (18) is shown in **Error! Reference source not found.**a.

The controller gains K_1, K_2 and K_3 are responsible for steady state regulation, oscillation and settling time. The designer has three degrees of freedom to choose the gain values. However, it must be confirmed that these values ensure tracking of the predefined trajectory. This is confirmed by fulfilling two existence conditions [26]:

Condition 1(Lyapunov): when $S>0$ then $\dot{S}<0$ and $u=1$

From (18):

$$-V_{in}+i_{in}(r_{in}-K_1)+v_c+i_o(K_2\ r_o)+v_oK_2+K_3(i^*_o-i_o)<v_c(K_2+1) \tag{19}$$

This implies that:

$$-\overset{\vee}{V}_{in}+r_1\ \hat{i}_{in}-K_1\overset{\vee}{i}_{in}-\overset{\vee}{v}_c\ K_2+K_2\ r_2\hat{i}_o+K_2\hat{v}_o+K_3(i^*_o-i_o)<0 \tag{20}$$

Condition 2: when $S<0$ then $\dot{S}>0$ and $u=0$

From (18):

$$-V_{in}+i_{in}(r_1-K_1)+v_c+i_o(K_2\ r_2)+v_oK_2+K_3(i^*_o-i_o)>0 \tag{21}$$

This implies that:

$$-\hat{V}_{in}+r_1\overset{\vee}{i}_{in}-K_1\hat{i}_{in}+\overset{\vee}{v}_c+K_2\ r_2\overset{\vee}{i}_o+K_2\overset{\vee}{v}_o+K_3(i^*_o-i_o)>0 \tag{22}$$

Equations (20) and (22) are referred to as existence equations. The sliding mode controllers for the other inverters are similarly obtained. The block diagrams of the other four buck-boost DMCSIs are shown in Fig. 4 while the associated existence equations are listed in Table 7.

5. Experimental results

The system concept, presented mathematical analysis, and simulations, are validated with a 2.5kW DMCSI as in Fig.1, with the parameters in Table 3, controlled with TMS320F280335 DSP. Fig. 5 shows the experimental rig, while Fig. 6 shows the experimental results for the presented analysis and discussion for the buck-boost DMCSIs when controlled by sliding mode control and connected to the grid (V_p = 200V) at unity power factor (γ=0). The efficiencies of the five buck-boost DMCSIs at different output power are shown in Fig. 7a. As from the simulation in Fig. 3, the efficiencies of the C5 and G5 are the highest. D1 and F5 have efficiencies higher than D2 for lower output power while D2 has a higher efficiency at higher output power. Fig. 7b shows the THD of the five inverters with respect to output power.

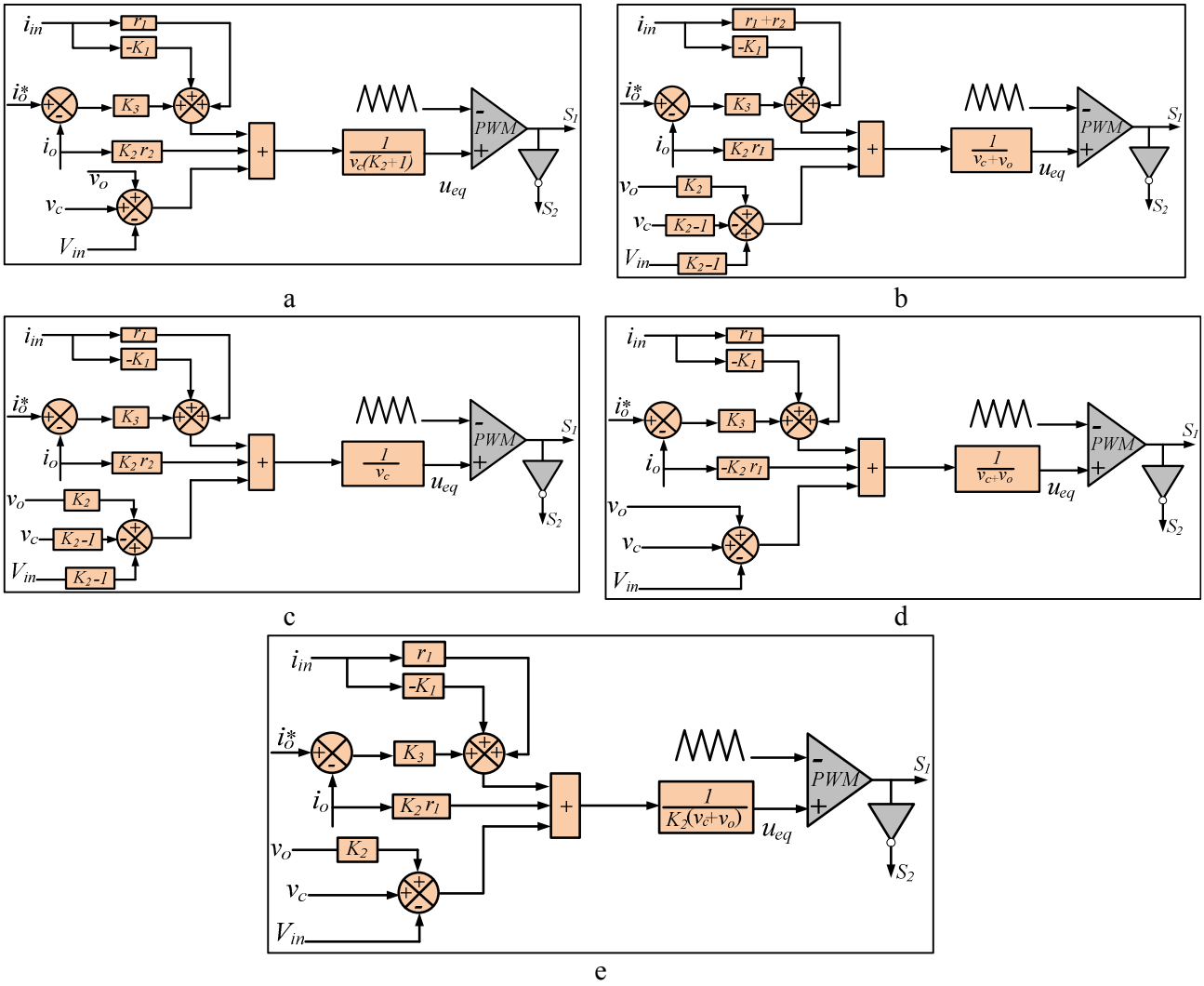


Fig. 4. *Block diagrams of DMCSI sliding mode controllers: (a) C5, (b) D1, (c) D2, (d) F5, and (e) G5*

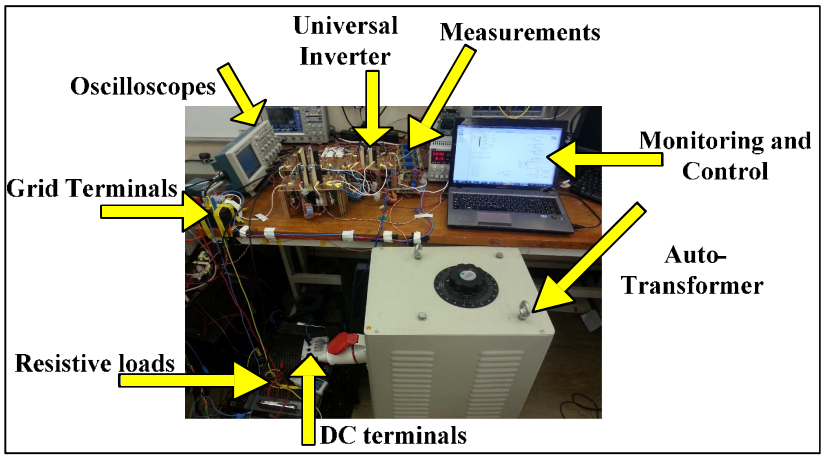


Fig. 5. *Experimental setup*

Table 7 Control and existence equations

C5	$u_{eq} = \delta = \frac{-V_{in} + i_{in}(r_1 - K_1) + v_c + i_o(K_2 r_2) + v_o K_2 + K_3(i^*_o - i_o)}{v_c(1 + K_2)}$ $-\check{V}_{in} + r_1 \hat{i}_{in} - K_1 \check{i}_{in} - \check{v}_c K_2 + K_2 r_2 \hat{i}_o + K_2 \hat{v}_o + K_3(i^*_o - i_o) < 0$ $-\hat{V}_{in} + r_1 \check{i}_{in} - K_1 \hat{i}_{in} + \check{v}_c + K_2 r_2 \check{i}_o + K_2 \check{v}_o + K_3(i^*_o - i_o) > 0$
D1	$u_{eq} = \frac{V_{in}(K_2 - 1) + i_{in}(r_1 - K_1) - v_c(K_2 - 1) + i_o(K_2 r_2) + v_o K_2 + K_3(i^*_o - i_o)}{v_c}$ $K_2 \check{V}_{in} - \hat{V}_{in} + r_1 \check{i}_{in} - K_1 \hat{i}_{in} - K_2 \hat{v}_c + \check{v}_c + K_2 r_2 \check{i}_o + K_2 \check{v}_o + K_3(i^*_o - i_o) > 0$ $K_2 \hat{V}_{in} - \check{V}_{in} + r_1 \hat{i}_{in} - K_1 \check{i}_{in} - K_2 \check{v}_c + K_2 r_2 \hat{i}_o + K_2 \hat{v}_o + K_3(i^*_o - i_o) < 0$
D2	$u_{eq} = \frac{V_{in}(K_2 - 1) + i_{in}(r_1 + r_2 - K_1) - v_c(K_2 - 1) + i_o(K_2 r_2) + v_o K_2 + K_3(i^*_o - i_o)}{v_c + v_o}$ $K_2 \check{V}_{in} - \hat{V}_{in} + (r_1 + r_2) \check{i}_{in} - K_1 \hat{i}_{in} - K_2 \hat{v}_c + \check{v}_c + K_2 r_2 \check{i}_o) + K_2 \check{v}_o + K_3(i^*_o - i_o) > 0$ $K_2 \hat{V}_{in} - \check{V}_{in} + (r_1 + r_2) \hat{i}_{in} - K_1 \check{i}_{in} - K_2 \check{v}_c + K_2 r_2 \hat{i}_o + K_2 \hat{v}_o - \check{v}_o + K_3(i^*_o - i_o) < 0$
F5	$u_{eq} = \frac{-V_{in} + i_{in}(r_1 - K_1) + v_c + i_o(K_2 r_2) + v_o K_2 + K_3(i^*_o - i_o)}{K_2(v_c + v_o)}$ $-\hat{V}_{in} + r_1 i_{in}(min) - K_1 \hat{i}_{in} + \check{v}_c + K_2 r_2 \check{i}_o + K_2 \check{v}_o + K_3(i^*_o - i_o) > 0$ $-\check{V}_{in} + r_1 \hat{i}_{in} - K_1 \check{i}_{in} - K_2 \check{v}_c - \hat{v}_c + K_2 r_2 \hat{i}_o + K_3(i^*_o - i_o) < 0$
G5	$u_{eq} = \frac{-V_{in} + i_{in}(r_1 - K_1) + v_c - i_o(K_2 r_2) + v_o + K_3(i^*_o - i_o)}{v_c + v_o}$ $-\hat{V}_{in} + r_1 \check{i}_{in} - K_1 \hat{i}_{in} + \check{v}_c - K_2 r_2 \hat{i}_o + \check{v}_o + K_3(i^*_o - i_o) > 0$ $-\check{V}_{in} + r_1 \hat{i}_{in} - K_1 \check{i}_{in} - K_2 r_2 \check{i}_o + K_3(i^*_o - i_o) < 0$

D2 has the lowest THD while C5 and D1 have the highest. Both D1 and F5 have the lowest input current ripple. However F5 and G5 require output capacitor C_o, while the voltage stresses across the intermediate capacitors in F5 and G5 are lower than the stresses in the other inverters. The relationship between the input current ripple and the total efficiency for the PV systems are to be considered in further publications.

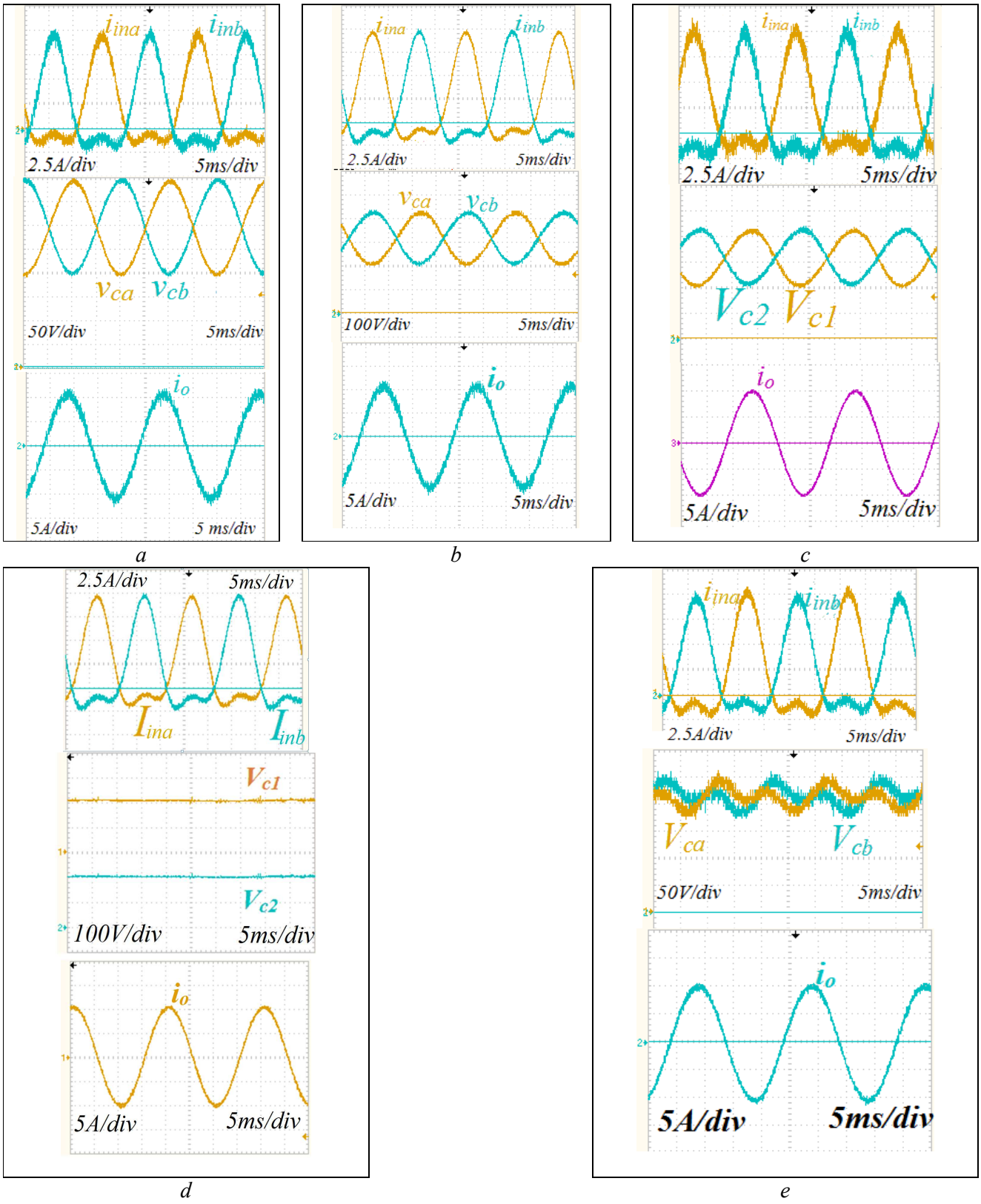
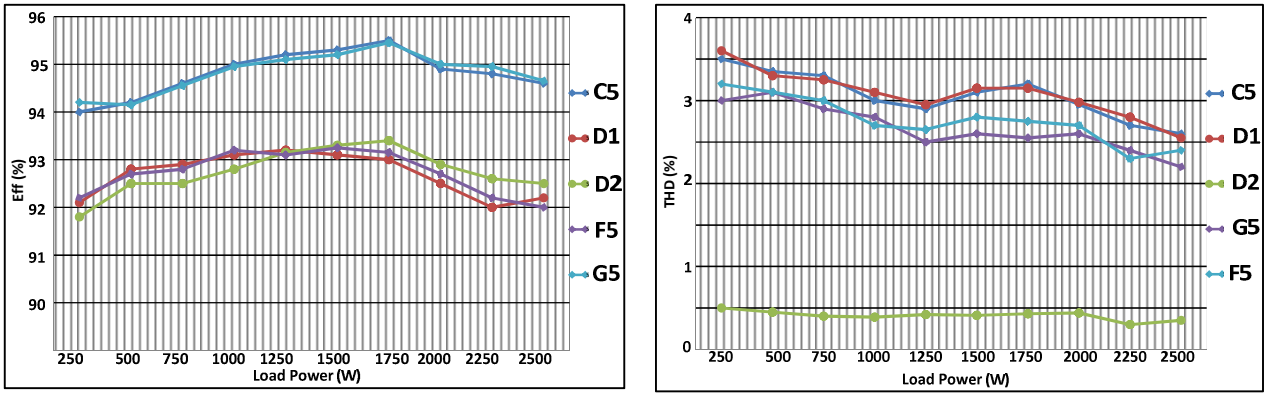


Fig. 6. *Experimental results: (*a) C5, (b) D1, (c) D2, (d) F5 and (e) G5.



a *b*

Fig. 7*. Experimental plots of DMCSIs: (*a) efficiency and (b) THD.

6. Dc side harmonic filtering

Single-phase inverters draw and deliver oscillating power, with the second-order current harmonic (superimposed on an average dc current) in the dc link (the dc side), independent of the power flow direction. In low power applications, such as small-scale PV systems for micro-grids, filtering is required at the dc side because the harmonic current components will significantly affect PV MPPT. In [21], a two-switch two-diode reversible boost converter can actively eliminate the second order harmonic component from the input of the PV or EV system currents as shown in Fig. 8a and the energy can be stored temporarily in an output capacitor C_{HC}. However, this harmonic compensator (HC) method requires an additional power electronic converter which adds to the total cost and control complexity.

The instantaneous power equation of the differential buck-boost inverter with an HC can be written as:

$$P_{in}(t) = P_{HC}(t) + P_o(t)$$

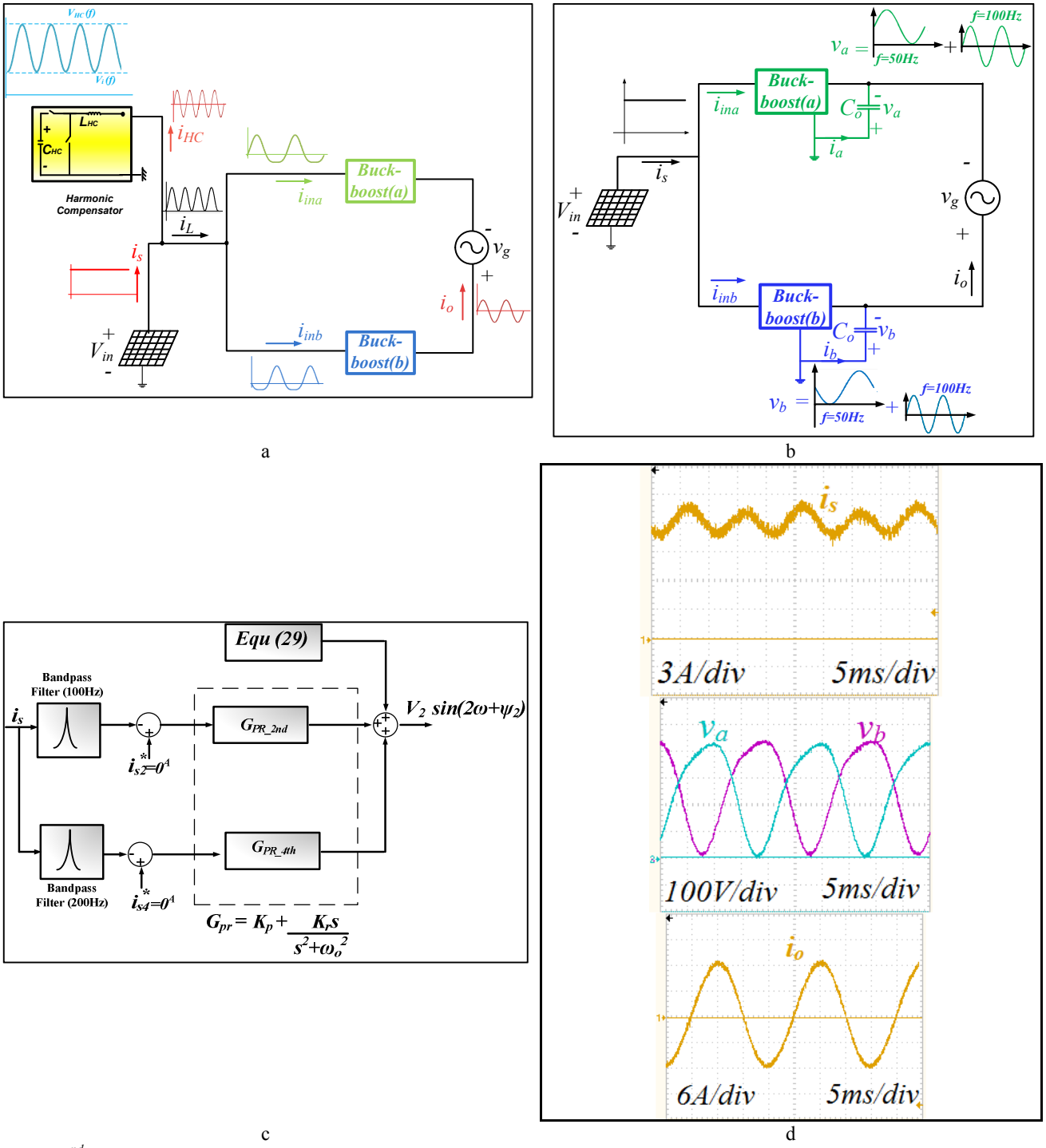
$$V_{in} I_s = i_{HC}(t)\, V_{in} + v_g(t)\; i_o(t)$$

$$I_s = \tfrac{1}{2}\frac{V_o\, I_o}{V_{in}}$$

$$i_{HC}(t) = I_s - \frac{v_g(t)\; i_o(t)}{V_{in}} \tag{23}$$

$$i_{HC} = \tfrac{1}{2}\frac{V_p\, I_o}{V_{in}}\cos 2\omega t$$

$$I_{HC}^{peak} = \tfrac{1}{2}\frac{V_p\, I_o}{V_{in}}$$



a b c d

Fig. 8. *2nd harmonic elimination of DMCSI: (*a) active elimination with additional power electronic converter [21], (b) active elimination without additional power electronic converter, (c) control for the proposed method, and (d) experimental results for C5 DMCSI with the proposed method.

The energy ($P_{HC}\,dt$) flows from the input side and is stored in the output capacitor C_{HC} in the +ve half cycle of i_{HC} and $v_{HC}(t)$ increases from $V_{HC}(i)$ to $V_{HC}(f)$. In the -ve half cycle of i_{HC}, the same energy flows from C_{HC} back to the dc supply leading $v_{HC}(t)$ to decrease from $V_{HC}(f)$ to $V_{HC}(i)$. This energy cycling can be expressed as:

$$\begin{aligned} &V_{in}\int_{0}^{½t_{HC}} i_{HC}(t)\,\mathrm{dt} = ½C_{HC}[v_{HC}^2(f) - v_{HC}^2(i)] \\ &\text{where } t_{HC} = 1/2f \text{ and } v_{HC}(i) = V_{in} \\ &v_{HC}^2(f) = V_{in}^2 + \frac{V_p\, I_o}{2\pi f\, C_{HC}} \\ &v_{HC}(f) = \sqrt{v_{in}^2 + \frac{V_p\, I_o}{2\pi f\, C_{HC}}} \end{aligned} \tag{24}$$

The proposed single-phase buck-boost DMCSIs have the capability to decouple the 2nd order harmonic current component without additional power electronic devices. From Fig. 8b, an additional controller forces energy oscillating at 100/120 Hz to be stored instantaneously in the output capacitors C_o (which are necessary for F5 and G5 inverters and optional for C5, D1 and D2 inverters). The controller must ensure that this stored energy does not affect the output voltages and currents. Therefore, two voltages with the same magnitude, phase-shift and 100/120 Hz frequency are superimposed across the output capacitors. Without decoupling the double-frequency power, the output instantaneous power is:

$$\begin{aligned} &p(t) = \underbrace{S\cos\gamma}_{P} \underbrace{-S\cos(2\omega t - \gamma)}_{Q} \\ &\text{where } S = \tfrac{1}{2}V_p I_o \end{aligned} \tag{25}$$

where Q is the reactive power absorbed by the load

The converter output voltages, v_a and v_b shown in Fig. 8b, can be expressed as:

$$\begin{aligned} v_a(t) &= ½V_p + ½V_p \sin\omega t + V_2 \sin(2\omega t + \psi_2) \\ v_b(t) &= ½V_p + ½V_p \sin(\omega t + \pi) + V_2 \sin(2\omega t + \psi_2) \end{aligned} \tag{26}$$

Because they are of same magnitude V_2, frequency $2f$, and phase shift ψ_2, the second order components in the output voltages v_a and v_b do not affect and are not seen by the load voltage v_g and current i_o. That is, the second order component is eliminate in the output $v_a - v_b$.

For the C5 DMCSI example, the total reactive power stored in the inductors (L_1 and L_2) and capacitors (C and C_o) in the differential inverter can be written as:

$$Q_s(t) = L_1\left(\frac{di_{ina}}{dt} i_{ina} + \frac{di_{inb}}{dt} i_{inb}\right) + 2L_2 \frac{di_o}{dt} i_o + C\left(\frac{dv_{ca}}{dt} v_{ca} + \frac{dv_{cb}}{dt} v_{cb}\right) + C_o\left(\frac{dv_a}{dt} v_a + \frac{dv_b}{dt} v_b\right) \quad (27)$$

To eliminate the 2nd order harmonic current supplied from the input dc source, the total stored energy in the inverter should be zero. Equating Q to Q_s in equations (25) and (27) and solving for V_2 and ψ_2 leads to:

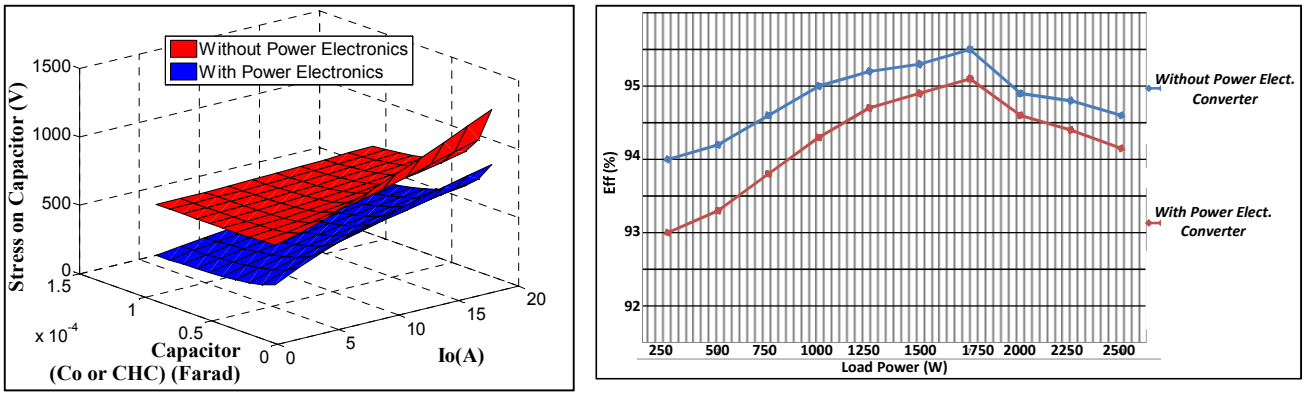
$$\psi_2 = \tan^{-1} \frac{\omega C_d V_p^{\,2}}{4S \cos\gamma}$$
$$V_2 = \frac{S \cos\gamma}{2\omega C_o V_p \cos\psi_2} \quad (28)$$

where $C_d = C + C_o$

However, eliminating the double frequency oscillating power will generate 4th order oscillating power Q_{4th}:

$$Q_{4th} = 2\omega V_2^2 \sin(4\omega t + 2\psi) \quad (29)$$

The emerging 4th order oscillating power will generate 4th order oscillating current in the input side and needs an additional control loop for elimination. In Fig. 8c, a proportional-resonant (PR) controller is implemented in order to ensure suppression of the 2nd and 4th order harmonics from the input current. As the controller's fast dynamics are not important, the gain values of the PR controller (K_p and K_r) can be selected much lower than the main loop values in order to avoid interaction. Fig. 8d shows the performance of this controller with C_o = 150μF where it removes 75% of the 2nd order harmonic component in the input current. Fig. 9a shows the voltage stress across the decoupling capacitors (C_{HC} and C_o) for the two active methods, with and without power electronic devices, at different output current and capacitor values.



a b

***Fig. 9**. 2nd harmonic elimination of DMCSI : (*a) voltage stress across the decoupling capacitor (C_o *or* C_{HC}) for active elimination methods and (b) differential-mode C5 inverter efficiency with 2nd order harmonic currents active elimination techniques.

Using additional power electronics results in lower stress on the capacitor C_{HC} (lower plane in Fig. 9a) than on C_o with the second method (upper plane in Fig. 9a). However, Fig. 9b shows that the efficiency of the second method is higher, since device power losses of the additional power electronic converter decrease efficiency.

7. Conclusion

The paper investigated single-stage single-phase inverters based on two differentially connected reversible buck-boost converters which have advantages when embedded in renewable energy generation systems. The inverters have a low dc side ripple current, without recourse to electrolytic capacitor filtering. The buck-boost converters have nonlinear high order transfer functions where the dynamics depend on the operation point and the duty ratio, which complicates control design. A 2nd order harmonic dc side input current component disturbs MPPT, hence reduces total efficiency. In this paper, five topologies for DMCSIs were proposed. With their operation, features, and control design using sliding mode control were investigated and verified.

The C5 and G5 based inverters have the lowest power loss, hence the highest efficiencies. However, they experience high input current ripple and may require higher input inductors values. The D1 and F5 converters have good efficiency at higher input dc voltages while the efficiency deteriorates at lower input voltages. The efficiency of the D2 inverter is lower than D1 and F5 at high input voltage but is better at lower input voltages. From the devices rating point of view, the five inverters topologies have the same performance. Using the same passive element values, D2 is found to have the lowest THD in the output voltage and current waveforms. D1 and F5 inverters have low input ripple current which is attractive feature for PV systems. F5 and G5 inverters have the lowest capacitor voltage stresses, hence smaller and cheaper capacitors can be used.

A new active method to suppress the 2nd order harmonic input current from the DMCSIs without additional power electronic converters is proposed. The 2nd order reactive power is decoupled using the inverter output capacitors in the ac side. Comparing the proposed technique with a power electronic based active elimination method, the proposed method avoids the power losses associated with an additional power electronic converter, which reduces system efficiency.

An experimental universal single-phase inverter was used to validate the theoretical and mathematical analysis. Detailed overall control analysis, including MPPT operation, as well as the effect of grid side imbalance, common mode voltage, and low order harmonics are yet to be considered.

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