Single-stage Three-phase Differential-mode Buck-Boost Inverters with Continuous Input Current for PV Applications

Ahmed Darwish* *University of Strathclyde, UK*
Ahmed Massoud *Qatar University, Qatar*
Derrick Holliday *University of Strathclyde, UK*
Shehab Ahmed *Texas A&M University at Qatar, Qatar*
Barry Williams *University of Strathclyde, UK*
*ahmed.mohamed-darwish-badawy@strath.ac.uk

***Abstract* – Differential-mode buck-boost inverters have merits such as reduced switch number, ability to provide voltages higher or lower than the input voltage magnitude, improved efficiency, reduced cost and size, and increased power density, especially in low-power applications. There are five buck-boost inverters that can provide flexible output voltage without the need of a large electrolytic input side capacitor, which degrades the reliability of inverters. The continuous input current of these inverters is appropriate for maximum power point tracking operation in photovoltaic and fuel cells applications. Three of the five inverters can be isolated with high-frequency-link (HFL) transformers where the common-mode leakage current can be mitigated. However, the performance and control of such converters have not been discussed in detail. In this paper, the five possible single-stage three-phase differential-mode buck-boost inverters with continuous input current are investigated and compared in terms of total losses, maximum ripple current, total harmonic distortion (THD), and device and passive element ratings. In addition, the possible methods are presented for eliminating the input third order harmonic current, resulting from the stored energy in the passive elements, as well as the output second order harmonic currents. The ability for isolating the input and output sides of the inverters with a small-high frequency transformers is discussed. A changeable-terminal 2.5kW bidirectional inverter is used to validate the design flexibility of the inverter topologies, when DSP-controlled.**

Keywords — dc-dc converters, Cuk converter, SEPIC converter, buck-boost inverter, state space averaging, high frequency transformers, Sliding Mode Control, switched mode power supply

NOMENCLATURE

$\overline{\quad}$	variable average value
*	variable reference value
a-b-c	Three phases subscripts
C	Converter transfer capacitor
C_o	Converter output capacitor
f	Output voltage and current fundamental frequency
f_s	Sampling frequency
h	Converters voltage ratio
H_{dc}, H_{ac}	DC and AC voltage ratio constants
i_{in}, i_o	Converter input and output currents
I_o	Peak value of load current
I_{in}	Total input current
L_1, L_2	Converter input and output inductors
r_1, r_2	Parasitic resistances of input and output inductors
L_g	Grid inductance
t_{on}, t_{off}	Converter on and off time
t_s	Sampling time
v_c	Transfer capacitor voltage
V_{in}	Input voltage
V_m	Peak value of output voltage
v_o	Output voltage
γ	Phase angle of load current
δ	Duty cycle
ω	Output voltage angular frequency

I. INTRODUCTION

New inverter topologies are gaining significance due to the rapid growth and penetration of renewable energy sources such as photovoltaics (PV), fuel cells, wind turbine systems, etc. Consequently, reducing converter weight, volume, and passive element values becomes more demanding [1]-[3]. Three-phase dc/ac converter topologies have been presented in the literature [4]-[10]. Most of the proposed topologies have full bridge configurations converting the dc input to ac output voltages, in case of the voltage source inverter (VSI) or dc input to the ac output currents, with current source inverter (CSI) topologies [11], [12]. As a drawback, these full bridge configurations may create undesirable common-mode leakage currents [13]. When a variable common-mode voltage is generated because of the mismatch in parasitic components values, the common-mode leakage current may flow through the inverters capacitors and the common ground, violating the safety regulations [14].

For reasons related to noise mitigation, electromagnetic compatibility and isolation, galvanic isolation between the input and output of a power converter is necessary in many applications [15]. Many small and medium scale power converters with buck-boost capability can be modified to offer transformer coupling and isolation. High-frequency-link (HFL) inverters have been proposed as solutions to common-mode leakage currents, providing higher output voltages, volume reduction and efficiency improvement [16]-[18].

Most dc-ac converters installed in PV systems require a large input filtering capacitance, typically electrolytic types. Replacing this electrolytic capacitor with a plastic type increases the inverter's reliability significantly as it is at least thirty times more reliable, for the same capacitance and voltage [19]. At rated operating conditions, the lifetime of this filter capacitor is short when compared with the other inverter components [20]. Thus, this capacitor forms a difficulty to increasing overall system reliability. The lifetime of a capacitor is halved for every 10^{o}C increase in the operating temperature [21].

For dc-ac conversion, the conventional two-level VSI is the most common converter topology [22, 23] where the output ac voltage peak is always lower than the input dc voltage and the output ac current peak is always greater than the input dc current. Because of the VSI voltage buck nature, a boost dc-dc converter may be installed between the PV and the inverter input, for voltage matching and maximum power point tracking (MPPT), hence the system total volume, weight, losses, and hence, cost are increased [24]. A classification of single-stage buck and boost inverter topologies has been presented [25]. In [26], buck-boost Z-source inverter topologies were proposed and investigated.

Two back-to-back dc-dc converters can form a single-phase differential-mode inverter. Some of these differential-mode inverter types are shown in [24], [22, 23]. The differential-mode inverter initially appeared in [23] as a single-phase boost inverter, while a differential-mode buck inverter is presented in [27]. The differential-mode boost inverter is discussed and

analysed in [28]. Knight *et al*. in [29] propose the differential-mode six-switch single-phase buck-boost inverter based on the *Ćuk* converter. However, the paper does not provide any performance evaluation for the proposed topology. A three-phase differential-mode inverter based on the *Ćuk* converter is proposed in [24] while a four-switch three-phase differential-mode inverter based on the sepic converter is proposed in [30]. Generally, differential-mode inverters have fewer switches and all are low-side driven. The inverters are capable of bidirectional energy flow using the same number of switches and the same control. As an advantage, differential-mode inverters can increase the step-up voltage or current ratios.

Of the known two-switch two-diode bidirectional buck-boost converters, there are five converters that can provide continuous input currents hence mitigate the need for large electrolytic filter capacitance [34]. Continuous input current switched mode power supplies (SMPS) based inverters enable safe and reliable converter-grid connection. Moreover, they are attractive solutions for energy conversion systems in terms of: 1) voltage buck-boost operation with a flexible output voltage range, 2) provide continuous input current, 3) have better efficiency, and 4) are suitable for high frequency transformer coupling. The main disadvantages of these inverters are the high voltage stress of the transfer capacitor and switches, at high duty cycles.

Generally, continuous input current converters are time variant systems where the overall transfer function describing the relation between the input and output voltages and currents depends on the switching periods of the switches. This results in a complex stable design because the converter poles and zeros travel through a long trajectory. Moreover, the time-varying transfer function leads to output voltage and current distortion [24], [31], [32]. Converter stability and reliability decreases with increasing passive element values [33]. However, reducing inductor and capacitor values results in larger high frequency switching ripple current and voltage components and hence, increased Total Harmonic Distortion

(THD) of the output current and voltage. But increasing the passive element values increases the stored energy causing the inverter to produce a third order harmonic component and its multiples in the input dc current.

This paper proposes, discusses and compares the possible five topologies of differential-mode buck-boost converters without electrolytic capacitors for low-power applications in terms of efficiency, input current ripple, output current THD, switch ratings and proposes proper control design. The basic structure of the three-phase buck-boost differential-mode current source inverter (DM-CSI) concept under investigation is shown in Fig.1. Also the paper presents possible methods for decoupling the low order harmonic current components in the proposed DM-CSIs and discusses the effect on passive element sizing. The ability for these inverters to be isolated with high frequency transformers, for noise and common-mode voltages mitigation, and the effect on normal inverter operation are considered.

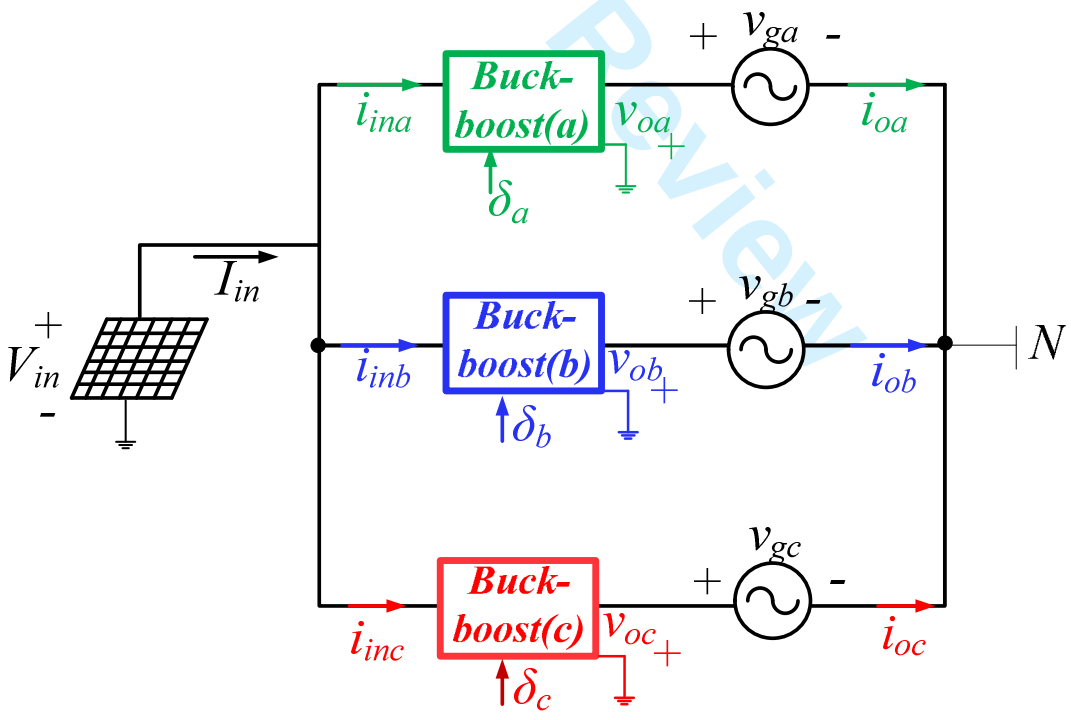


Fig.1. Basic structure of a grid-connected three-phase differential-mode buck-boost inverter.

II. SYSTEM DESCRIPTION

The input voltage dc source is connected to three bidirectional buck-boost converters as shown in Fig.1. Assume the grid phase voltages v_{ga}, v_{gb} and v_{gc} are expressed as:

$$\begin{aligned} v_{ga}(t) &= V_g \sin\omega t \\ v_{gb}(t) &= V_g \sin(\omega t - \tfrac{2}{3}\pi) \\ v_{gc}(t) &= V_g \sin(\omega t + \tfrac{2}{3}\pi) \end{aligned} \tag{1}$$

Each buck-boost converter produces an output phase voltage comprised of a sinusoid pulse width modulated waveform superimposed on a common dc offset component. Due to the differential-mode connection of the converter output voltages, the dc component in the output voltages are decoupled from the inverter load, which is the three-phase grid voltage in this case. The converter voltages v_{oa}, v_{ob} and v_{oc} are expressed as:

$$\begin{aligned} v_{oa}(t) &= -h_a V_{in} \\ h_a &= H_{dc} + H_{ac}\sin(\omega t + \theta) \\ v_{oa}(t) &= -[V_{dc} + V_m \sin(\omega t + \theta)] \end{aligned} \tag{2}$$

$$\begin{aligned} v_{ob}(t) &= -h_b V_{in} \\ h_b &= H_{dc} + H_{ac}\sin(\omega t + \theta - \tfrac{2}{3}\pi) \\ v_{ob}(t) &= -[V_{dc} + V_m \sin(\omega t + \theta - \tfrac{2}{3}\pi)] \end{aligned} \tag{3}$$

$$\begin{aligned} v_{oc}(t) &= -h_c V_{in} \\ h_c &= H_{dc} + H_{ac}\sin(\omega t + \theta + \tfrac{2}{3}\pi) \\ v_{oc}(t) &= -[V_{dc} + V_m \sin(\omega t + \theta + \tfrac{2}{3}\pi)] \end{aligned} \tag{4}$$

where h is the conversion ratio, θ is the voltage arbitrary phase-shift and H_{dc} and H_{ac} are constants. All the buck-boost converters under investigation have voltage conversion ratios of the form:

$$h_x = \frac{v_{ox}}{V_{in}} = \frac{i_{inx}}{i_{ox}} = \frac{\delta_x}{1-\delta_x}, \quad \text{where } x = a, b, \text{or } c \tag{5}$$

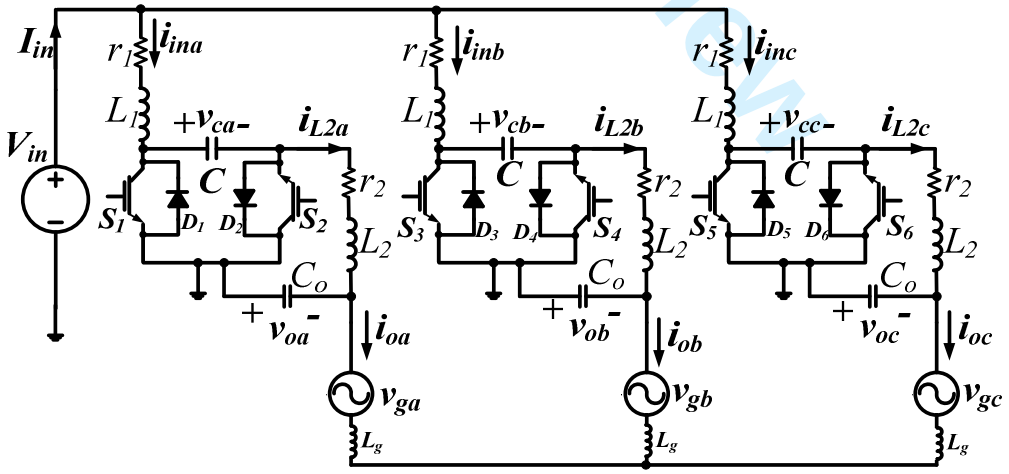
The duty ratios can be calculated as:

$$\delta_x = \frac{h_x}{1+h_x}, \quad where\ x = a, b, or\ c \tag{6}$$

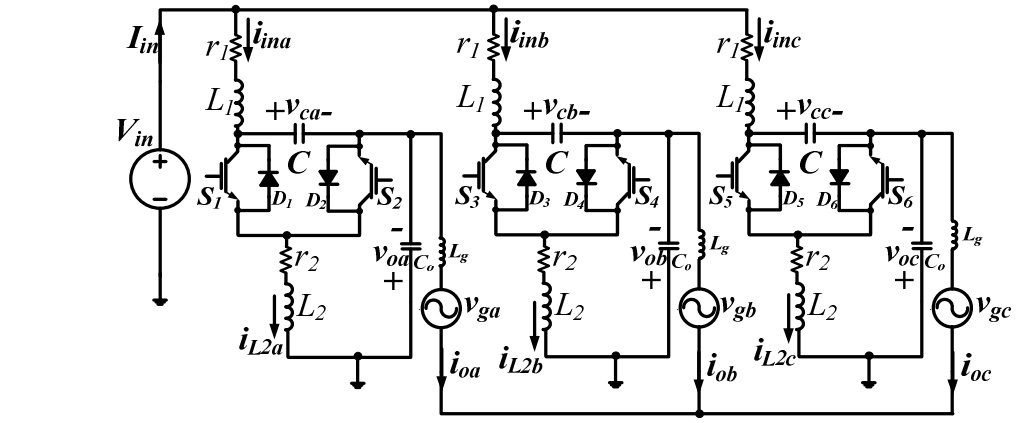
The output currents i_{oa}, i_{ob}, and i_{oc} are expressed as:

$$\begin{aligned} i_{oa}(t) &= I_o \sin(\omega t + \gamma) \\ i_{ob}(t) &= I_o \sin(\omega t - \tfrac{2}{3}\pi + \gamma) \\ i_{oc}(t) &= I_o \sin(\omega t + \tfrac{2}{3}\pi + \gamma) \end{aligned} \tag{7}$$

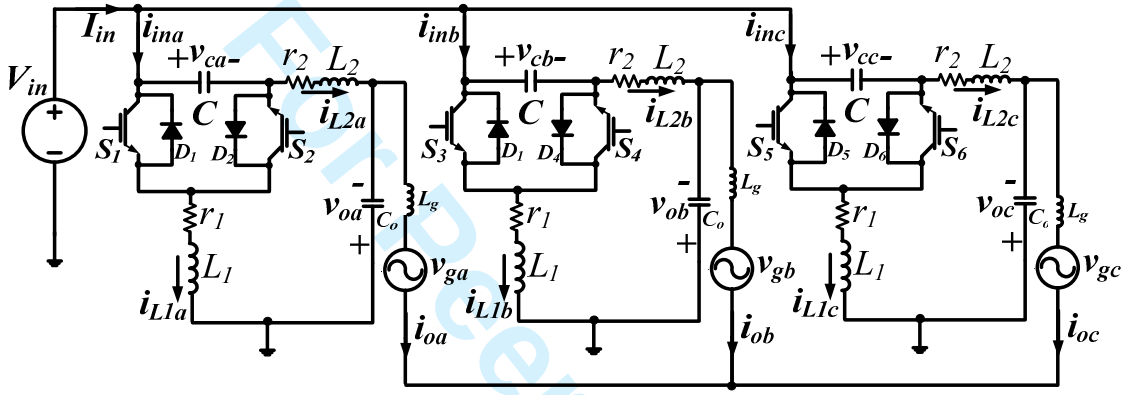
Of the known two-switch two-diode buck-boost converters, there are five converters that provide continuous input currents, namely, *C5 (Ćuk), D1, D2, F5, and G5 (sepic)* as per [34]. For all these converters, the power is transferred from the input to the output (or in the opposite direction) through a capacitor (C) while stored in input and output inductors (L_1 and L_2). For the C5, D1 and D2 converters, the output shunt capacitor C_o is optional. However, it is mandatory for the F5 and G5 converters. The single-stage three-phase buck-boost DM-CSIs based on these converters are shown in Fig.2. The switches (S_1, S_3, S_5) are ON during $0<t<t_{on}$ while the switches (S_2, S_4, S_6) are ON during $t_{on} \le t < t_s$. The switch pairs (S_1, S_2), (S_3, S_4), and (S_5, S_6) are complementary.



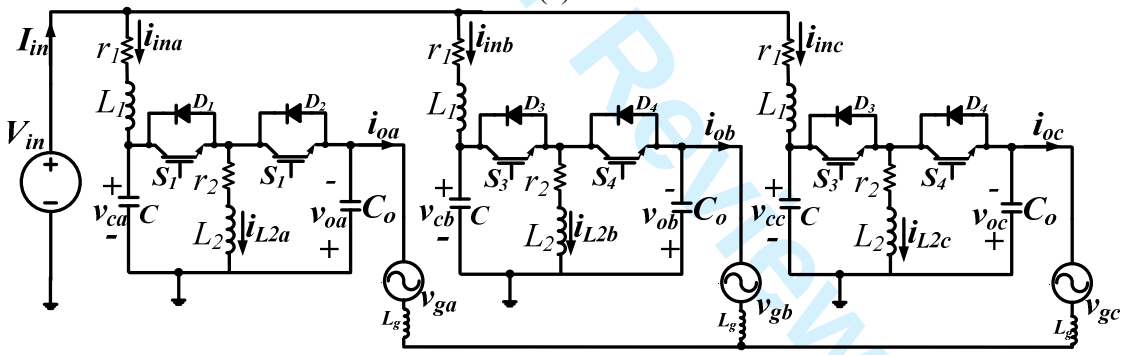
(a) C5



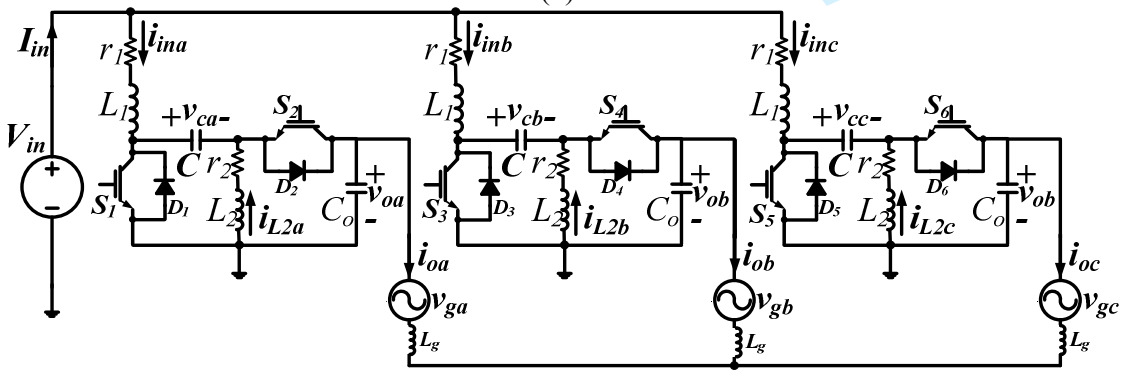
(b) D1



(c) D2



(d) F5



(e) G5

Fig.2. Buck-boost differential-mode current source inverters.

III. DM-CSIs Performance Comparison

In this section, comparison of the significant features of the proposed inverters is presented, commencing from their basic building blocks. These features are: 1) overall efficiency, 2) input current ripple, 3) output current THD, and 4) capacitor voltage stresses. The mathematical analysis and formulas are presented in Appendix A.

1. Power losses and efficiency

The power losses plots are shown in Fig.3 for different input voltages and output currents using the circuit conditions in

TABLE I. For the five three-phase inverters, three sources of power loss are considered: in the active switches ($S_1 \rightarrow S_6$), the reverse diodes ($D_1 \rightarrow D_6$) and the copper loss in the parasitic resistances of the inductors (r_1 and r_2). All five three-phase buck-boost DM-CSIs have the same switch and diode currents and voltages hence; they have the same power loss at all conditions. From Fig.3a, the power loss of the input side switches S_1, S_2, and S_5 are increased dramatically when the input side voltage is lower than half the output peak voltage (V_m). However, from Fig.3b, the copper losses of C5 and G5 are the lowest when V_{in} is above half the output voltage (V_m) while the copper losses of D2 are the lowest when V_{in} is above half the output voltage (V_m). The copper losses of D1 and F5 are always higher than the other DM-CSIs. The efficiencies of the five three-phase buck-boost DM-CSIs are plotted in Fig.3c. Summarizing, the efficiency of the C5 and G5 is better at higher V_{in} while D2 efficiency is better at lower V_{in}. The efficiency of D1 and F5 is always lower than the other DM-CSIs. The mathematical analysis related to Fig.3 is presented in A.1.

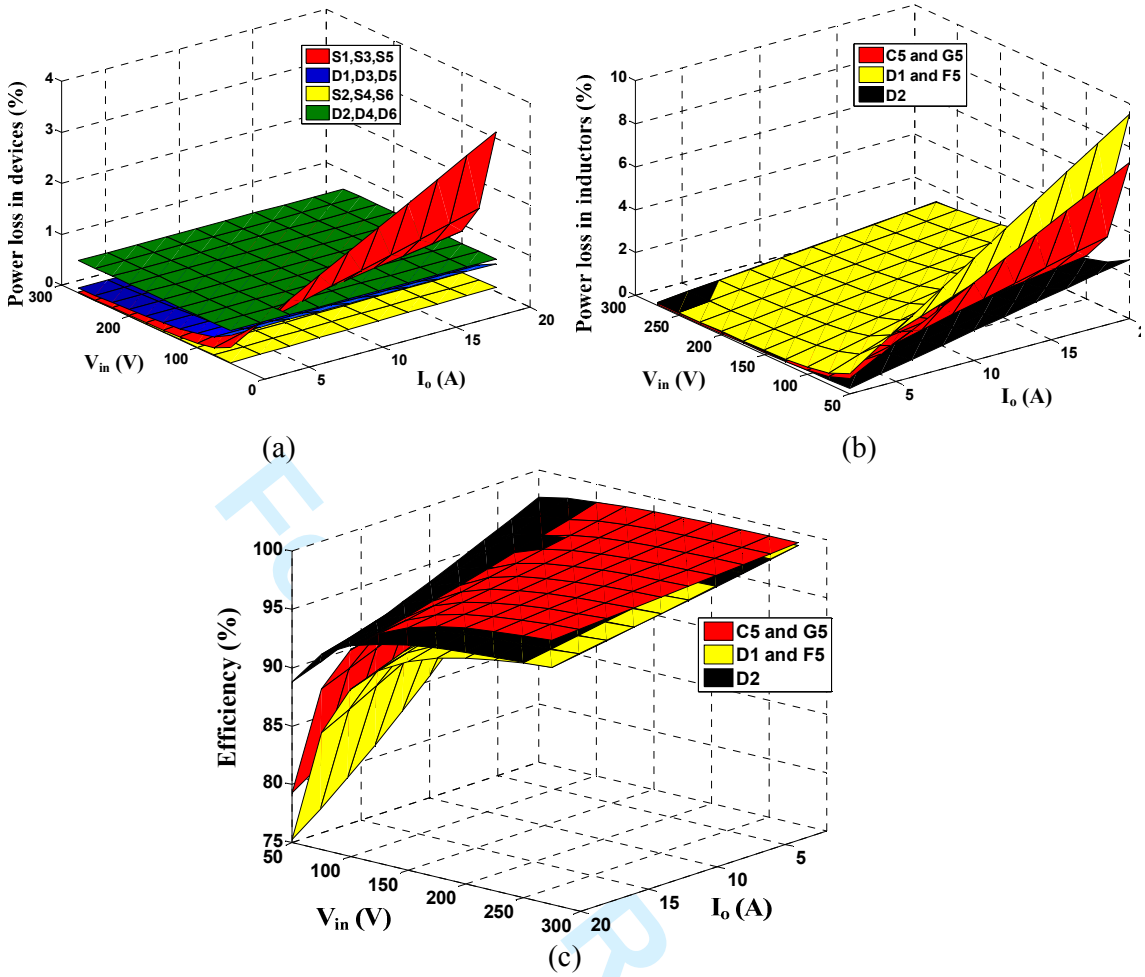


Fig.3. Power losses and efficiencies: (a) power losses in devices, (b) power losses in inductors, and (c) total efficiencies of the three-phase DM-CSIs.

2. Dc input current ripple (ΔI_{in})

For energy conversion applications like PV, fuel cells, etc., current and voltage ripple cause harmonics and power loss in the overall system, so should be reduced. Ref [35] demonstrates that input current and voltage ripple inversely affect the total power extracted from PV systems. The simulation in Fig.4 shows the input current ripple for the three-phase buck-boost DM-CSIs at the circuit conditions in

TABLE I and I_o = 10A. Generally, C5, G5 and D2 based DM-CSIs have the same input current ripple versus input and output voltage. As an important feature, both D1 and F5 have insignificant input current ripple compared with the other inverters.

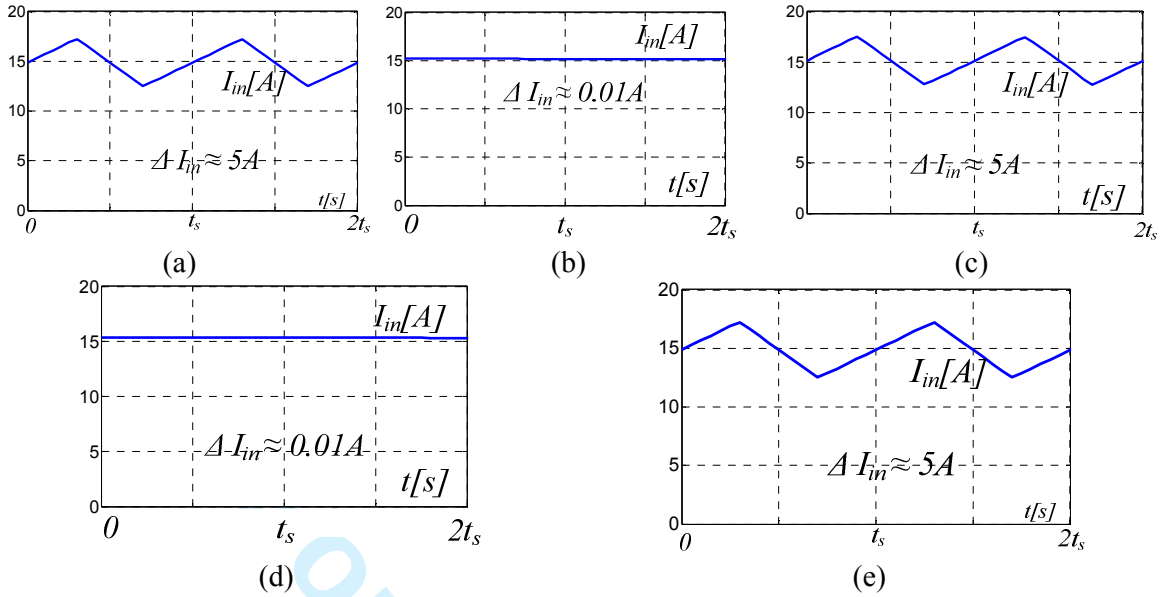


Fig.4. Matlab simulations of input current ripple of the five DM-CSIs: (a) C5, (b) D1, (c) D2, (d) F5, and (e) G5

TABLE I. PARASITIC COMPONENT VALUES AND CIRCUIT CONDITIONS

Parameter	Value
Rated power	2.5 kW
Switching frequency	f_s = 50 kHz
Input inductor	L_1 = 1mH, r_1 = 75 mΩ
Output inductor	L_2 = 1mH, r_2 = 75 mΩ
Input voltage	V_{in} = 100 V
Output voltage	V_m = 200 V
Output current angle	γ = 0º
Diode forward voltage	V_{DF} = 2V
Switch on resistance	R_{on} = 75mΩ
Transfer capacitor	C = 10μF
Output capacitor	C_o = 2.5μF

3. *Output current THD*

The output current distortion can be classified into low and high frequency distortion. Low order current distortion appears because of the non-linear nature and high system order of the proposed inverters and can be removed with appropriate control loops [24]. The high

frequency current and voltage ripple in the output side occur because of the switching action. These high frequency ripple components are dependent on the converter topology which the differential-mode inverter descends from. The simulation in Fig.5 shows the output current and THD for the three-phase buck-boost DM-CSIs at the circuit conditions in

TABLE I when I_o = 10A. From the simulation in Fig.5, C5, D1, and D2 have low THD compared with F5 and G5 for the same passive element values. This is commensurate with the fact that these two inverters are descendent from power converters with discontinuous output current therefore, should have a higher output capacitance value C_o. All inverters have considerable negative-sequence second order harmonic current components which can be eliminated with additional control loops.

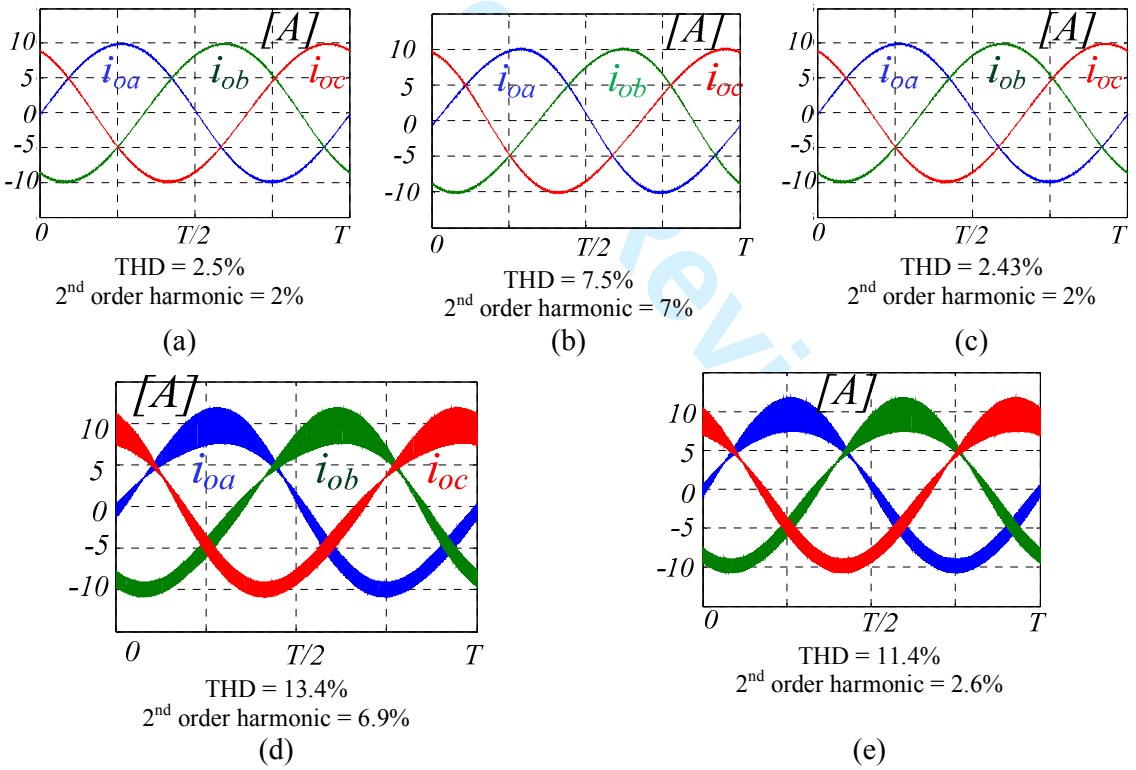


Fig.5. Matlab simulations of output current of the five DM-CSIs: (a) C5, (b) D1, (c) D2, (d) F5, and (e) G5

4. *Capacitor voltage stresses*

Knowledge of the voltage stresses on the energy transfer capacitor C is important for its specification. For some inverters, the voltage across C consists of a dc-bias plus a sinusoidal

voltage component (fundamental) while for other converters, the voltage across *C* is only dc. Inverters using F5 and G5 have lower capacitor voltage stresses than C5, D1 and D2. TABLE II summarizes the capacitor voltage stress for each converter, in terms of the source voltage and differential sinusoidal output maximum voltage, V_m.

TABLE II VOLTAGE STRESS ACROSS CAPACITOR C (SEE FIG. 2)

Topology	Minimum dc-bias	Sinusoidal voltage (fundamental)	Peak Voltage
C5	$V_{in}+V_m$	$V_m \sin \omega t$	$V_{in}+2V_m$
D1	$V_{in}+V_m$	$V_m \sin \omega t$	$V_{in}+2V_m$
D2	$V_{in}+V_m$	$V_m \sin \omega t$	$V_{in}+2V_m$
F5	V_{in}	≈0	V_{in}
G5	V_{in}	≈0	V_{in}

IV. CONTROL STRATEGIES FOR THREE-PHASE BUCK-BOOST DM-CSIS

The five three-phase buck-boost DM-CSIs under investigation are high order systems where classical control design is difficult and complex to implement. The small-signal transfer functions of the DM-CSIs are presented in Appendix A. A general control scheme can be used for all DM-CSIs, as shown in Fig.6.

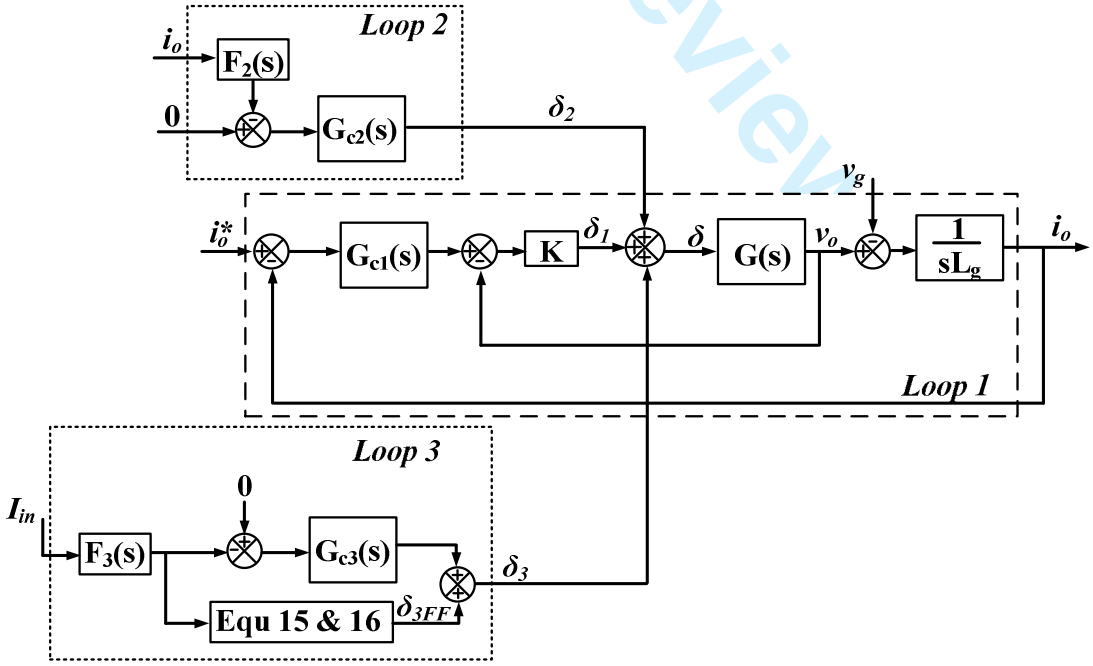


Fig.6. Control scheme for buck-boost three-phase DM-CSIs.

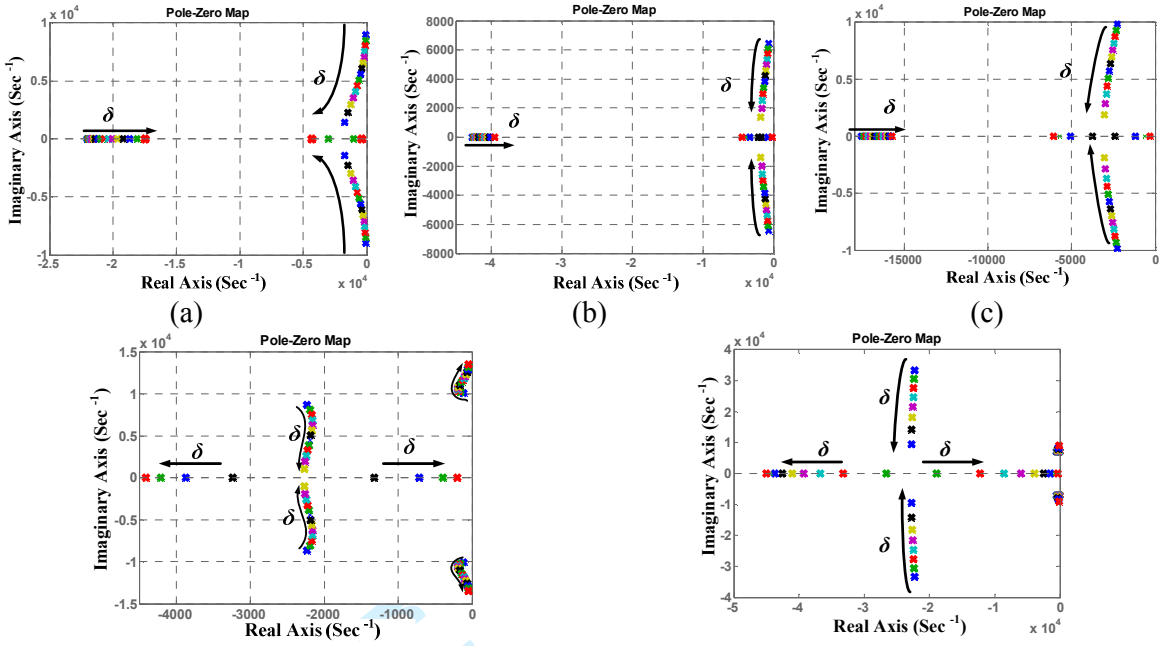


Fig.7. Open loop poles loci of buck-boost three-phase DM-CSIs: (a) C5, (b) D1, (c) D2, (d) F5, and (e) G5.

The control scheme consists of three feedback loops:

1. *Loop 1*

The first loop controls the fundamental components of the output current and voltage. The poles loci of the small-signal transfer functions *G(s)* for the different inverters are shown in Fig.7. To control the fundamental current (i_o), $G_{c1}(s)$ is chosen as a PR controller:

$$G_{c1}(s) = K_{p1} + \frac{K_{r1}s}{s^2+\omega_o^2} \tag{8}$$

The three degrees of freedom from the loop gains (K_{p1}, K_{r1}, *and* K) will be used to obtain fast response, low current oscillation, and good stability margins. Taking inverter C5 as an example, the closed loop transfer function is expressed as:

$$G_{CL}(t) = \frac{KG_{c1}G}{sL_g(1+KG)+KG_{c1}G} \tag{9}$$

Fig.8 plots the closed loop poles with variation of proportional gain value K_{p1} with three different values of K. The system is always stable for $0.5<K_{p1}<5$. Consequently, $K_{p1} = 2.5$, in the middle of the trajectory, is chosen for the experimentation. The main functions of the

inner loop gain K, are to increase the overall system bandwidth, and hence achieve fast response, as well as to damp resonance between the inverter inductors and capacitors. However, increased K leads to lower phase margin and hence, affects overall system stability. The value of K = 40 is selected to optimize the bandwidth and phase margin, see Fig.9. The resonant gain of the controller (K_{r1}) reduces the steady state error at the fundamental frequency (ω_o). Because of DM-CSI transfer function complexity, this gain is tuned during simulation and experimentation. K_{r1}= 20 gives an acceptable steady state error and transient response at ω_o.

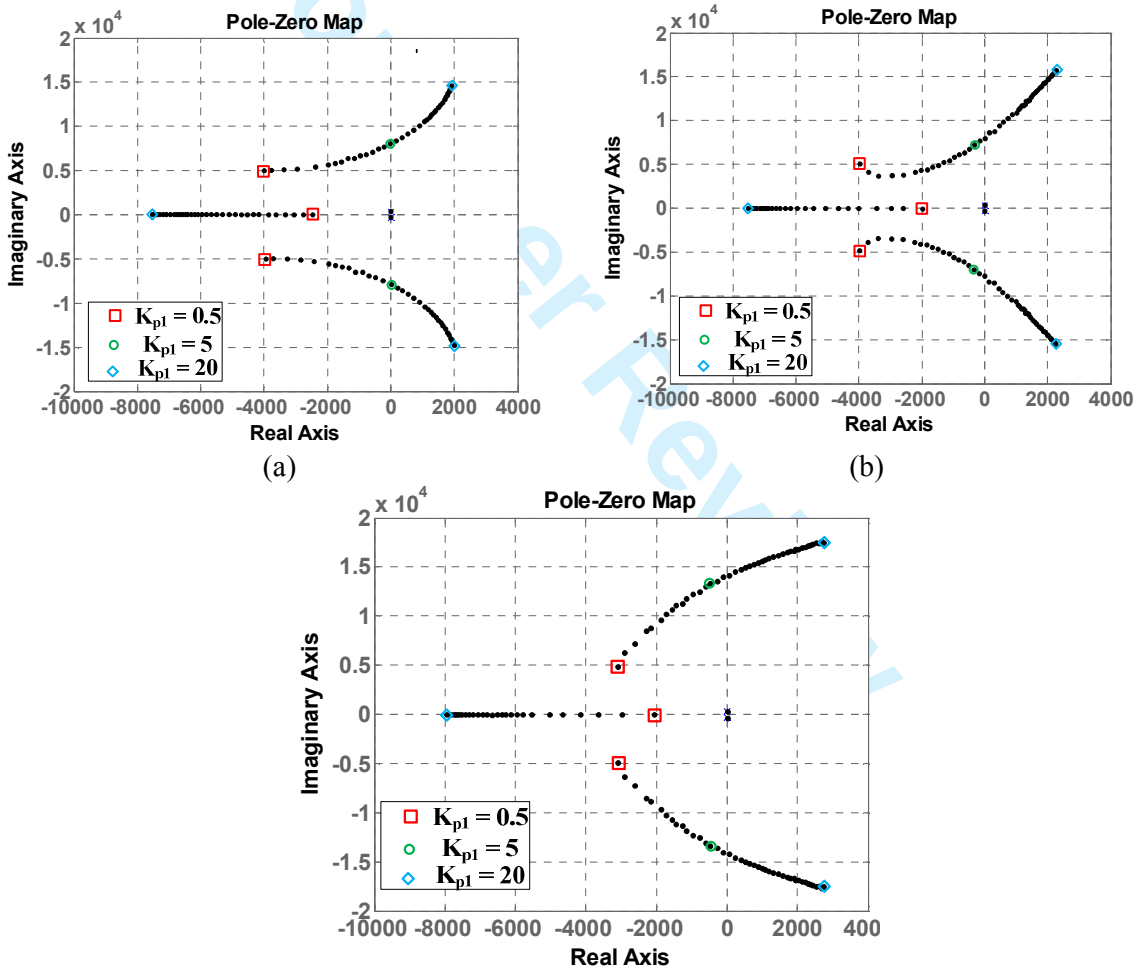


Fig.8. Variation of Loop 1 closed loop poles with controller proportional gain K_{p1}. (a) K = 10, K_{r1} = 20, K_{p1} = 0.5→20, (b) K = 50, K_{r1} = 20, K_{p1} = 0.5→20, and (c) K = 100, K_{r1} = 20, K_{p1} = 0.5→20

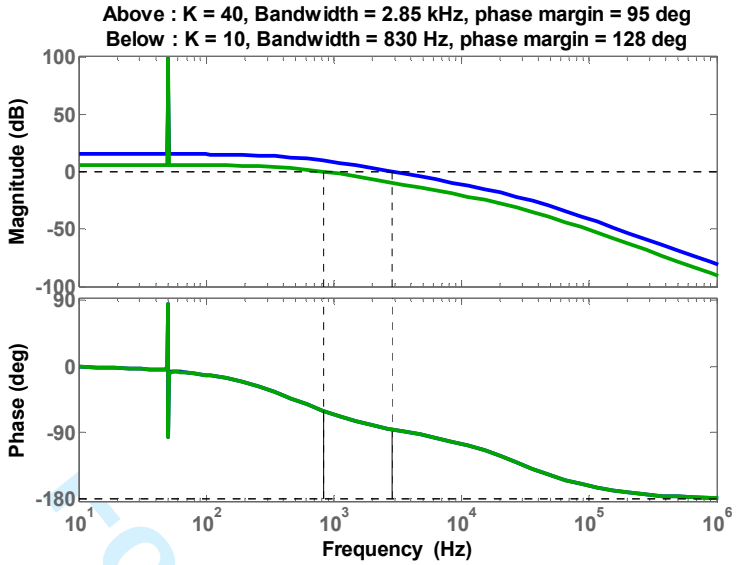


Fig. 9. Variation of Loop 1 frequency response with controller gain K values (K_{p1} = 2.5, K_{r1} = 20).

Increasing *K* leads to better and faster inverter fault current limiting capability. However, there is a tradeoff between increasing K and having acceptable stability margins for Loop 1. The system concept, presented mathematical analysis, and simulations, are validated with a 2.5 kW DM-CSI as in Fig.1, with the parameters in TABLE I, controlled using a TMS320F280335 DSP. Fig.10 shows the experimental rig. Fig.11 shows DM-CSI operation with Loop 1, along with the resultant second order distortion.

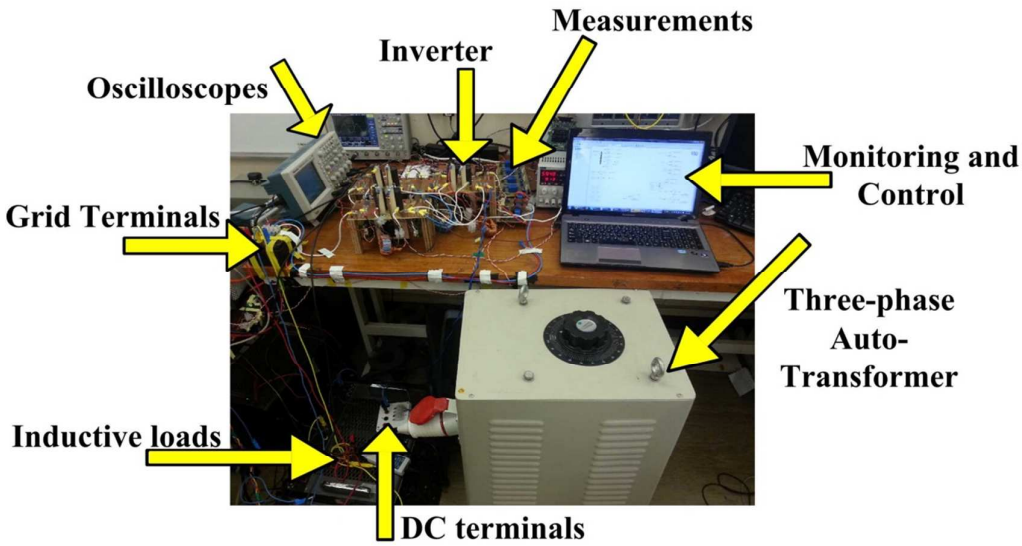


Fig.10. Experimental setup.

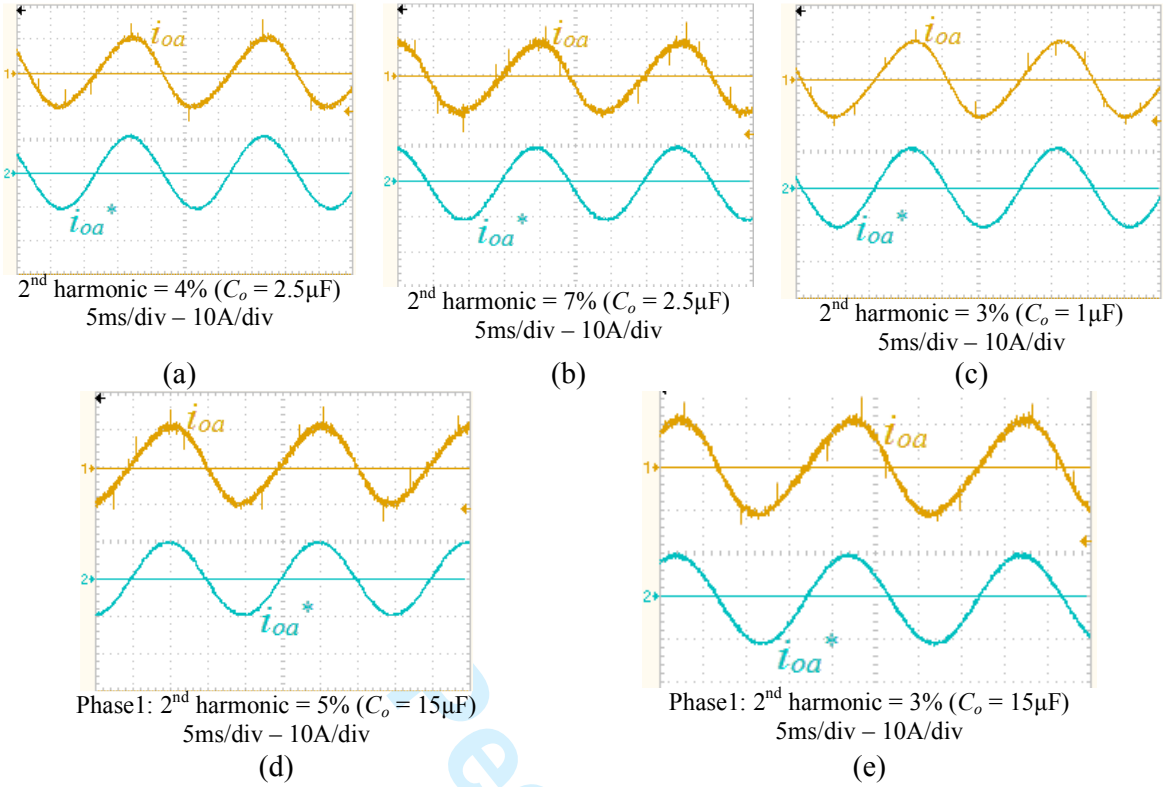


Fig.11. Operation of three-phase buck-boost DM-CSIs with Loop 1: (a) C5, (b) D1, (c) D2, (d) F5, and (e) G5.

2. Loop 2

Control Loop 2 is necessary to eliminate the second order harmonic current in the output three-phase current because of the nonlinearity of the buck-boost DM-CSIs; see Fig.11. This nonlinearity can be sensed from the open loop pole loci of the inverters as the poles move through the long trajectory with different duty ratios. The second order harmonic current component increases with increase inverter passive element values. However, such an increase may be necessary for some applications when the switching frequency is to be lowered. The second order harmonic current is extracted with a band-pass filter $F_2(s)$ and fed to a resonant controller $G_{c2}(s)$ at double the fundamental frequency to calculate the required second order duty ratio δ_2. The filter gain (a_2) is selected to adjust the filter's bandwidth to cater for a ±1% frequency variation.

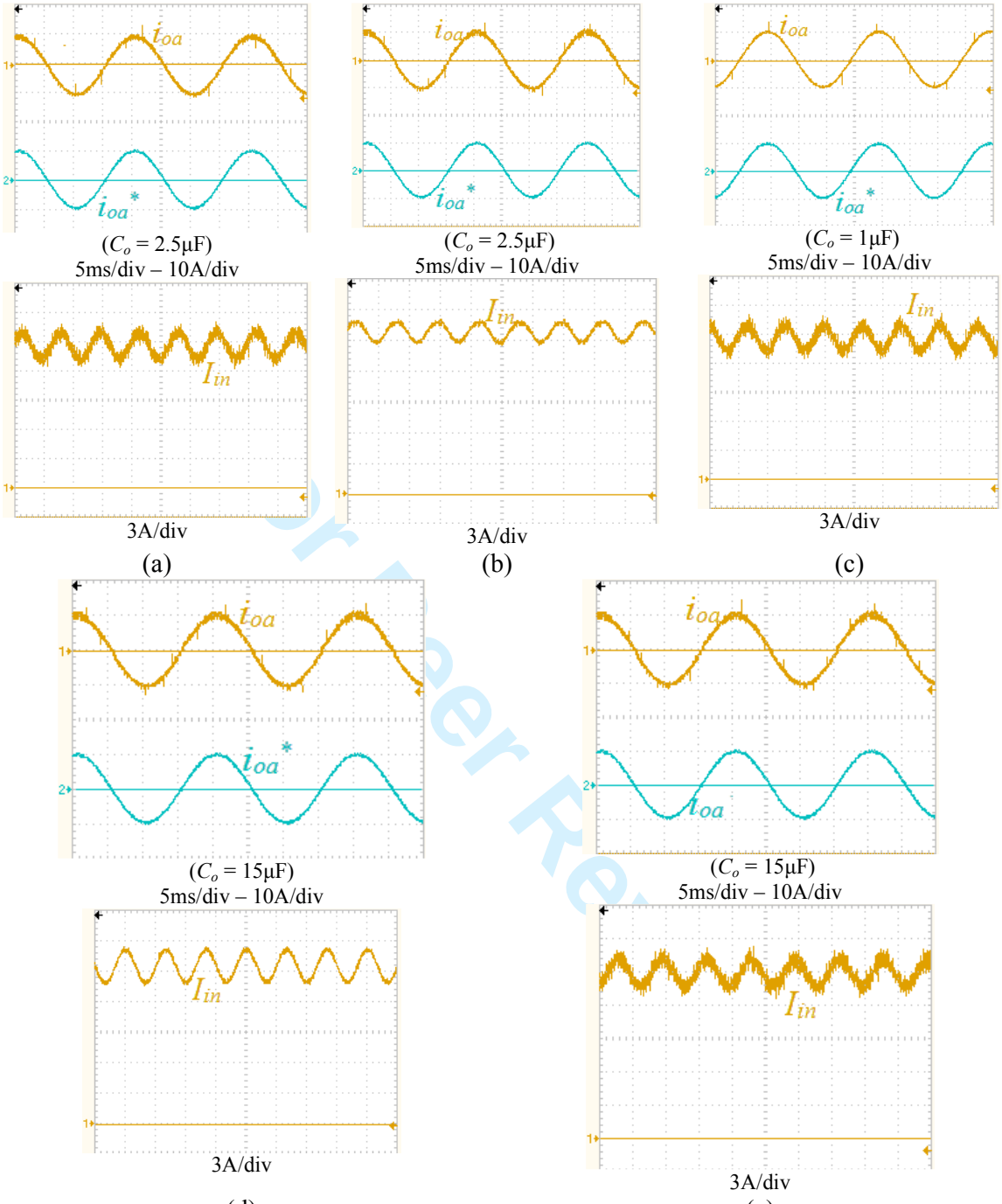


Fig.12. Operation of three-phase buck-boost DM-CSIs with Loop 1 + Loop 2: (a) C5, (b) D1, (c) D2, (d) F5, and (e) G5

Unlike Loop 1, fast dynamics for Loop 2 is not pressing. Therefore, K_{r2} is selected much lower than K_{r1} in order not to conflict Loop 1 performance.

$$F_2(s) = \frac{a_2 s}{\frac{1}{(4\pi f)^2} s^2 + a_2 s + 1} \tag{10}$$

$$G_{c2}(s) = \frac{K_{r2} s}{s^2 + 4\omega_o^2} \tag{11}$$

Fig.12 shows the experimental operation of Loop 1 and Loop 2 when the second order output harmonic current component is suppressed to less than 1% in all five cases.

3. Loop 3

From Fig.12, all the DM-CSIs suffer from a third order oscillating current component in the input dc current. This comes from the fact that the input currents (i_{ina}, i_{inb}, and i_{inc}) all have in-phase third order harmonic current components that sum up to the input dc current. As with the second order components in the three-phase output current, the third order component in the input dc current increases with higher passive elements values. If the third order current component in the input dc current I_{in} is expressed as:

$$i_{in3}(t) = I_{in3} \sin(3\omega t + \lambda) \tag{12}$$

then the oscillating power in the dc side is:

$$Q_{3in}(t) = V_{in} \quad i_{in3}(t) = V_{in} \quad I_{in3} \sin(3\omega t + \lambda) \tag{13}$$

Instead of oscillating in the input side, this oscillating power can be stored in the output capacitor C_o. As shown in Fig.13, each C_o has an additional third order harmonic voltage component $v_3(t)=V_3 \sin(3\omega+\varphi)$. Being co-phasal, the voltage $v_3(t)$ is not seen by the output load.

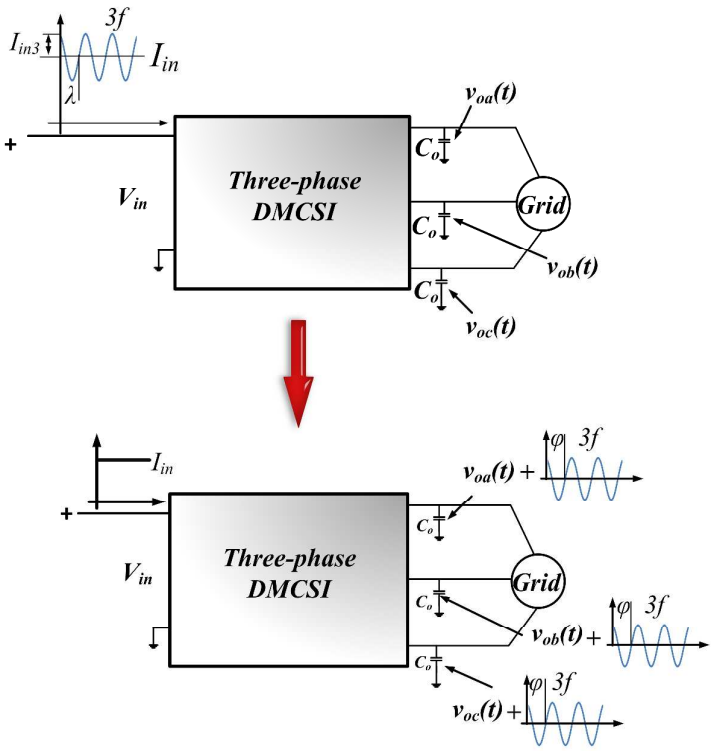


Fig.13. Elimination of the third harmonic current component in the input dc current I_{in}.

In order to supress Q_{in3}, the total instantaneous power across the output capacitors is:

$$Q_{3out}(t) = 9\omega\, C_o V_m V_3 \cos(3\omega t + \varphi) = -\, Q_{3in}(t) \tag{14}$$

Solving (13) and (14) yields:

$$V_3 = \frac{V_{in} I_{in3}}{9\omega V_m C_o}$$
$$\varphi = \lambda - \tfrac{3}{2}\pi \tag{15}$$

The feed-forward duty ratio δ_{3FF}, shown in Fig. 6, can be calculated as:

$$\delta_{3FF} = \frac{v_3(t)}{V_{in} + v_3(t)} \tag{16}$$

The function of the resonant controller $G_{c3}(s)$ is to fix the small error arising from the calculations in (15) and (16). Therefore, the gain K_{r3} can be selected much lower than K_{r1} in order not to interfere with the main loop. Fig.14 shows the experimental results when Loop 3

is added to the control system, where the input current third order harmonic components of the five inverters are suppressed.

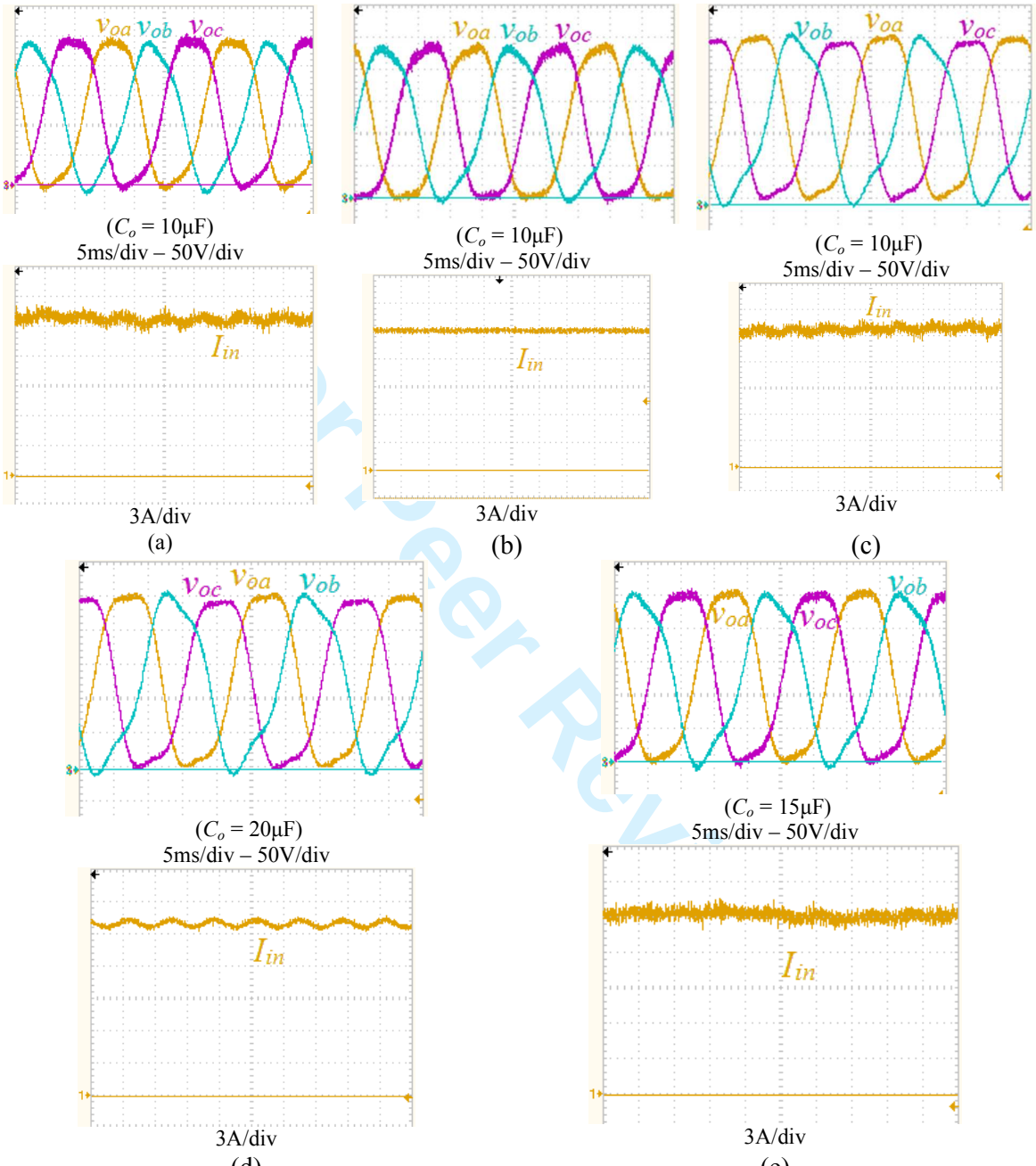


Fig.14. Operation of the three-phase buck-boost DM-CSIs with Loop 1 + Loop 2 + Loop 3: (a) C5, (b) D1, (c) D2, (d) F5, and (e) G5.

V. INVERTER ISOLATION

For reasons related to noise mitigation, electromagnetic compatibility and insulation, galvanic isolation between the input and output of the power converters is necessary in many applications [36]. Some of the proposed inverters can be modified to offer the possibility for transformer coupling and isolation. Generally, there are two main methods for power converters transformer coupling. In the first, a magnetic core temporarily stores the energy and then releases it to the output side [37]. However, the maximum transferred energy is limited by core volume as it equals $\frac{1}{2}BH\times$Volume. In the second method, the magnetic energy is transferred through instantaneous transformer action rather than being temporary stored in an intermediate magnetic circuit and then released. Thus, relatively small core volume can be used, where Faraday's equation, $v=Nd\varphi/dt$, is applicable.

i. Considering the case of a typical *G5* converter, the differences between the two methods is shown in Fig.15a. In Fig.15b, the energy is temporarily stored in the magnetic isolation transformer. Although the average voltage across the transformer is zero in *G5* in Fig.15b, the transformer core is exposed to a dc bias current and flux because of the stored energy; thus, the core volume (for a given current ripple) is increased. Such dc current bias increases core power loss and decreases its maximum current utilization.

ii. The series energy transfer intermediate capacitor can be split into two and placed at both sides of the isolation the transformer as shown in Fig.15c. The energy transfer from the input to the output is achieved instantaneously, without energy storage in the transformer core.

With the two methods, the average voltage across the transformer is zero. If the turns ratio N_2/N_1 is greater than 1, the converter voltage output V_o can be increased to offer a higher voltage range. Of the known 33 single-switch single diode power converters in [34], seven converters, all buck-boost, can be isolated using a high frequency transformer (those with

single element shunt paths and a shunt inductor [temporary storage action] and/or series capacitor[transformer action]), of which three have continuous input current, namely C5, F5, and G5; see Table III.

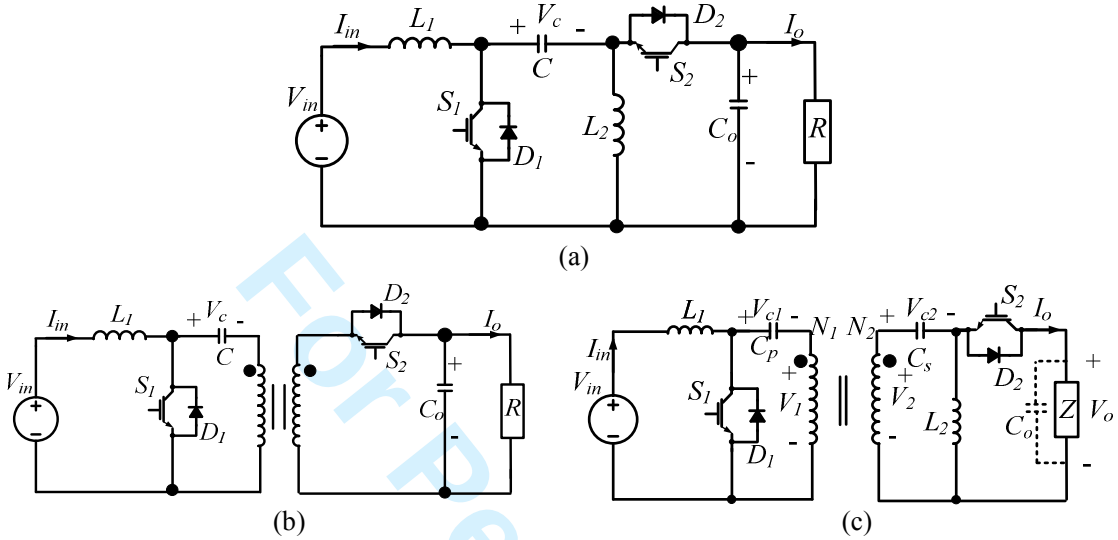
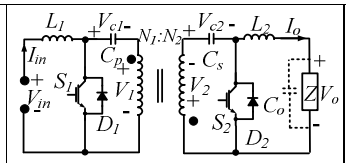
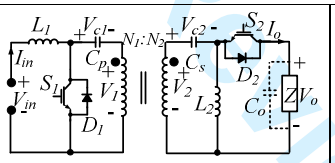
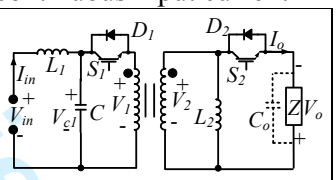


Fig.15. G5 converter: (a) non-isolated converter, (b) magnetic storage coupling, and (c) instantaneous transformer coupling.

TABLE III Transformer-isolated buck-boost converters with continuous input current

Topology			
	C5	G5	F5
Coupling Method	Instantaneous energy transfer	Instantaneous energy transfer	Temporarily stored energy
Current bias	0	0	I_{in}
Split-Capacitor Voltages	$V_{c1} = V_{in}$, $V_{c2} = V_o$	$V_{c1} = V_{in}$, $V_{c2} = 0$	-

The three buck-boost DM-CSIs having HFL isolated abilities are shown in Fig.16. Experimental comparison between the efficiencies of non-isolated and isolated versions of the three inverters is presented in Fig.17. The transformer core is a nano-crystalline material

which has high permeability (high magnetising inductance) and low leakage inductance. However, from Fig.4d, F5 has the preferable advantages of low input current ripple. But increased load current reduces the total inverter efficiency more than in C5 and G5 because of the core dc-bias current and average net core flux. The transformer action of C5 and G5 offers higher efficiencies than with the energy storage action of F5.

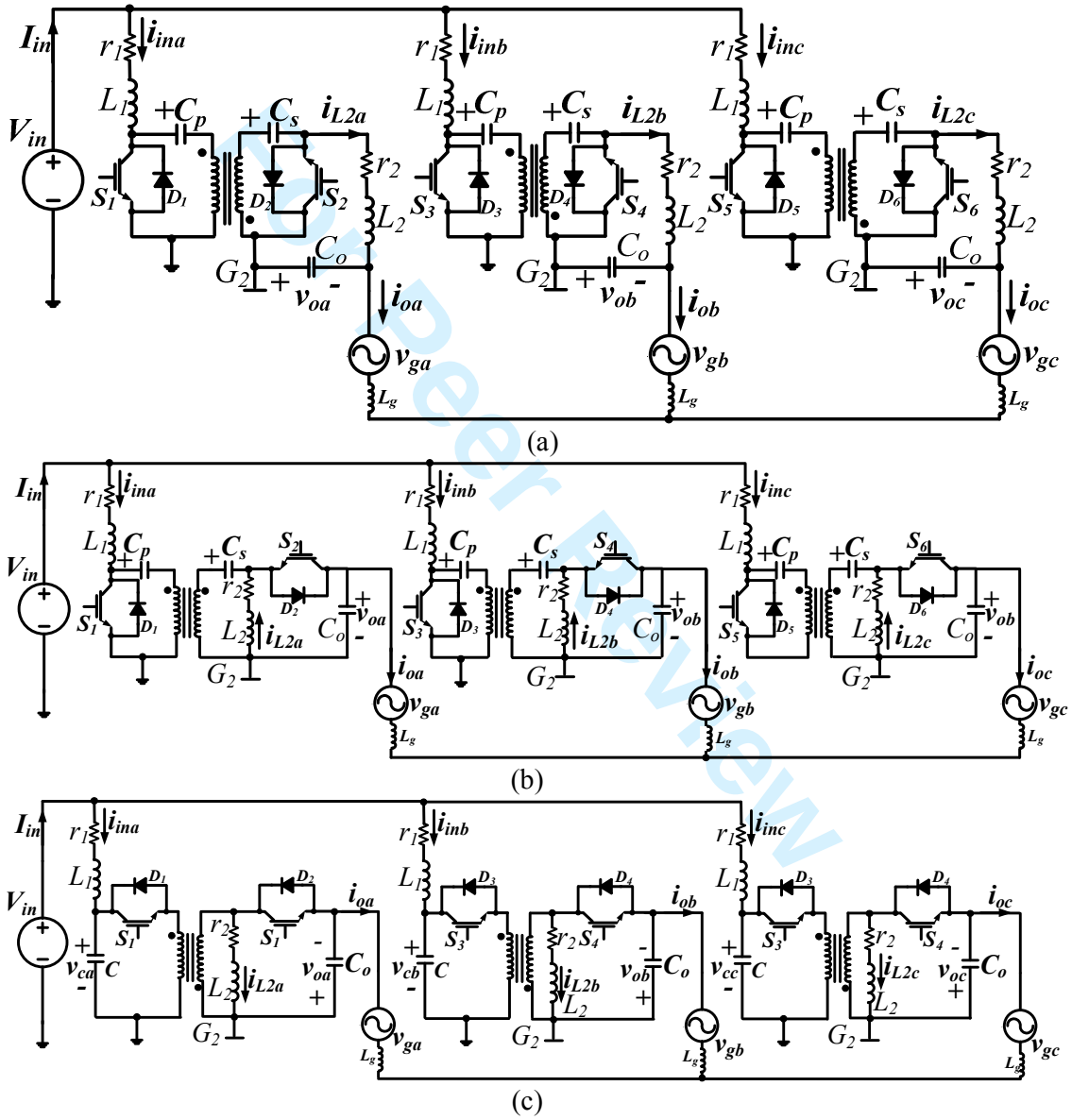


Fig.16. HFL isolated three-phase buck-boost DM-CSIs: (a) C5, (b) G5, and (c) F5.

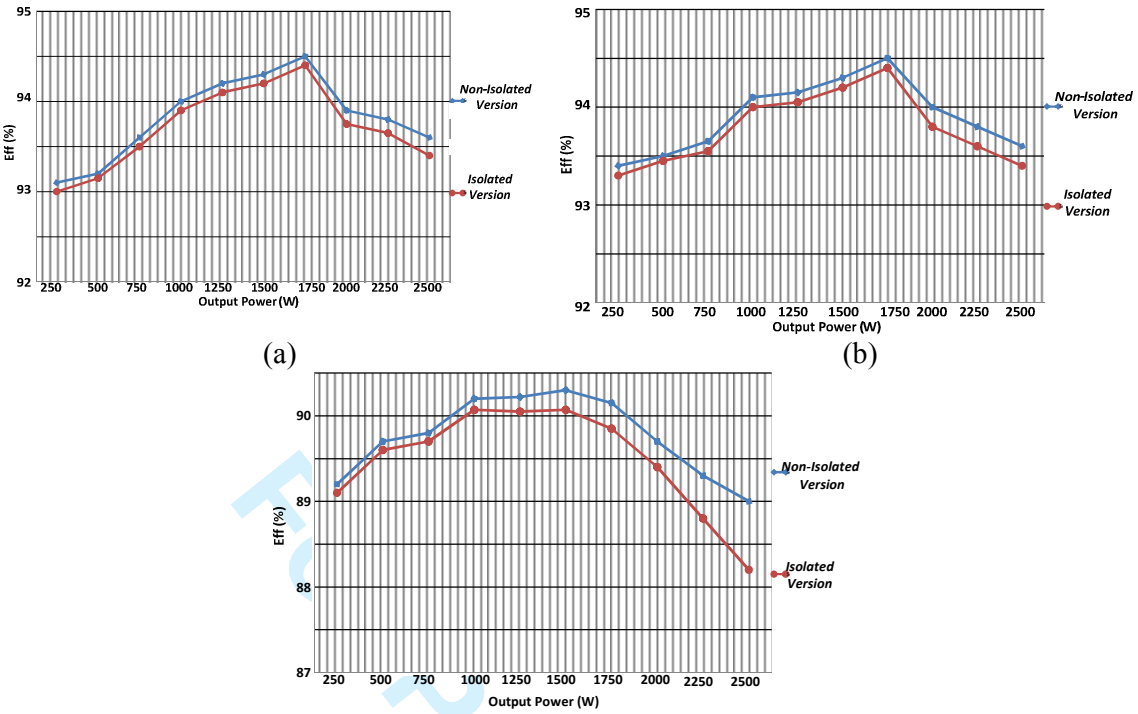


Fig.17. Experimental efficiencies of isolated and non-isolated versions of buck-boost three-phase DM-CSIs: (a) C5, (b) G5, and (c) F5.

VI. CONCLUSION

The paper investigated three-phase buck-boost inverters based on three differentially-connected reversible converters which have advantages when embedded in renewable energy generation systems. The presented DM-CSIs provide a flexible output voltages range as well as continuous input currents. This means the total dc side ripple current is low, (without recourse to electrolytic capacitor filtering), which is an important feature for MPPT techniques used in renewable energy systems.

A comparison between the DM-CSIs highlighted their main differences. The C5 and G5 based inverters have the lowest power loss and hence the best efficiencies. However, they experience higher input current ripple and may require higher input inductor values. Converters D1 and F5 have good efficiency at higher input dc voltages while the efficiency deteriorates at lower input voltages. The efficiency of D2 is lower than D1 and F5 at high input voltage and is better when the input voltage is lowered. In terms of device rating, the all

five inverters topologies have the same performance. Using the same passive element values, D2 inverter is found to have the lowest THD in the output voltage and current waveforms. D1 and F5 inverters have very low input ripple current, which is an attractive feature for PV systems. F5 and G5 inverters have the lowest capacitor voltage stresses and hence smaller and cheaper capacitors can be used.

The main challenge of DM-CSI implementation is that they are non-linear converters where the dynamics depend on the operation point and duty ratio. This high order transfer function hampers easy classical control design. Accordingly, the inverters investigated suffer from negative sequence second order harmonic in the output current, which affect the output current THD and hence, require larger output filters, and third order harmonic in the total input dc side current, which affects the MPPT techniques of the input sources.

Three control loops to control the fundamental currents and voltages and to remove the mentioned input and output currents distortion were implemented. The control design can effectively improve the operation and response of the different DM-CSIs. Finally, high-frequency transformer isolation methods for three-phase buck-boost DM-CSIs were investigated. In the first method, the inverter is isolated by small-size cores and the energy is transferred between the input and output sides instantaneously by transformer action. In the second method, part of the energy is temporarily stored in the coupling circuit core which requires larger cores. The generated topologies and their operation as isolated inverters were illustrated. Comparison between the efficiency of the isolated and non-isolated versions showed the coupled version suffers higher core losses which decrease efficiency.

APPENDIX

A.1 Power loss in the semiconductor devices

The rated power of the inverters investigated is 2.5 kW. For all three-phase buck-boost DM-CSIs, the current through devices S_1-D_1 (which is the same for S_3-D_3 and S_5-D_5), is shown in Fig.A1.

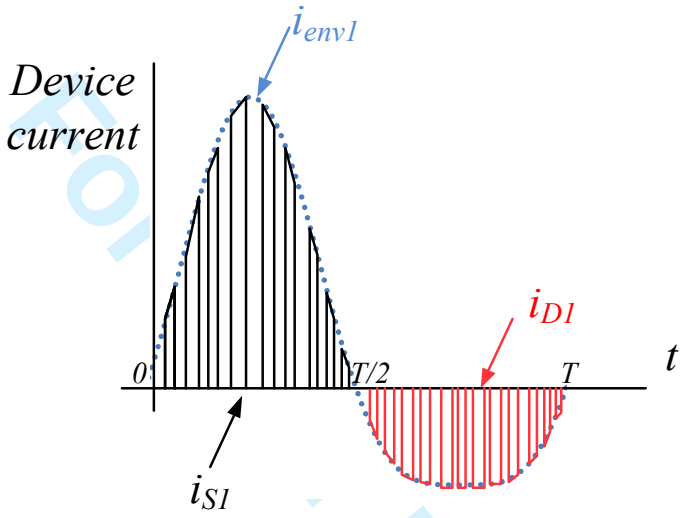


Fig.A1. Devices S_1-D_1 current.

The envelope of the switch current can be expressed as:

$$i_{inv1}(t) = \frac{1}{1-\delta_a} i_o \tag{A.1}$$

The rms value of the switch current i_{s1} is:

$$I_{s1(rms)}^2 = \frac{1}{T}\int_0^{T/2} (i_{s1})^2 . \, dt = \frac{1}{T}\int_0^{T/2} (i_{env1})^2 . \, \delta_a . \, dt \tag{A.2}$$

$$\delta_a = \frac{V_{dc} + V_m \sin\omega t}{V_{dc} + V_m \sin\omega t + V_{in}} \tag{A.3}$$

$$I_{s1(rms)}^2 = \left(\frac{I_o}{V_{in}}\right)^2 \{V_{in}(¼V_{dc} + 0.1061\, V_m(\cos^2\gamma + 1)) + 0.2122\, V_m V_{dc}(\cos^2\gamma + 1) + V_m^2(1/16 + ⅛\cos^2\gamma) + ¼V_{dc}^2 \tag{A.4}$$

If the inverter operates at unity power factor (γ = 0º) and $V_{dc} = V_m$, then (A.4) yields:

$$I_{s1(rms)}^2 = \frac{V_m I_o^2 (0.4622\ V_{in} + 0.8619\ V_m)}{V_{in}^2} \tag{A.5}$$

The average value of the diode current i_{D1} is calculated from:

$$\begin{aligned} \bar{I}_{D1} &= \frac{1}{T}\int_{T/2}^{T} (i_{D1}).\ dt = \frac{1}{T}\int_{T/2}^{T} (i_{inv1})\ dt = \frac{1}{T}\int_{T/2}^{T} \left(\frac{\delta_a}{1-\delta_a} i_o\right) dt \\ &= \frac{V_m I_o (4-\pi)}{4\pi V_{in}} \end{aligned} \tag{A.6}$$

The power loss in device S_1-D_1 can be approximated as:

$$P_{device1} = R_{on}\ I_{s1(rms)}^2 + \bar{I}_{D1}\ V_{DF} \tag{A.7}$$

The current through S_2-D_2 , (and S_4-D_4 and S_6-D_6), is shown in Fig.A2.

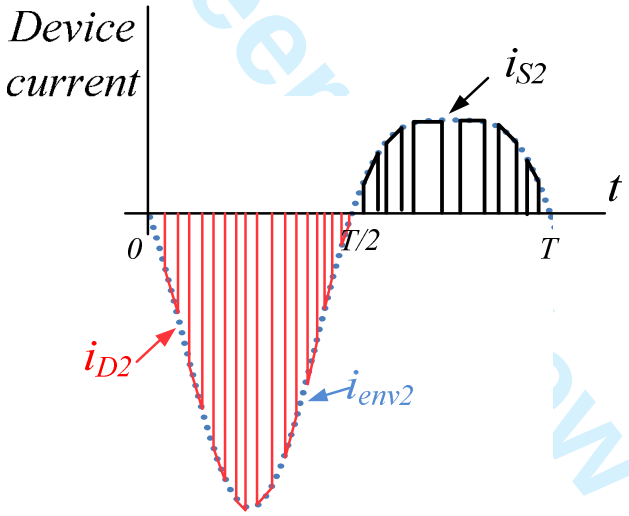


Fig.A2. Device S_2-D_2 current.

The envelope of the switch current can be expressed as:

$$i_{inv\,2}(t) = \frac{-1}{1-\delta_a} i_o \tag{A.8}$$

The rms value of the switch current i_{s1} is:

$$I_{s1(rms)}^2 = \frac{1}{T}\int_{T/2}^{T} (i_{s2})^2\ .\ dt = \frac{1}{T}\int_{T/2}^{T} (i_{env2})^2\ .\ (1-\delta_a).\ dt \tag{A.9}$$

$$I_{s2(rms)}^2 = I_o{}^2[\frac{1+V_{dc}/V_{in}}{4} + \frac{V_m}{V_{in}}(0.0266\ \cos 2\gamma - 0.0796 - \frac{\cos^2\gamma}{2\pi})] \quad \text{(A.10)}$$

If the inverter operates at unity power factor ($\gamma = 0^o$) and $V_{dc} = V_m$, then (A.10) yields:

$$I_{s2(rms)}^2 = I_o{}^2(¼ + \frac{0.0378\ V_m}{V_{in}}) \quad \text{(A.11)}$$

The average value of the diode current i_{D1} is calculated from:

$$\bar{I}_{D2} = \frac{1}{T}\int_0^{T/2}(i_{D2}).\ dt = \frac{1}{T}\int_0^{T/2}(i_{inv2})\ dt = \frac{1}{T}\int_0^{T/2}(i_o)\ dt = \frac{I_o}{\pi} \quad \text{(A.12)}$$

The power loss in the S_2-D_2 can be approximated as:

$$P_{device2} = R_{on}\ I_{s2(rms)}^2 + \bar{I}_{D2}\ V_{DF} \quad \text{(A.13)}$$

A.2 Power loss in the inductors

The currents through inductors L_1 and L_2 can be expressed as functions of the output current, voltage and duty ratio, as shown in TABLE A.1. The quantity $\frac{1}{1-\delta}$ is always greater than 1 while $\frac{\delta}{1-\delta}$ is greater than 1 when $\delta > 0.5$ and less than 1 when $\delta < 0.5$.

TABLE A.1 CONVERTER INDUCTOR CURRENTS

Topology	Current through L_1 i_{L1}	Current through L_2 i_{L2}
C5	$\frac{\delta}{1-\delta} i_o = i_{in}$	i_o
D1	$\frac{\delta}{1-\delta} i_o = i_{in}$	$\frac{1}{1-\delta} i_o$
D2	$\frac{1}{1-\delta} i_o = i_{in} \diagup \delta$	i_o
F5	$\frac{\delta}{1-\delta} i_o = i_{in}$	$\frac{1}{1-\delta} i_o$
G5	$\frac{\delta}{1-\delta} i_o = i_{in}$	i_o

For the first phase, as an example, the quantities $\frac{\delta_a}{1-\delta_a} i_o$ and $\frac{1}{1-\delta_a} i_o$ can be expressed as:

$$\frac{\delta_a}{1-\delta_a} i_o(t) = \frac{V_m I_o}{2\ V_{in}} + \frac{V_m I_o}{V_{in}} \sin \omega t - \frac{V_m I_o}{2\ V_{in}} \cos 2\omega t \quad \text{(A.14)}$$

$$\frac{1}{1-\delta_a} i_o(t) = \frac{V_m I_o}{2\ V_{in}} + I_o(1 + \frac{V_m}{V_{in}}) \sin \omega t - \frac{V_m I_o}{2\ V_{in}} \cos 2\omega t \quad \text{(A.15)}$$

Then the copper losses of the different DM-CSIs are listed in TABLE A.2.

TABLE A.2 COPPER LOSSES

Type	Copper losses / r	
	L_1	L_2
C5	$\frac{7V_m^2 I_o^2}{8V_{in}^2}$	$½I_o^2$
D1	$\frac{7V_m^2 I_o^2}{8V_{in}^2}$	$I_o^2[\left(\frac{7V_m}{8V_{in}} + 1\right) + ½]$
D2	$I_o^2[\left(\frac{7V_m}{8V_{in}} + 1\right) + ½]$	$½I_o^2$
F5	$\frac{7V_m^2 I_o^2}{8V_{in}^2}$	$I_o^2[\left(\frac{7V_m}{8V_{in}} + 1\right) + ½]$
G5	$\frac{7V_m^2 I_o^2}{8V_{in}^2}$	$½I_o^2$

A.3 Input current ripple

The input ripple current of the DM-CSIs are listed in TABLE A.3

TABLE A.3 INPUT CURRENT RIPPLE

Topology	p-p
C5	$\frac{2.88V_m V_{in} t_s}{L_1(1.44V_p + V_{in})}$
D1	$\frac{0.72V_m V_{in} I_o {t_s}^2}{L_1 C(1.44V_m + V_{in})^2}$
D2	$\frac{2.88V_m V_{in} t_s}{L_1(1.44V_p + V_{in})}$
F5	$\frac{0.72V_m V_{in} I_o {t_s}^2}{L_1 C(1.44V_m + V_{in})^2}$
G5	$\frac{2.88V_m V_{in} t_s}{L_1(1.44V_p + V_{in})}$

A.4 Transfer function G(s)

(a) C5

$$G(s) = \frac{\tilde{V}_o(s)}{\delta(s)} = \frac{a_2 s^2 + a_1 s + a_0}{b_3 s^3 + b_2 s^2 + b_1 s + b_0}$$

$$\begin{aligned}
a_2 &= CR(1 - D_e)L_1 V_{in} \\
a_1 &= V_{in}(-L_1 {D_e}^2 + CRr_1(1 - D_e)) \\
a_0 &= V_{in}(R(1 - D_e)^2 - {D_e}^2 r_1) \\
b_3 &= CL_1 L_2(1 - D_e)^2 \\
b_2 &= CL_1(R + r_2 + {D_e}^2 r_2 - 2D_e(R + r_2) + {D_e}^2 R) + CL_2 r_1(1 - D_e)^2 \\
b_1 &= L_1({D_e}^2 - 2{D_e}^3 + {D_e}^4) + L_2(1 + 6{D_e}^2 - 4{D_e}^3 + {D_e}^4 - 4D_e) \\
&\quad + CRr_1(1 + {D_e}^2) + Cr_1 r_2(1 + {D_e}^2) - 2CD_e r_1(R + r_2) \\
b_0 &= R(1 - D_e)^4 + r_1 {D_e}^2(1 - D_e)^2 + r_2(1 - D_e)^4
\end{aligned} \tag{A.16}$$

(b) D1

$$G(s) = \frac{\tilde{V}_o(s)}{\delta(s)} = \frac{a_2 s^2 + a_1 s + a_0}{b_3 s^3 + b_2 s^2 + b_1 s + b_0}$$

$$\begin{aligned}
a_2 &= CR(1-D_e)L_1 V_{in} \\
a_1 &= V_{in}(-D_e(L_2 + L_1 D_e) + CRr_1(1-D_e)) \\
a_0 &= -RV_{in}(1-D_e)^2 - D_e V_{in}(r_2 + r_1 D_e) \\
b_3 &= CL_1 L_2 (1-D_e)^2 \\
b_2 &= C(1-D_e)^2 [L_1(R+r_2) + L_2(R+r_1)] \\
b_1 &= (1-D_e)^2 [(L_2 + L_1 D_e^2) + CR(r_1 + r_2) + Cr_1 r_2] \\
b_0 &= (1-D_e)^2 [R(1-D_e)^2 + (r_2 + r_1 D_e^2)]
\end{aligned} \tag{A.17}$$

(c) D2

$$G(s) = \frac{\tilde{V}_o(s)}{\delta(s)} = \frac{a_1 s + a_0}{b_3 s^3 + b_2 s^2 + b_1 s + b_0}$$

$$\begin{aligned}
a_1 &= -D_e V_{in} L_1 \\
a_0 &= V_{in}[R(1-D_e)^2 - r_1 D_e] \\
b_3 &= CL_1 L_2 (1-D_e)^2 \\
b_2 &= C(1-D_e)^2 [L_1(R+r_2) + L_2 r_1] \\
b_1 &= (1-D_e)^2 [L_1 + L_2(1-D_e)^2 + Cr_1 r_2 + CRr_1] \\
b_0 &= (1-D_e)^2 [(R+r_2)(1-D_e)^2 + r_1]
\end{aligned} \tag{A.18}$$

(d) F5

$$G(s) = \frac{\tilde{V}_o(s)}{\delta(s)} = \frac{a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_3 s^3 + b_2 s^2 + b_1 s + b_0}$$

$$\begin{aligned}
a_3 &= C\ D_e L_1^2 L_2 V_{in} \\
a_2 &= -C\ D_e V_{in}[(L_1 r_2 + L_2 r_1) + L_1 R(2-D_e)] \\
a_1 &= -V_{in}[D_e L_1 (D_e L_1 + Cr_1 r_2 + L_2) - CL_2 Rr_1 (1-D_e)^2] \\
a_0 &= V_{in}[R(1-D_e)^2 - D_e(D_e r_1 + r_2)] \\
b_4 &= C\ C_o L_1^2 L_2 R(1-D_e)^2 \\
b_3 &= CL_1(1-D_e)^2 [L_1 L_2 + C_o R(L_1 r_2 + L_2 r_1)] \\
b_2 &= L_1(1-D_e)^2 [CL_1 R(1-D_e)^2 + C(L_1 r_2 + L_2 r_1) + C_o(L_2 R + D_e^2 + CRr_1 r_2)] \\
b_1 &= L_1(1-D_e)^2 [L_2 + D_e^2 L_1 + CRr_1(1-D_e)^2 + C_o R(r_1 D_e^2 + r_2)] \\
b_0 &= (1-D_e)^2 [R(1-D_e)^2 + r_2 + r_1 D_e^2]
\end{aligned} \tag{A.19}$$

(e) G5

$$G(s) = \frac{\tilde{V}_o(s)}{\delta(s)} = \frac{a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_3 s^3 + b_2 s^2 + b_1 s + b_0}$$

$$\begin{aligned}
a_3 &= -CD_e L_1 L_2 V_{in} \\
a_2 &= CRV_{in}(1-D_e)^2(L_1+L_2) \\
a_1 &= C\ RV_{in}(1-D_e)^2(r_1+r_2) - CD_e V_{in} r_1 r_2 - D_e^2 L_1 V_{in} \\
a_0 &= RV_{in}(1-D_e)^2 - D_e^2 V_{in}\, r_1 \\
b_4 &= CC_o L_1 L_2 R(1-D_e)^2 \\
b_3 &= CL_1 L_2(1-D_e)^2 + CC_o R(1-D_e)^2[r_1 L_2 + r_2 L_1] \\
b_2 &= CR(1-D_e)^4(L_1+L_2) + C_o L_2 R(1-D_e)^4 + C_o L_1 R D_e^2 (1-D_e)^2 \\
&\quad + C(1-D_e)^2(L_1 r_2 + L_2 r_1) + CC_o R r_1 r_2 (1-D_e)^2 \\
b_1 &= L_2(1-D_e)^4 + L_1 D_e^2 (1-D_e)^2 + CR(r_1+r_2) + \\
&\quad C_o(1-D_e)^2[(1-D_e)^2 + Rr_1] + CR(1-D_e)^4[r_1+r_2] + Cr_1 r_2(1-D_e)^2 \\
b_0 &= (1-D_e)^4(R+r_2) + r_1 D_e^2 (1-D_e)^2
\end{aligned} \tag{A.20}$$

References

[1] P. Mazumdar, P. N. Enjeti, and R. S. Balog, "Analysis and Design of Smart PV Modules," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 2, pp. 451-459, 2014.

[2] M. Amirabadi, H. A. Toliyat, and W. C. Alexander, " A Multiport AC Link PV Inverter With Reduced Size and Weight for Stand-Alone Application," IEEE Transactions on Industry Application, vol. 49, no.5, pp. 2217-2228, 2013.

[3] S. Chakraborty, B. Kramer, and B. Kroposki, "A review of power electronics interfaces for distributed energy systems towards achieving lowcost modular design," Renewable Sustain. Energy Rev., vol. 13, no. 9, pp. 2323–2335, Dec. 2009.

[4] C.T. Pan and J.J. Shieh, "A single-stage three-phase boost–buck AC/DC converter based on generalized zero-space vectors," IEEE Transactions on Power Electronics , vol. 14, pp. 949–958, Sept. 1999.

[5] D.S. Wijeratne, and G. Moschopoulos "A Comparative Study of Two Buck-Type Three-Phase Single-Stage AC–DC Full-Bridge Converters," IEEE Transactions on Power Electronics , vol.29, no.4, pp.1632,1645, April 2014

[6] P. Sun, C. Liu, Jih-Sheng Lai, C. Chen, and N. Kees, "Three-Phase Dual-Buck Inverter With Unified Pulsewidth Modulation," IEEE Transactions on Power Electronics, vol.27, no.3, pp.1159,1167, March 2012

[7] Ching-Tsai Pan, and Jenn-Jong Shieh, "New space-vector control strategies for three-phase step-up/down AC/DC converter", IEEE Transactions on Industrial Electronics, vol.47, no.1, pp.25, 2000

[8] J. Kikuchi, and T.A. Lipo, "Three-phase PWM boost-buck rectifiers with power-regenerating capability", IEEE Transactions on Industry Applications, vol.38, no.5, pp.1361, 2002

[9] Yang Chen, and K. Smedley, "Three-Phase Boost-Type Grid-Connected Inverter," IEEE Transactions on Power Electronics, vol.23, no.5, pp.2301,2309, Sept. 2008

[10] B. Sahan, S.V. Araújo, C. Nöding, and P. Zacharias, "Comparative Evaluation of Three-Phase Current Source Inverters for Grid Interfacing of Distributed and Renewable Energy Systems", IEEE Transactions on Power Electronics, p.p 2304 - 2318 vol.26, no., Aug. 2011

[11] E. Twining, and D. G. Holmes "Grid Current Regulation of a Three-Phase Voltage Source Inverter With an LCL Input Filter," IEEE Transactions on Power Electronics, vol. 18, no. 3, pp. 888-895, 2003.

[12] P. C. Loh, and D. G. Holmes "Analysis of Multiloop Control Strategies for LC/CL/LCL-Filtered Voltage-Source and Current-Source Inverters," IEEE Trans. Industry Applications, vol. 41, no. 2, pp. 644-654, 2005.

[13] Y. Bae and R. Y. Kim, "Suppression of common-mode voltage using a multicentral photovoltaic inverter topology with synchronized PWM," IEEE Transactions on Industrial Electronics., vol. 61, no. 9, pp. 4722–4733, Sep. 2014.

[14] Bo Yang, W. Li, Yunjie Gu, W. Cui, and X. He, "Improved Transformerless Inverter With Common-Mode Leakage Current Elimination for a Photovoltaic Grid-Connected Power System," IEEE Transactions on Power Electronics, vol. 27, no. 2, pp. 752–762, 2012.

[15] J. Zeng, W. Qiao; L. Qu, and Y. Jiao "An Isolated Multiport DC–DC Converter for Simultaneous Power Management of Multiple Different Renewable Energy Sources", *IEEE Journal of Emerging and Selected Topics in Power Electronics,* pp. 70 - 78 vol. 2, no. 1, March 2014

[16]] J. A. Pomilio and G. Spiazzi, "High-precision current source using low loss, single-switch, three-phase AC/DC converter," IEEE Transactions on Power Electronics, vol. 11, no. 4, pp. 561–566, Jul. 1996.

[17] U. R. Prasanna and A. K. Rathore, "A Novel Single-Reference Six-Pulse Modulation (SRSPM) Technique-Based Interleaved High-Frequency Three-Phase Inverter for Fuel Cell Vehicles," IEEE Transactions on Power Electronics, vol. 28, no. 12, pp. 5547–5556, Dec. 2013.

[18] N. Mohan and S. Gandikota, "High frequency ac-link transformer isolated three phase inverter with natural commutation of leakage energy," in 7th IET International Conference on Power Electronics, Machines and Drives (PEMD 2014), 2014, pp. 1.10.03–1.10.03.

[19] "Reliability Prediction for Electronic Equipment," Doc. MIL-HDBK- 217X, United States Dept. Defence, Washington, DC, Dec. 1991.

[20] M. Hongbo, L. Jih-Sheng, F. Quanyuan, Y. Wensong, Z. Cong, and Z. Zheng, "A Novel Valley-Fill SEPIC-Derived Power Supply Without Electrolytic Capacitor for LED Lighting Application," IEEE Transactions on Power Electronics, vol. 27, pp. 3057-3071, 2012.

[21] S. Y. R. Hui, L. Si Nan, T. Xue Hui, C. Wu, and W. M. Ng, "A Novel Passive Offline LED Driver With Long Lifetime," IEEE Transactions on Power Electronics, vol. 25, pp. 2665-2672, 2010.

[22] S. Mehrnami and S. K. Mazumder, "Discontinuous Modulation Scheme for a Differential-Mode Cuk Inverter," IEEE Transactions on Power Electronics, vol. 30, pp. 1242-1254, 2015.

[23] R. O. Caceres and I. Barbi, "A boost DC-AC converter: analysis, design, and experimentation," IEEE Transactions on Power Electronics, vol. 14, pp. 134-141, 1999.

[24] A. Darwish, D. Holliday, S. Ahmed, A. M. Massoud, and B. W. Williams, "A Single-Stage Three-Phase Inverter Based on Cuk Converters for PV Applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 2, pp. 797-807, 2014.

[25] J. M. A. Myrzik, "Novel inverter topologies for single-phase stand-alone or grid-connected photovoltaic systems," in *Power Electronics and Drive Systems, 2001. Proceedings., 2001 4th IEEE International Conference on*, 2001, pp. 103-108 vol.1.

[26] F. Z. Peng, "Z-source inverter," IEEE Tansactions on Industry Applications, vol. 39, no. 2 pp. 504-510, April 2003

[27] C. Daolian and W. Guoling, "Differential Buck DC-DC Chopper Mode Inverters With High-Frequency Link," IEEE Transactions on Power Electronics, vol. 26, pp. 1444-1451, 2011.

[28] J. Minsoo, M. Ciobotaru, and V. G. Agelidis, "A Single-Phase Grid-Connected Fuel Cell System Based on a Boost-Inverter," IEEE Transactions on Power Electronics, vol. 28, pp. 279-288, 2013.

[29] J. Knight, S. Shirsavar, and W. Holderbaum, "An improved reliability Cuk based solar inverter with sliding mode control," IEEE Transactions on Power Electronics, vol. 21, pp. 1107-1115, 2006.

[30] M. S. Diab, A. Elserougi, A. M. Massoud, A. S. Abdel-Khalik, and S. Ahmed, "A Four-Switch Three-Phase SEPIC-Based Inverter," IEEE Transactions on Power Electronics, vol. 30, pp. 4891-4905, 2015.

[31] P. R. Prasanna and A. K. Rathore, "Analysis, Design, and Experimental Results of a Novel Soft-Switching Snubberless Current-Fed Half-Bridge Front-End Converter-Based PV Inverter," IEEE Transactions on Power Electronics, vol. 28, pp. 3219-3230, 2013.

[32] R. D. Middlebrook and S. Cuk, "Isolation and multiple output extensions of a new optimum topology switching DC-to-DC converter," in *Power Electronics Specialists Conference, 1978 IEEE*, 1978, pp. 256-264.

[33] K. Hongrae, B. Parkhideh, T. D. Bongers, and G. Heng, "Reconfigurable Solar Converter: A Single-Stage Power Conversion PV-Battery System," IEEE Transactions on Power Electronics, vol. 28, pp. 3788-3797, 2013.

[34] B. W. Williams, "Generation and Analysis of Canonical Switching Cell DC-to-DC Converters," IEEE Transactions on Industrial Electronics, vol. 61, pp. 329-346, 2014

[35] A. H. El Khateb, N. Abd.Rahim, J. Selvaraj, and B. W. Williams, "DC-to-DC Converter With Low Input Current Ripple for Maximum Photovoltaic Power Extraction," IEEE Transactions on Industrial Electronics , vol. 62, pp. 2246-2256, 2015.

[36] Z. Jianwu, Q. Wei, and Q. Liyan, "An isolated multiport DC-DC converter for simultaneous power management of multiple renewable energy sources," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, 2012, pp. 3741-3748.

[37] R. W. Erickson and D. Maksimovic, "Fundamentals of Power Electronics," *University of Clorado*, 2001.