Maturing DC Protection Methods for the More-Electric Aircraft

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Abstract *With the increasing electrification of modern aircraft designs, there is a growing dependence on the aircraft's electrical power system for safe flight. Novel enabling technologies such as new converter topologies, DC power distribution and composite airframes however present challenging fault modes, which in turn require the application of new protection schemes and circuit breaking technologies. Hardware testing of such schemes is a critical stage of their maturation. This requires the use of dedicated protection rigs which capture key network elements influencing the system fault response and which can safely withstand full fault effects without risk of equipment damage. This paper presents such a protection rig being developed at the University of Strathclyde, designed to enable the evaluation and maturation of protection concepts and development of algorithms for compact DC aerospace power systems.*

Introduction

The increasing adoption of the more-electric aircraft concept has seen a growth in the proposed use of power electronic systems and DC power distribution in order to attain numerous benefits. These include higher end-to-end power transfer efficiency, reduced power system weight through increased power density, and greater system flexibility and reconfigurability. However, there are also significant safety challenges arising from an unconventional system fault response, which places challenging operating requirements on any protection systems employed.

This paper reviews these challenges and the associated requirements for network protection systems. It illustrates how these requirements are difficult to meet with existing protection approaches and circuit breaking technologies. Novel techniques which are fast acting and highly sensitive may offer a light weight solution to the challenges presented.

The paper argues that key to developing these and other protection solutions is extensive hardware testing on a dedicated protection testing rig which facilitates: the application of zero impedance short circuit faults, realistic circuit dynamics, representation of capacitive discharges, high bandwidth measurement and data logging, and repetitive testing on a readily reconfigurable compact DC network.

The paper then presents a newly developed protection rig at the University of Strathclyde. Key features of this rig are outlined before a case study is presented, demonstrating both its use and the potential benefits of a fast acting protection solution discussed earlier. The paper concludes by outlining the expansion plans for this rig to accommodate studies on larger networks and higher voltage testing.

Challenges of DC Systems Protection

Previous work from the authors has discussed and analysed the protection challenges of converter interfaced DC networks in depth [1, 2, 3]. The key points from these publications are summarised below.

First, references [1, 3] highlighted that the utilisation of converter interfaces between generation and the distribution network has the potential to significantly alter the protection system design requirements in future aircraft platforms. However, the impact these converters can vary widely, depending on the topology of converter, its filter requirements and its control strategy. This means that the precise impact on the network fault response is often difficult to quantify. Through the analysis of example converter topologies and literature on the protection of DC networks, [1] tackles this problem by identifying key design characteristics of converters which influence their fault response. Using this information, the converters are classified based on their general fault characteristics, enabling potential protection issues and solutions to be readily identified. From this broad converter classification, two aspects related to the network fault response consistently appear, albeit to varying degrees, as key issues to the protection of the network and converter. These issues are the potential for:

- Extremely high capacitive fault currents
- Reverse voltage conditions at converter terminals and the subsequent conduction of high currents through freewheeling diodes within the converter

These issues are particularly apparent for standard voltage source converter topologies. This converter topology and an example of the typical stages of its fault response are shown in Figs 1 and 2.

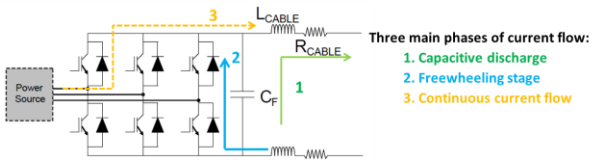

Fig 1. Standard six switch VSC converter

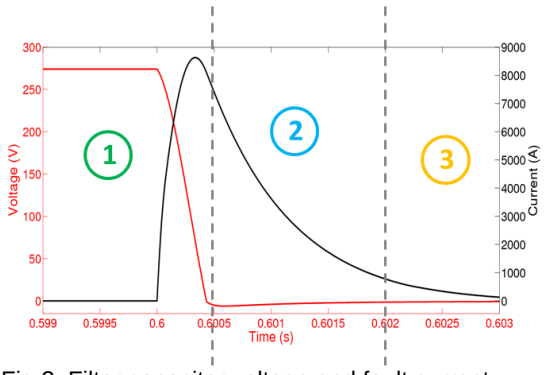

Fig 2. Filter capacitor voltage and fault current response to a short circuit fault applied at 0.6s

References [3] highlighted that various options exist to tackle these problems, with the uprating of components and use of suppression technologies within appropriate parts of a network the most immediately applicable. On longer timescale, one proposed longer term operating philosophy, which has the potential to resolve all of the above challenges, is to utilise fast acting protection in order to isolate a fault before any severe transient develops. In addition to overcoming the above protection issues, this approach also provides system design benefits as it is a potentially lightweight method (as it does not require any additional components unlike the suppression options), would minimise both damage to components and disruption to the rest of the network due to the early interruption of the fault and decrease energy at the point of fault (which is particularly significant for arc flash events). It is however a very challenging solution to implement and requires a much faster response than is currently implemented.

The two significant challenges for implementation are:

- The discrimination of fault location and coordination of protection devices within the required timeframe (sub millisecond operation may be required)
- Development of suitably rated and fast enough acting circuit breakers

The following section will first discuss the performance requirements of protection hardware to overcome these challenges. Later sections will then describe demonstration facilities and protection methods capable of meeting these strict requirements.

DC Protection Hardware Requirements for Practical Implementation

There are two discrete aspects to the protection hardware requirements. The first relates to the fault detection system – including sensors, data logging and control systems to host the appropriate protection algorithms. This system would represent the time taken from the measurement of network response to the issuing of protection trip signals when required. To execute this within the sub-millisecond time frame, performance requirements for hardware include:

- Multi-channel sensor output sampling of current (and voltage) in the MHz range to keep up with the ~100µs time to fault peak.
- FPGA or micro-processor capable of deploying control loops for the protection algorithms in the MHz range.

The specific requirements will depend on the dynamics of the target network however it is anticipated that these will be consistent across multiple voltage levels.

The second aspect of the protection system design is the physical circuit breakers themselves. Two key requirements are on the operating speed and the required rating of the devices. A review of circuit breaker technologies within [3] highlighted that solid state circuit breaking (SSCB) technology was the only option which enabled protection operation in the desired time frame, (alternative technologies considered were electro-mechanical and hybrid breakers). To achieve a very short operating time, the switching time of these SSCBs must be fully controllable. Therefore commercially available devices with slower acting pre-programmed protection functions [4] would not be suited to this application.

The required rating of the SSCB (both for breaking fault current as well as the ability to ride through faults when required) will depend heavily on its application and the voltage within which it is operating (as this will have a large impact on fault current level). The level of fault current which may be expected in a 270VDC system was illustrated in the previous section. Whilst the development of highly rated devices was not a key part of the work described in this paper (with the focus more on the deployment of SSCBs alongside fast acting detection systems as will be illustrated in later sections), the identification and/or development of appropriately rated devices is clearly important for practical implementation.

Hardware Environment for the Generation of Representative Fault Responses

The hardware demonstration of protection technologies within a representative faulted environment is an essential step in bridging the gap to an eventual application. For this purpose, a protection system evaluation rig has been developed at the University of Strathclyde. The rig set up was designed with a number of design features in mind and these include:

- A realistic fault response to test protection systems against (e.g. scaled magnitude but similar dynamics to Fig 1)
- Accommodation of zero impedance fault path switching for short circuit tests
- The ability to reconfigure the network to test protection schemes in different electrical architectures as well as providing variance in fault location
- The ability to vary fault conditions including fault impedance, different ground conditions and high impedance ground paths (e.g. for composite airframes)
- The ability to carry out repetitive fault tests to fully evaluate protection methods under test
- The ability to support algorithm development
- The ability to progress technologies under test to TRL 3/4

To allow these criteria to be fulfilled within a lab environment, the operating voltage should be chosen at a level which limits the potential danger and minimises cost for early prototyping work. The outline circuit diagram for the rig is shown in Fig 3. Details of the numbered items within this diagram are shown within Table 1.

As outlined in Table 1, a lab power supply was utilised to provide 18-30V supply that is in tune to aerospace 28Vdc (with subsystems intended to be scalable to higher voltages such as 270Vdc). The capacitance within this network (4) represents the capacitive output filter of a power converter. The lab setup is designed to be modular whereby the different electrical architectures can be tested using the same control setup. The control setup itself makes use of a

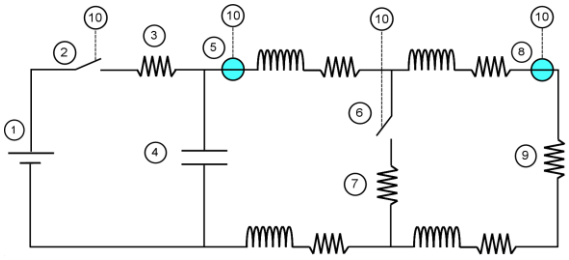

Fig 3. Outline circuit diagram for rig setup

Table 1: Details of experimental rig setup

No.	Function	Hardware	Experimental test settings
1	Power supply	30V, 2A Bench Power Supply	Set to 18V constant voltage
2	Disconnect supply prior to fault	Semikron SKM 111 AR MOSFET [6]	100V nominal, 200A nominal (600A max)
3	Current limiting	Resistors	2.2Ω
4	Emulate power converter interface capacitor	BHC Components ALS30A103KE 100 capacitor	10mF, Charged to 16-17V ($v_C(t)$).
5	$i_a(t)$ Current measurement	LEM HAS 200S [7]	50A/V measurement ratio
6	Introduce fault path	Semikron SKM 111 AR MOSFET [6]	100V and 200A nominal (600A max), switching times ≈200ns - 1µs (possible from datasheet)
7	Fault current path	Cable and other in series resistance	4 m of 10mm^2 (≈1.2µH) AWG cable.
8	$i_b(t)$ Current measurement	LEM HAS 200S [7]	50A/V measurement ratio
9	Representative load	Resistors	75Ω
10	A/D conversion, current comparison, protection signaling	NI CRIO-9114 FPGA [8], NI 9223 AI module [9], NI 9401 DO/DI module [10]	1MS/s/channel analogue input, 10MS/s/channel digital output. Control loops set at ≈ 1µs (FPGA can provide ≥300ns possible)

desktop computer deploying top level control software on a dedicated module which then provides real time control of the protection algorithms and fault sequencing of the electrical power equipment.

The following section will illustrate the response of this rig set up and demonstrate how it can be used to test novel protection methods.

Example Rig Response and Protection System Test Results

The experimental set up presented in the previous section was used to replicate a rail to rail short circuit fault occurring between the boundaries of the power converter interface capacitor and the subsequent electrical zone/s. This testing represented a single branch setup (shown in Fig 3) and was utilised to test operational speeds of a fast acting differential protection in DC networks. Further details of this experiment are reported within [5]. Sample results are presented in Fig 4.

The fault response of the experimental setup is shown in Fig. 4 (a) without the implementation operation of any protection system. Within this figure,

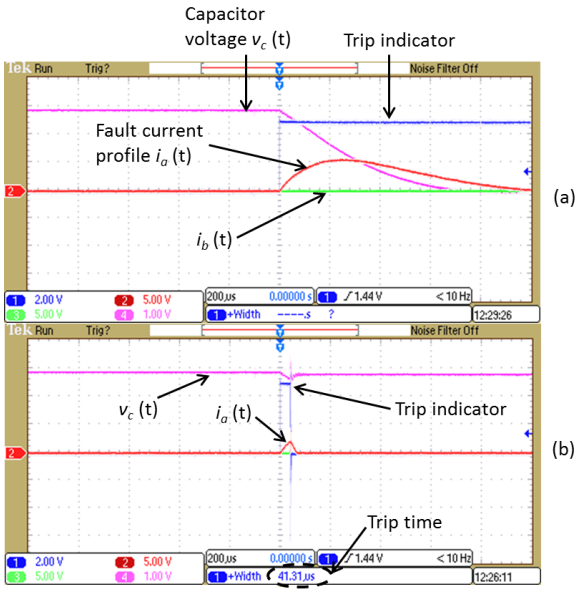

Fig 4. Oscilloscope traces of the fault response of the experimental setup with (a) no protection operation, (b) protection set to a threshold of Δi=90A

i_a *(t)* represents the main fault current component and has a peak of around 280A occurring at approximately 240µs after fault initiation. This shows very similar characteristics to the higher voltage response in Fig 2 as required.

Fig. 4 (b) illustrates the protection system operation for a fixed differential threshold setting of 90A. The figure demonstrates that as i_a *(t)* exceeds this threshold then the protection system quickly issues a trip signal to open the MOSFET switch. This is issued at 41.3µs, with much of this time owed to the development of the current up to the threshold level. These results help validate the protection method under test. Therefore, in conjunction with appropriate circuit breakers (and with the current interruption time being appropriate to avoid high dv/dt), the method is shown to be a viable method of delivering very fast, coordinated protection operation.

Conclusions

This paper has reviewed the potentially significant protection challenges faced in the implementation of DC aircraft power systems, and has discussed the need for novel protection approaches to meet these. The paper then presented a dedicated rig for the maturation of such novel methods, providing key functionality for extensive and realistic testing. The authors are currently extending this rig to incorporate greater complexity in the network architecture, adding dynamic loading to assess protection robustness and incorporating COTS protection equipment for benchmarking purposes. Furthermore, a second rig, operating at higher voltages (270Vdc) is planned to enable higher TRL testing of methods and devices.

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