Full-bridge Modular Multilevel Converter (FB-MMC) with Extended Control Range

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Abstract —This paper presents an attractive control scheme that decouples cell capacitor voltage regulation of the FB-MMC from the dc link voltage regulation. This is achieved by manipulating both ac and dc components of modulation functions. The dc component of modulation function is used to regulate the cell capacitor voltages independent of the dc link voltage, while the magnitude and phase of modulation function ac component are manipulated to control active and reactive powers FB-MMC exchanges with the ac grid. The significance of this control scheme is that it permits the FB-MMC to operate with variable dc link voltage, including negative dc link voltage and zero, while full control over the power FB-MMC exchanges with ac grid is retained. Additionally, this paper provides comprehensive discussion of MMC fundamental theory, including logical and mathematical derivations of the basic relationships that governed its operation and modulation. The validity of the presented control scheme is confirmed using simulations.

Key words—**Half and full-bridge modular multilevel converters; hybrid multilevel converters; high-voltage DC transmission systems; and multi-terminal HVDC networks.**

I. INTRODUCTION

As many countries are expected to adopt large-scale offshore wind farms to reduce their CO_2 and greenhouse gases emission, several voltage source converter high-voltage dc (VSC-HVDC) transmission systems will be built to transmit these powers to the consumption centers. Recent evolution of smart grids and development of multi-terminal HVDC networks may require new types of voltage source converters, which are efficient and resilient to ac and dc network faults. Some of the existing converter topologies with potential to meet some of these requirements are half and full bridge MMCs, and a number of hybrid converters recently proposed [1-19]. Some of the attractive hybrid multilevel converters for multi-terminal HVDC networks that can match the performance of half and full-bridge MMC during dc network faults with minimal impact on the ac side voltage are: mixed cells MMC, alternative arm MMC and hybrid cascaded converters [8, 9, 12, 20-24]. However, mixed cell MMC offers dc fault blocking with lower semiconductor losses than the FB-MMC and inherent all the attributes of FB-MMC [25-31]. This paper exploits the control scheme recently presented in[32] to explore the increased operational possibilities the FB-MMC can offer when used in HVDC links. The significance of this contribution is that it allows cell capacitor voltage regulation to be decoupled from dc link voltage; thus, enables the HVDC link to exchange active and reactive powers independent of dc link voltage. Although will not be demonstrated in this paper, the control scheme Figure 2 can facilitate VSC-HVDC link to be operated with positive and negative dc link as conventional line commutating current source converter HVDC links. This paper uses simulation results obtained from two-terminal symmetrical monopole HVDC link that employs 21-cell FB-MMC to demonstrate the viability of the presented control scheme. The presented simulation results show that the proposed control scheme makes HVDC links that employ FB-MMC to be superior than all other types of VSC systems that can work harmoniously beside LCC-HVDC link in generic dc grid.

II. FUNDAMENTAL THEORY OF MODULAR MULTILEVEL CONVERTER

Figure 1 (c) shows a linear model of the phase leg of the full-bridge modular multilevel converter (FB-MMC) in Figure 1(a). This simplified model is used to illustrate the fundamental theory of the MMC and its control strategy. Using Kirchhoff's current and voltage laws, algebraic and differential equations that describe MMC steady state and internal dynamics in open loop (set $v_g=0$, when MMC is connected to passive load)are:

$$i_o = i_1 - i_2 \qquad (1)$$

$$\tfrac{1}{2}V_{dc} - v_1 - v_o = R_a i_1 + L_a \frac{di_1}{dt} \qquad (2)$$

$$\tfrac{1}{2}V_{dc} - v_2 + v_o = R_a i_2 + L_a \frac{di_2}{dt} \qquad (3)$$

Where i_1 and i_2 are MMC upper and lower arm currents, V_{dc} is the dc link voltage, v_1 and v_2 are the voltages developed across the entire cell capacitors of the upper and lower arms, v_o is the output phase voltage relative to the virtual supply mid-point, and R_a and L_a are the resistance and inductance of the arm reactors.

Subtracting (3) from (2), gives

$$-v_1 + v_2 - 2v_o = R_a(i_1 - i_2) + L_a \frac{d(i_1 - i_2)}{dt} \qquad (4)$$

After combining (1) and (4):

$$-v_1 + v_2 - 2v_o = R_a i_o + L_a \frac{di_o}{dt} \qquad (5)$$

Equation (5) relates output phase current i_o to inverter output voltage v_o and upper and lower arm voltages v_1 and v_2. This equation shows that in order to synthesize a pure sinusoidal ac current i_o at the output phase, the left side of (5) must be a pure sinusoid, this means $-v_1+v_2-2v_o$ must be pure ac of sinusoidal form. Adding equation (2) to (3) yields:

$$V_{dc} - (v_1 + v_2) = R_a(i_1 + i_2) + L_a \frac{d}{dt}(i_1 + i_2) \qquad (6)$$

If the left side of equation (6) is controlled to be pure DC, sum of the upper and lower arm currents $i_1 + i_2$ must be DC, therefore:

$$i_1 + i_2 = i_{dc} \qquad (7)$$

This means equation (6) can be re-arranged as:

$$V_{dc} - (v_1 + v_2) = R_a i_{dc} + L_a \frac{d i_{dc}}{dt} \qquad (8)$$

If $v_1 + v_2$ is controlled to be higher than V_{dc}, power flow will be from the ac side to the dc side; when lower than V_{dc} the power flow is in the opposite direction. Based on these assumptions, if $v_1 + v_2$ is regulated at V_c:

$$v_1 + v_2 = V_c \qquad (9)$$

This equation permits the converter output voltage to be expressed as: $v_o = \frac{1}{2} m V_c \sin \omega t$, whence, re-arranged:

$$-v_1 + v_2 = m V_c \sin \omega t \qquad (10)$$

Where, m is the modulation index.

After solving (9) and (10), the voltages across the upper and lower arms are:

$$v_1 = \frac{1}{2} V_c (1 - m \sin \omega t)$$
$$v_2 = \frac{1}{2} V_c (1 + m \sin \omega t) \qquad (11)$$

Equation (11) provides the mathematical proof of the complementary operation of FB-MMC arms. From (11), modulation waveforms for the upper and lower arms can be resolved into dc and ac components as:

$$m_1 = (1 - m \sin \omega t) = m_d - m_a$$
$$m_2 = (1 + m \sin \omega t) = m_d + m_a \qquad (12)$$

where $m_d = 1$ and $m_a = m \sin \omega t$. Similarly, the upper and lower arm currents of the modular converter are resolved into difference and common mode components as:

$$i_1 = i_{d1} + i_{o1}$$
$$i_2 = i_{d2} + i_{o2} \qquad (13)$$

After substituting (13) into (1):

$$(i_{d1} - i_{d2}) + (i_{o1} - i_{o2}) = i_o \qquad (14)$$

The dc component of equation (14) must vanish in order to synthesize sinusoidal output current i_o: This means $i_{d1} - i_{d2} = 0 \Rightarrow i_{d1} = i_{d2} = i_d$. Similarly, substitute (13) into (7):

$$(i_{d1} + i_{d2}) + (i_{o1} + i_{o2}) = i_{dc} \qquad (15)$$

For the common mode current in (15) to be pure DC current, as assumed, its ac fundamental component $i_{o1} + i_{o2}$ must vanish; therefore $i_{o1} = -i_{o2}$. Substituting $i_{o1} = -i_{o2}$, yields $i_{o1} = \frac{1}{2} i_o$ and $i_{o2} = -\frac{1}{2} i_o$, showing:

$$i_1 = i_{dc} + \frac{1}{2} i_o$$
$$i_2 = i_{dc} - \frac{1}{2} i_o \qquad (16)$$

Equation (16) is the mathematical proof of the current distribution in the modular converter arms, which is universally accepted and widely used in the literature, but without any mathematical proof.

From (8) and (9), i_{dc} can be written as:

$$i_{dc} = K_1 e^{-\frac{R_a}{L_a} t} + \frac{V_{dc} - V_c}{2 R_a} \qquad (17)$$

Substituting (10) into (5):

$$i_o R_a + L_a \frac{d i_o}{dt} = -2 v_o + m V_c \sin \omega t \qquad (18)$$

Assuming the load consists of an inductor L and a reactor R, then:

$$v_o = i_o R + L \frac{d i_o}{dt} \qquad (19)$$

Substituting (19) into (18):

$$2 (R + \tfrac{1}{2} R_a) i_o + 2 (L + \tfrac{1}{2} L_a) \frac{d i_o}{dt} = m V_c \sin \omega t \qquad (20)$$

Considering $R_T = 2 (\tfrac{1}{2} R_a + R)$ and $L_T = 2 (\tfrac{1}{2} L_a + L)$, then (18) can be derived as:

$$i_o R_T + L_T \frac{d i_o}{dt} = m V_c \sin \omega t \qquad (21)$$

From (21), i_o can be written as:

$$i_o = K e^{-R_T t / L_T} + \frac{\tfrac{1}{2} m V_c}{\sqrt{R_T^2 + (\omega L_T)^2}} \sin (\omega t + \varphi) \qquad (22)$$

Where, $\varphi = \tan^{-1} \frac{\omega L_T}{R_T}$.

From equation (22), the steady state load current i_o is determined by V_c, combined resistances and inductances of the load and arm reactors, and modulation index. The decay of the transient component of i_o is determined by the combined time constant $\tau_c = L_T / R_T$.
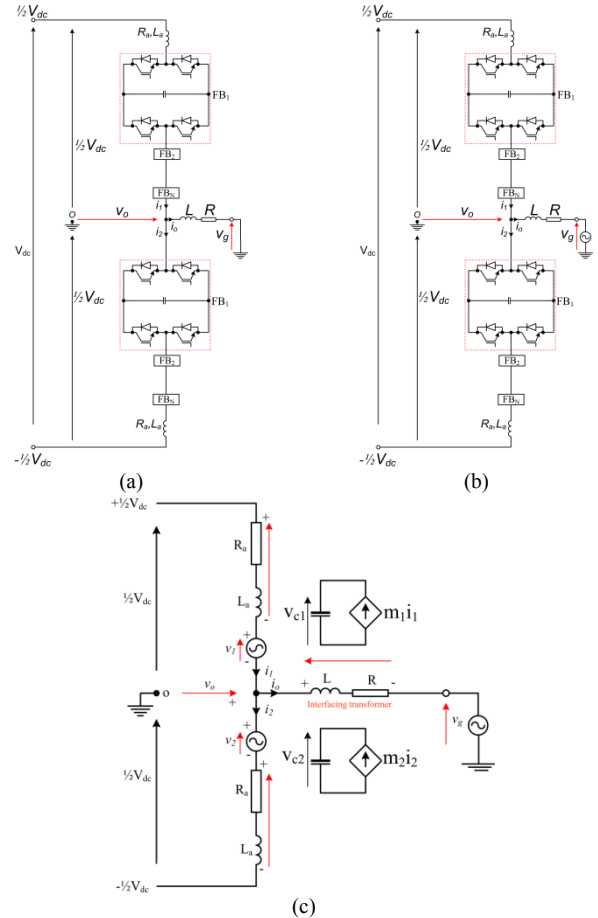

(a)   (b)

(c)

Figure 1: Single-phase of FB-MMC (a) connected to passive load, (b) connected to grid and (c) linear model connected to grid(where m_1 and m_2 are upper and lower arm modulation functions; V_{c1} and V_{c2} are voltage of the equivalent cell capacitors of the upper and lower arms)

III. CONTROL OF FULL-BRIDGE MODULAR MULTILEVEL CONVERTER

FB-MMC in Figure 1 can be controlled using complimentary modulation functions illustrated by equations (11) and (12). However, control scheme in Figure 2 varies both components of the modulations functions m_a and m_d widely to extend control range of FB-MMC beyond that can be achieved with most of the existing control strategies. To operate FB-MMC with positive and negative dc link voltage, m_a and m_d must be allowed to vary over full control range: $-1 \leq m_a \leq 1$ and $-1 \leq m_d \leq 1$. In normal operation, m_d is regulated around 1(buck mode), and in this mode, FB-MMC generates its output voltage (v_o) by inserting cell capacitors of both arms in opposite polarities to that of the dc link voltage (only subtractive states are utilized). However, cell capacitor insertion with the same polarity as the dc link (additive states) is allowed only during the intermediate voltage levels to accelerate cell capacitor voltage balancing. Any reduction in dc link voltage (V_{dc}) will be associated by reduction in m_d,

where $m_d \approx V_{dc}/V_c$ and V_c is the sum of the cell capacitor voltages in each arm. When the dc link voltage is reduced until m_a crosses to negative, the FB-MMC changes its operating mode to boost. In this mode, FB-MMC can insert some of the cell capacitors with the same polarity as that of the dc link voltage (additive states); and the cell capacitors in each arm are used as virtual dc links, provided the sum of the cell capacitor voltages of each arm is maintained around V_{dc}. For practical considerations related to the VSC dc cable insulation, the usable range of m_d is limited to $0 \leq m_d \leq 1$. However, $-1 \leq m_d \leq 0$ represents a new operating region, which is a mirror of that when $0 \leq m_d \leq 1$. In this mode, the MMC can operate normally with the dc link voltage polarity reversed, with voltage stresses across the cell capacitors and switching devices are fully controlled. This mode permits the additive switch states to be used in conjunction with subtractive states at the intermediate voltage levels to accelerate cell capacitor voltage balancing.
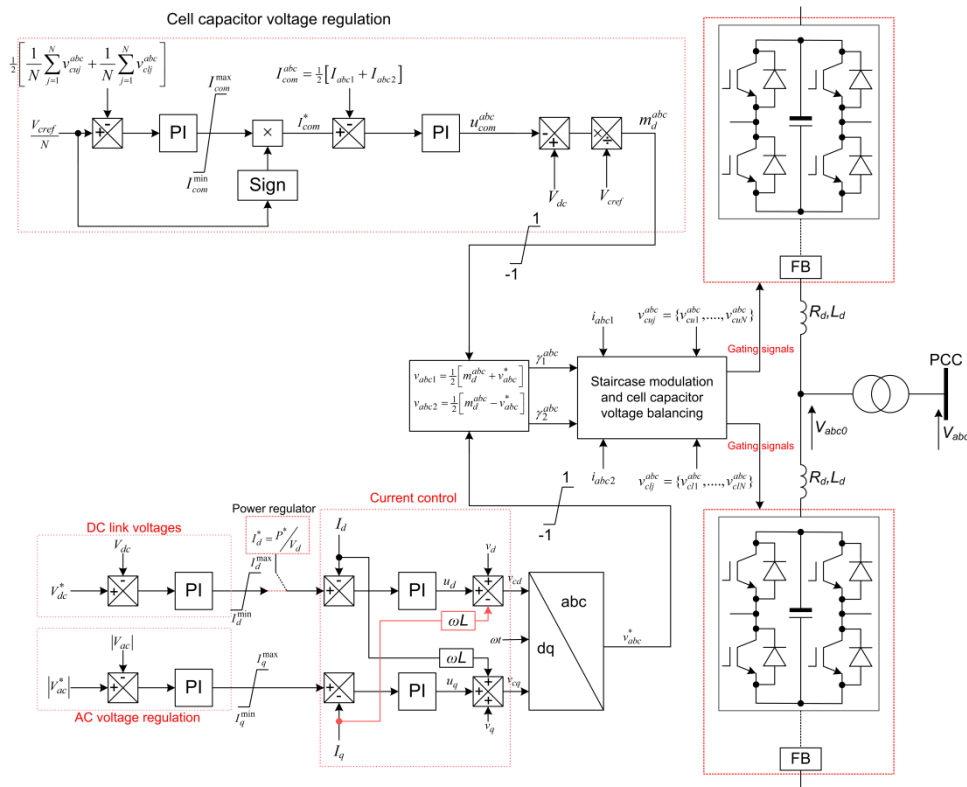

Figure 2: Control diagram for the DC and AC components of the arm voltage references

IV. SIMULATIONS

To demonstrate the extended control range FB-MMC can offer when control scheme in Figure 2 is used, a two-terminal HVDC link that employs FB-MMC with 21 cells per arm is simulated, with parameters listed in Table 1. Converter terminals VSC$_1$ and VSC$_2$ are designated to control active power and dc voltage level respectively; both with unity power factors at their point of common couplings. Initially, VSC$_1$ is commanded to import 800MW from G$_2$ to G$_1$, at $t=0.4s$, it power output is reduced to 400MW and restored to 800MW at $t=2s$. Whilst VSC$_2$ is initially commanded to maintain dc link voltage at 640kV; at $t=0.5s$ its dc link

voltage is reduced to 320kV, and then restored to 640kV at $t=1.6s$. At $t=2.5s$, the cell capacitor voltages of VSC$_2$ are increased by 10% to demonstrate the ability of the presented control scheme in regulating the cell capacitor voltages independent of the dc link voltage. Results obtained from this test are displayed in Figure 3. Observe that the ac currents VSC$_1$ and VSC$_2$ exchange with G$_1$ and G$_2$ and their arm currents in Figure 3 (a) and (b), and (c) and (d) are well regulated, including during period when dc link voltage is reduced by 50% of its rated. Figure 3 (e) and (f) show the dc link current and voltage, both measured at the terminal of the VSC$_2$. Notice that VSC$_2$ is acting as power balancer as the

energy levels of the cell capacitors and dc line distributed capacitors change with the dc link voltage or cell capacitor voltage (draws the deficit from the ac grid or returns the surplus to the ac grid). Figure 3 (g) and (h) show that although the dc voltage is varied from 640kV to 320kV and vice versa, the cell capacitor voltages of VSC_1 and VSC_2 are maintained nearly constant at V_{dc}/N. The plot for the cell capacitor voltages of the VSC_1 displayed in Figure 3 (h) confirms that the presented control strategy permits FB-MMC cell capacitors to be regulated at any arbitrary set-point, provided the sum of the cell capacitor voltages of each arm is greater than the peak of phase line-to-line voltage. Figure 3 (i) and (j) show snapshots of the voltage developed across upper and lower arms of VSC_1, zoomed around transition of dc link voltage from 640kV to 320kV and when the dc link voltage is 320kV. Observe that the dc components of the arm voltages (corresponding to m_d) vary with dc link voltage as previously illustrated. Notice that when dc link voltage is 320kV, the voltages developed across the upper and lower arms cross to negative, and this will trigger the use of additive states as discussed in section III.

Table 1: system parameters

| Parameters	Value
DC link voltage(V_{dc})	±320kV
Converter terminals nominal power	1000MVA
Converter terminals rated active power	950MW
Nominal ac voltage	300kV
Inductance of the arm reactance (L_d)	15mH
Arm reactance plus switching device on-state resistance (R_d)	0.5Ω
Interfacing transformer nominal power	1000MVA
Interfacing transformer voltage ratio	300kV/400kV
Interfacing transformer per unit reactance	0.2pu
AC grid voltage (G_1 and G_2)	400kV
AC grid three-phase short circuit level	20000MVA
X/R	15
DC cable resistance	0.009Ω/km
DC cable inductance	1.1mH/km
DC cable capacitance	0.23μFkm
DC cable length	100km
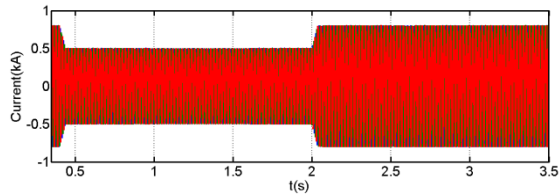
(a)   Current waveforms VSC_1 exchanges with G_1
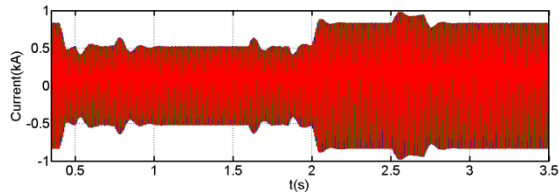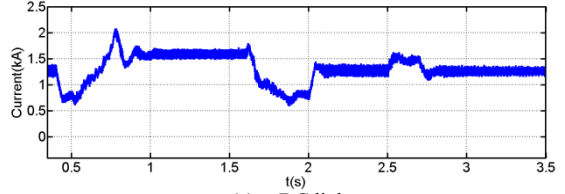

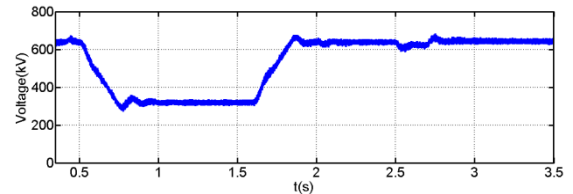(b)   Current waveforms VSC_2 exchanges with G_2
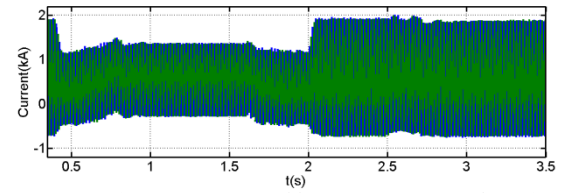
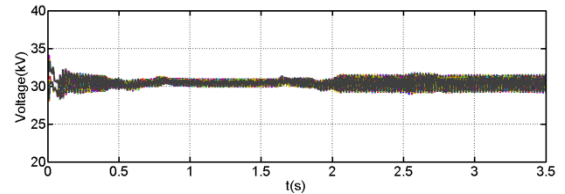(c) VSC_1 upper and lower arm currents (phase a)
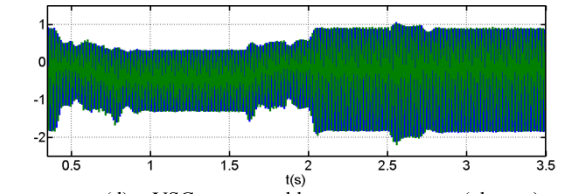
(d) VSC_2 upper and lower arm currents (phase a)
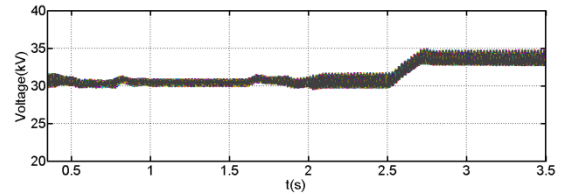
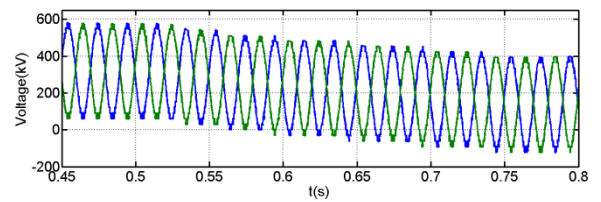

(e)   DC link current
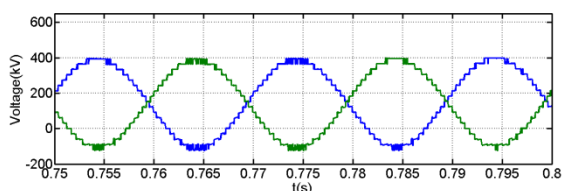

(f) VSC_2 dc link voltage

(g) VSC_1 cell capacitor voltages

(h) VSC_2 cell capacitor voltages

(i)   Snapshot of the voltage waveforms developed across the upper and lower arms of the FB-MMC, zoomed around transition of dc link voltage from 640kV to 320kV

(j) Snapshot of the voltage waveforms developed across the upper and lower arms of the FB-MMC when dc link voltage is 320kV

Figure 3: Selected waveforms that illustrating extended control range of the FB-MMC HVDC link, including decoupling of the cell capacitor voltage regulation from dc link voltage

V. CONCLUSION

This paper presented a control scheme that permits the cell capacitor voltages of the FB-MMC to be regulated independent of physical dc link. This feature allows FB-MMC to exchange active and reactive powers with the ac grid, including when its dc link voltage is lower than the peak of the line-to-line voltage. The validity of the presented control scheme is confirmed using simulations performed on two-terminal HVDC link that employs 21-cell FB-MMC.

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