A single-stage ac-dc buck-boost converter for medium-voltage high-power applications

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Abstract **─**This paper proposes three topologies based on single-stage three-phase ac-dc buck-boost converters suitable for medium-voltage high-power applications. The first two topologies are based on a dual three-phase buck-boost converter, with a three-winding phase-shifted transformer to achieve sinusoidal input currents, with relatively small ac filters. The limitation of these two topologies are the switching devices are exposed either to a high voltage beyond that tolerable by a single device. The third topology is based on three single-phase buck-boost converters; with their dc output terminals connected in series to generate high voltage. By using this approach, voltage stresses on the switching devices are greatly reduced, and sinusoidal input currents with nearly unity power factor is achieved over the entire operating range when using small ac filters. Analysis, PSCAD/EMTDC simulations and experimentation are used to assess the feasibility of the proposed topologies during normal operation. Major findings of this study are discussed and summarised as a comparison between the three topologies.

Key words: ac-dc converters, buck-boost converters, wind energy conversion system and back-to-back converters

I. Introduction

AC-dc converters are used intensively as back-to-back converters in renewable energy systems such as wind and solar; dc-motor drives and dc distributed generation systems (micro-grids); and in power supplies for industrial and domestic electric appliances. Utility recognition of ac-dc conversion power quality problems, especially, harmonic currents injected into ac side, has meant practical measures are taken to improve the power factor and quality of the ac grid currents of these converters. Also, effort is being invested to develop new generations of ac-dc converters that can meet strict power quality regulations and offer the flexibilities needed in renewable power conversion systems[1-5]. Generally, three-phase ac-dc converters can be categorised as follows: buck, boost, and buck-boost converters, and single-stage and two-stage converters. In the majority of the two-stage converters, the first stage is dedicated to power factor correction (PFC) and shaping of the input current, while the second stage is used to regulate the dc output voltage. But this category of ac-dc converters has a number of drawbacks such as: high cost and complex power circuit structures. Therefore, their application is limited.

The following part summarises research on three-phase single-stage ac-dc converters that attempted to reduce the number of active switches and overall cost. For example, the single-switch single-stage buck type converter discussed in [6, 7] is attractive, because it has a simple controller and produces highly quality continuous input currents. Its main drawback is that it operates at a high switching frequency (25 kHz [7]) and exposes the switching devices to high voltage stress due to the high peaks of the discontinuous input capacitor currents. The single-stage buck converter proposed in [8] uses two active switches exposed to half the voltage of that in [6, 7]. However, it requires a switching frequency beyond that appropriate for medium-voltage applications. The three-phase conventional ac-dc boost converter presented in [9-11] has a simple circuit topology and is found in many applications. But the use of a boost converter after the diode stage restricts the scalability of this type of converter (requires a high switching frequency and the need to pre-charge the dc-side capacitor) and it has poor short-circuit protection if an external dc chopper is not incorporated at the dc terminals of the grid side converter. Reference [12] proposed a single-switch boost converter with reduced voltage stress, equal to half the output dc voltage; which is achieved by using a coupled inductor and two buffering capacitors. For higher power rating, a version that uses parallel boost stages is proposed in [13, 14]. The three-phase single-switch ac-dc buck-boost converter proposed in [7, 15, 16] has discontinuous input capacitor current (thus, high-voltage stress per device) and sinusoidal input current. But this approach is not suitable for high-power applications as it uses a high switching frequency of 25 kHz. Reference [17] reintroduces the three-phase buck–boost converter where the input capacitor operates in a continuous current mode and the switching frequency is reduced dramatically to 1.2 kHz to suit medium-voltage applications. However, it requires a sizable ac filter to achieve sinusoidal input current, and exposes the switching devices to high voltage stresses. The authors in [18] presented a new buck-boost ac-dc converter that uses two semiconductor switches, with reduced voltage stress.

In this paper, three single-stage buck-boost converter based topologies suitable for medium-voltage high-power application are proposed. Topology ‘A’ is the dual three-phase buck-boost converter in Fig.1(a), which is an extension of a single-stage three-phase buck-boost converter discussed in [17]. Topology ‘A’ can operate at a relatively low switching frequency such as 1.2kHz. However, it requires sizable ac filters to produce sinusoidal input currents, and its main switching device and the blocking diode are exposed to voltage stress. To overcome this problem, an improved version of topology ‘A’ is proposed as shown in Fig.1(b) (referred to as topology ‘B’), where the total voltage stress is shared evenly between two switching devices S_1 and S_2 and two blocking diodes D_{bd1} and D_{bd2}. Both topologies 'A' and 'B' exploit the harmonic cancelation feature of the three-phase three windings phase-shifted transformer to decrease the size of the ac side C-filter needed to produce high quality input currents. The third topology proposed in this paper is topology 'C', which consists of three single-phase buck-boost converters with dc outputs connected in series as shown in Fig. 2(a). Each sub-converter is rated at ⅓ the total converter rated power and the voltage stress per switch is reduce to the line-to-neutral voltage plus ⅓ the output voltage. Although topology 'C' can operate under continuous or discontinuous dc-link inductance current modes (CCM or DCM), simulation studies show that DCM is better as it reduces the voltage stress on the main switching device and the blocking diode in each sub-converter. This is achieved with higher current stresses in these devices compared to CCM.

The three proposed topologies have the following features: buck and boost capability in a single stage with a minimum switch count, modular structure, simple control system, and sinusoidal supply current with unity power factor.

This paper is organised as follows: Section II describes the operating principle of the proposed dual three-phase ac–dc buck–boost converters (topologies 'A' and 'B'), including their control loop systems and filter design. Section III describes the operating principle of topology 'C', and establishes the basic equations that govern its steady-state operation under CCM and DCM. Its control loops are defined. Section IV uses simulation results from PSCAD/EMTDC to demonstrate the technical feasibility of topologies 'B' and 'C' (under CCM and DCM), including a comparison between topologies 'B' and 'C'. Section V presents experimental results from a 10kW prototype of topology 'C' to verify its steady state and dynamic performance during DCM operation. Conclusions and major findings are highlighted in Section VI.

II. DUAL THREE-PHASE BUCK-BOOST CONVERTER TOPOLOGIES 'A' AND 'B'

a) Circuit description

Fig.1(a) shows a medium-voltage high-power dual three-phase buck-boost converter (topology 'A'), which is an improved version of the single and three-phase buck-boost converters discussed in [17]. It consists of two cascaded three-phase diode bridges and series commutable switch '*S*', see Fig.1(a). Switch 'S' is used to control the output dc voltage by modulating inductor current I_L. Turning on switch '*S*' boosts the energy stored in dc inductor L_{dc}, and this stored energy supplies the load when switch '*S*' is off. The proposed converter uses a three winding transformer, with secondary and tertiary windings are phase shifted 30^o (Δ/Y) from each other to attenuate the 5th and 7th harmonic currents. The ac filters (C_s) connected to transformer secondary and tertiary windings are tuned to remove low-order harmonic currents not eliminated by phase shift transformer, and those associated with the switching frequency components and their sidebands. To simplify the analysis, the rated rms line-to-line voltage of all windings are assumed equal, $v_p=v_{s1}=v_{s2}$; this means the transformer turns ratios are $N_1/N_2=1$ (for the star secondary) and $N_1/N_3=1/\sqrt{3}$ (for the delta secondary). The average output voltage of each bridge rectifier is $-\frac{3\sqrt{3}}{\pi}V_{Cm}$, where V_{cm} is the peak fundamental ac voltage across the filter capacitor C_s. The negative sign reflects the inversion of the bridge output voltage with respect to the load. By using the approach described in [17, 19, 20], the average output dc voltage V_{dc} in CCM is:

$$V_{dc} = 2 \times \frac{\delta}{1-\delta} \times \frac{3\sqrt{3}}{\pi} V_{cm} \tag{1}$$

where δ represents the duty cycle of the switch 'S'. By controlling δ over a wide range $0<\delta<1$, buck ($\delta<½$) and boost ($\delta>½$) operation can be achieved. The major shortcoming of the converter in Fig.1 (a) is that the blocking diode D_{bd} and switch S are exposed to extremity high voltage stresses of $V_{dc}+2V_{Cm}$. This may limit use of the proposed buck-boost converter to the lower end of medium-voltage applications. Topology 'B' is proposed as shown in Fig.1(b), which is an improved version of the converter in Fig.1 (a), where the problem of voltage stresses are partially solved by using two switching devices S_1 and S_2 and two blocking diodes D_{bd1} and D_{bd2} to evenly share the overall voltage stress. This is achieved by splitting the dc inductance L_{dc} into L_{dc1} and L_{dc2} (where $L_{dc1}=L_{dc2}=¼L_{dc}$), and the two dc side capacitors ($C_{dc1}=C_{dc2}$) are connected as Fig.1(b). Although topology 'B' is slightly changed from topology 'A', it still maintains the simplicity and performance of the original circuit, and switches $S_1$and S_2 receive identical gating signals.

b) Filter design and power factor performance

Fig.1(c) shows the equivalent circuit for resonant mode analysis, and filter admittance can written in terms of filter capacitance and transformer inductances as:

$$Y(s) = sC_s + \frac{1}{sL_r + \frac{1}{\frac{1}{sL_s} + \frac{sC_s}{s^2 L_r C_s + 1}}} \tag{2}$$

where L_s is the transformer primary leakage inductance plus the inductance of the supply lines, and L_r is the transformer secondary and tertiary leakage inductances. It is possible to make the leakage inductances of the Y and Δ transformer equal [21]. The parallel resonant frequency can be calculated from the zeros of the $Y(s)$ admittance:

$$\omega_1 = \frac{1}{\sqrt{L_r C_s}} \tag{3}$$

$$\omega_2 = \frac{1}{\sqrt{(2L_s + L_r)C_s}} \quad (4)$$

The transformer is used to cancel the 5th, 7th, 17th, and 19th harmonic currents [22-24], and ω_1 depends on the transformer secondary leakage inductance. Since the transformer leakage inductances are known, the value of the ac-side C-filter is selected such that the cut-off frequency is placed at nine times the base frequency, $9\omega_B$. With the ac filter designed on this basis, simulation studies show that acceptable supply current THD is achieved over the full control range.

c) Control strategy

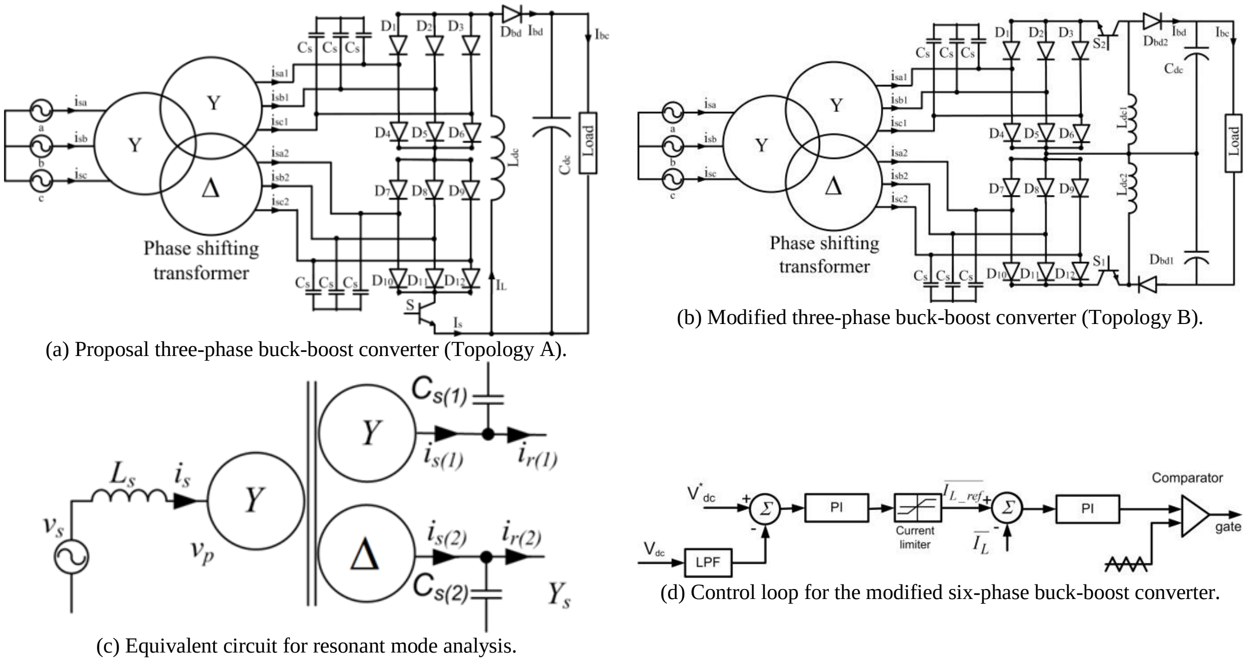
Fig.1*(d)* summarises the control scheme used to control the dual three-phase buck-boost converters in Fig.1(a) and (b). The control system in Fig.1(d) consists of an outer voltage loop that controls the converter total output dc voltage (V_{dc}) and sets reference inductor current (I_L^*); and an inner current loop that forces the dc inductor current I_L to follow its reference, and generates duty cycle δ for the switch S or (S_1 and S_2). The output of the second proportional-integral (PI) controller is compared with a triangular carrier wave to generate the gating signal with fixed pulse width for given operating point to control the buck-boost converter switch (S) or switches ($S_1$and S_2). Operation of switch S with fixed pulse width allows the converter output dc voltage to be controlled, but does not improve the harmonic attenuate of the input ac currents due to discontinuity of the input currents caused by the 120^o conduction pattern of the diode rectifier bridges [17].

III. THREE-PHASE BUCK-BOOST CONVERTER TOPOLOGY 'C'

a) Circuit description

To further reduce the voltage stresses on the semiconductor devices, the three-phase buck-boost converter proposed in Fig. 2 (a) is proposed, Topology 'C' which uses each single-phase diode bridge in series with a switch. The ac terminals of the diode bridge of each phase are connected to three single-phase transformers with isolated secondary windings, while the primary sides can be connected star or delta; however, star connection is shown in Fig. 2 (a). The co-existence of each diode bridge in series with an active switch allows the proposed converter to regulate its dc output voltage in buck and boost mode, with reduced voltage stress per active switch (S_1, S_2 and S_3) and blocking diode (D_{bd1}, D_{bd2} and D_{bd3}): reduced to the line-to-neutral voltage plus ⅓ the output voltage. The proposed converter in Fig. 2 (a) can be operated in CCM or DCM. Its operation modes and control strategy in CCM are the same as discussed in [19] for a single-phase version. The output dc voltage for the three-phase buck-boost converter in Fig. 2 (a) is:

$$V_{dc} = 3 \times \frac{\delta}{1-\delta} \times \frac{2V_m}{\pi} \tag{5}$$



(a) Proposal three-phase buck-boost converter (Topology A).

(b) Modified three-phase buck-boost converter (Topology B).

(c) Equivalent circuit for resonant mode analysis.

(d) Control loop for the modified six-phase buck-boost converter.

Fig.1: Three-phase dual buck-boost converters and their control systems.

b) DCM analysis

For simplicity, the analysis of the proposed converter during DCM operation is carried out on per phase basis, and then extended to the three-phase version. Per phase analysis of the output dc voltage of a single-phase full-bridge diode is adopted.

Assume the switching and supply fundamental frequencies are f_s and f, during the analysis of each switch period the supply voltage is assumed fixed, and the voltage drop in the series elements of input L-C filter is assumed to be sufficiently small to be neglectable. Fig. 2(c) shows that the ac-dc buck-boost converter being studied has three operating intervals in DCM:

First interval ($0<t<t_{on}$): This mode represents the situation when the switch S is on and the dc-link inductor L_{dc} is being energised from the supply, and dc-side capacitor supplies the load with near constant current if its capacitance is sufficiently large. In this interval, the dc-link inductor voltage and current, and dc capacitor current are:

$$v_L(t) = \left|v_s(t_s)\right| = \left|V_m \sin \omega t_s\right| \tag{6}$$

$$\frac{di_L(t)}{dt} = \frac{\left|V_m \sin \omega t_s\right|}{L_{dc}} \tag{7}$$

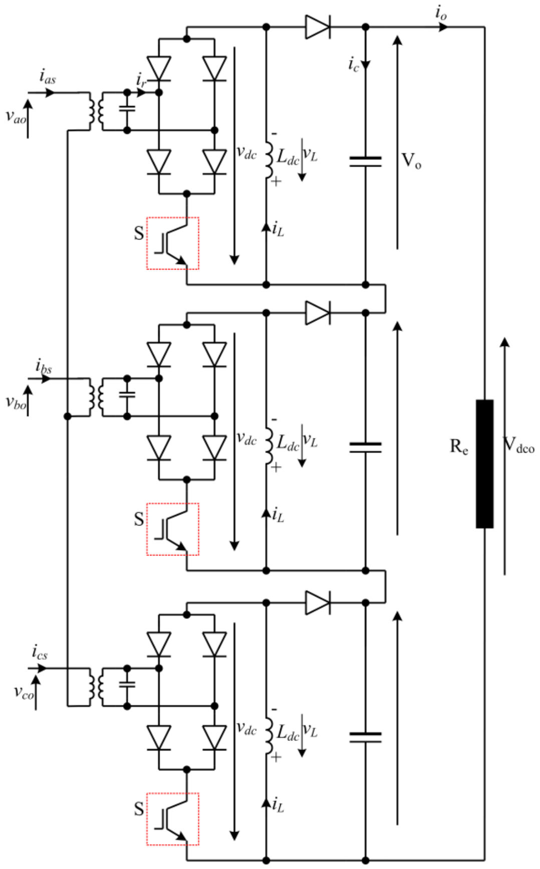
$$i_c(t) = -\frac{V_o}{R} \tag{8}$$

After solving these equations, $i_L(t)$ in this interval is:

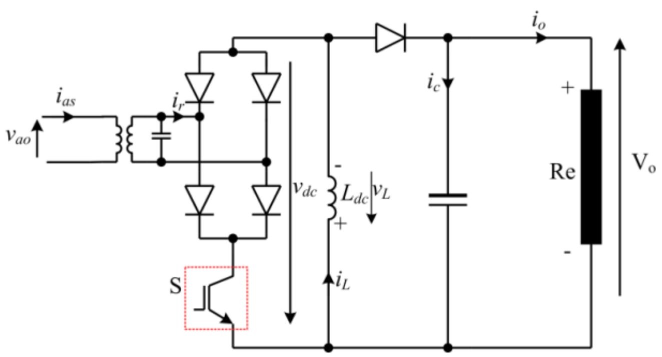
$$i_L(t) = \frac{|V_m \sin \omega t_s|}{L_{dc}} t \tag{9}$$

With switching frequency f_s selected to be much higher than supply frequency f, equation 10 can be used to approximate the peak inductor current (I_{Lmax}) at the instant when the switch S is turned off (at $t = t_{on} = \delta T_s$).

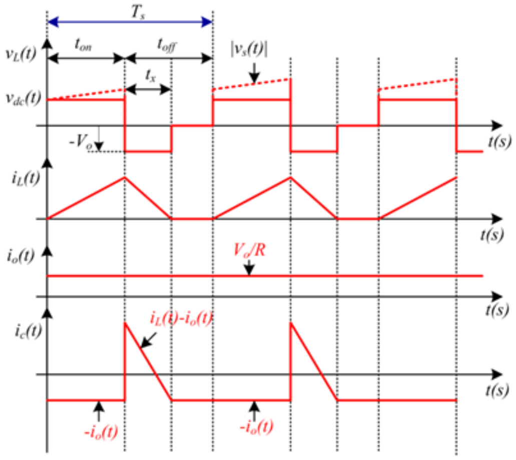
$$I_{L\max} = \frac{|V_m \sin \omega t_s|}{L_{dc}} \delta T_s \tag{10}$$



(a) Proposed three-phase buck-boost converter (topology C).



(b) Single-phase version of the proposed buck-boost ac-dc converter



(c) Waveforms: voltage across dc-side inductor v_L, inductor current i_L, output current i_o and dc-side capacitor current over two and half switching cycles (for one phase Fig. 2 (b)).

Fig. 2: Proposed three-phase ac-dc buck-boost converter.

Second interval ($t_{on} < t < t_x$): This is the period when switch S is off and the dc-link inductor supplies the load and charges the dc-side capacitor, and the voltage impressed across L_{dc} is equal to the load voltage but with negative polarity as shown in Fig. 2 (c). Thus, the dc-link inductor voltage and current, and dc capacitor current are:

$$v_L(t) = -V_o \tag{11}$$

$$\frac{di_L(t)}{dt} = -\frac{V_o}{L_{dc}} \Rightarrow i_L(t) = -\frac{V_o}{L_{dc}}(t - t_{on}) + I_{L\max} = -\frac{V_o}{L_{dc}}(t - \delta T_s) + \frac{\left|V_m \sin \omega t_s\right|}{L_{dc}}\delta T_s \tag{12}$$

$$i_c(t) = i_L(t) - i_o(t) = -\frac{V_o}{L_{dc}}(t - \delta T_s) + \frac{\left|V_m \sin \omega t_s\right|}{L_{dc}}\delta T_s - \frac{V_o}{R} \tag{13}$$

From Fig. 2 (c),$i_L(t_{on}+t_x)=0$ when the energy stored in the dc link inductor L_{dc} is exhausted; thus, t_x is:

$$t_x = \frac{\left|V_m \sin(\omega t_s)\right|}{V_o}\delta T_s \tag{14}$$

Alternatively, this equation can be obtained by setting the average dc link inductor voltage to zero.

Third interval ($t_{on}+t_x< t \leq T_s$): This interval represents the period when the energy stored in the dc link inductor L_{dc} is fully exhausted when its current drops to zero at $t=t_{on}+t_x$ before the next switching period and remains at zero. In this interval, inductor current and voltage are $i_L(t)=0$ and $v_L(t)=0$, and the dc link capacitor current is:

$$i_c(t) = -i_o = -\frac{V_o}{R} \tag{15}$$

Considering the three intervals, the average capacitor current during one switching cycle is:

$$\overline{i_c} = \frac{1}{T_s}\left[\int_0^{t_{on}} i_c(t)dt + \int_{t_{on}}^{t_{on}+t_x} i_c(t)dt + \int_{t_{on}+t_x}^{T_s} i_c(t)dt\right] =$$

$$-\frac{V_o}{R} - \frac{½V_o t_x^2 + V_o t_{on} t_x - V_o \delta T_s t_x - |V_m \sin \omega t_s| \delta T_s t_x}{L_{dc} T_s} \tag{16}$$

Since the input current and output dc voltage of a single-phase full-bridge diode rectifier have half wave symmetry ($0<\omega t<\pi$), the average capacitor current during one half of the supply cycle is:

$$\overline{i_{C\_HC}} = \frac{1}{\pi}\int_0^{\pi}\left(-\frac{V_o}{R} - \frac{1}{L_{dc}T_s}\left[½V_o t_x^2 + V_o t_{on} t_x - V_o \delta T_s t_x - |V_m \sin \omega t_s| \delta T_s t_s\right]\right) d\omega t_s \tag{17}$$

$$\overline{i}_{c\_HC} = \frac{T_s V_m^2 \delta^2}{4 L_{dc} V_o} - \frac{V_o}{R} \tag{18}$$

The steady state average capacitor current tends to zero; the converter voltage gain can be calculated as:

$$V_0 = \frac{1}{2}\delta V m \sqrt{\frac{T_s R}{L_{dc}}} \tag{19}$$

For a given dc link inductance L_{dc}, the critical duty cycle δ_c that defines the boundary between CCM and DCM can be obtained by setting $t_x=T_{off}=(1-\delta_c)T_s$ and $|V_m sin\omega t_s|=V_m$. From equations (14) and (19) δ_c is:

$$\delta_c = 1 - 2 \Big/ \sqrt{\frac{T_s R}{L_{dc}}} \tag{20}$$

In each switching period during DCM operation, the equivalent continuous current in the switch S and pre-filter input current are:

$$i_S(t) = \left\{ \frac{1}{2L} \delta^2 T_s V_m \sin \omega t, \quad 0 \le \omega t \le \pi \right. \tag{21}$$

$$i_r(t) = \left\{ \frac{1}{2L} \delta^2 T_s V_m \sin \omega t, \quad 0 \le \omega t \le 2\pi \right. \tag{22}$$

Equation (21) represent the equivalent continuous current in switch S, and (22) represents the fundamental component of the pre-filter input current, which is sinusoidal and in-phase with the supply voltage. Since the switched version of the input current $i_{sr}(t)$ is contained within the envelope of the supply voltage, $i_{sr}(t)$ only contains switching frequency harmonic components and their sidebands. This feature makes the ac-side L-C filter size smaller and simpler in design than that of the dual three-phase buck-boost converter discussed. These observations indicate that with a small ac filter and fixed duty cycle, the input current of the three-phase buck-boost converter in Fig. 2 (a) can be ensured to be sinusoidal (as there are no low-order harmonics to distort the input current).

The average and root mean square current in the switch S are:

$$\overline{I_S} = \frac{1}{\pi}\int_0^{\pi} \frac{\delta^2 T_s V_b \sin \omega t}{2L_{dc}} d\omega t = \frac{\delta^2 T_s V_m}{\pi L_{dc}} \tag{23}$$

$$I_{S\_rms} = \sqrt{\frac{1}{\pi}\int_0^{\pi} \frac{\delta^4 T_s^2 V_m^2 \sin \omega t}{4L_{dc}^2} d\omega t} = \frac{\delta^2 T_s V_m}{2\sqrt{2} L_{dc}} \tag{24}$$

The average and root mean square current in each diode of the single-phase bridge are:

$$\overline{I_D} = \frac{1}{2\pi}\int_0^{\pi} \frac{\delta^2 T_s V_m \sin \omega t}{2L_{dc}} d\omega t = \frac{\delta^2 T_s V_m}{2\pi L_{dc}} \tag{25}$$

$$I_{D\_rms} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} \frac{\delta^2 T_s^2 V_m^2 \sin \omega t}{4L_{dc}^2} d\omega t} = \frac{\delta^2 T_s V_m}{4L_{dc}} \tag{26}$$

Since the proposed three-phase buck-boost convert consists of three single phase modules, each phase provides ⅓ the output power, and the voltage gain V_{o_3ph} and δ_{cr_3ph} are:

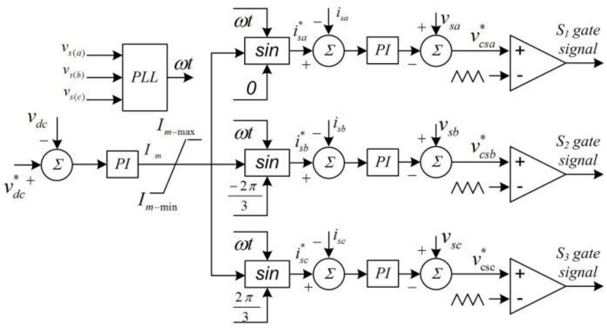
$$V_{0\_3ph} = \frac{3}{2}\delta V m \sqrt{\frac{T_s R}{3L_{dc}}} \tag{27}$$

$$\delta_{cr-3ph} = 1 - 2\sqrt{\frac{T_s R}{3L_{dc}}} \tag{28}$$

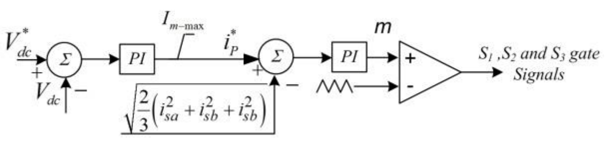
c) Control strategy

Fig. 3(a) shows the proposed controller for the converter in Fig. 2(a) under CCM, where there is one outer control loop and three inner control loops (one per phase). The outer control loop regulates the converter dc output voltage and estimates the peak fundamental current i_m required to maintain the dc link voltage at any desired level. The inner control loops provide reference currents (i_{sa}^* ,i_{sb}^* ,i_{sc}^*) synchronised to the grid voltage, see Fig. 3(a). In addition, to ensuring sinusoidal input currents independent of the load conditions, these inner control loops estimate the fundamental component of the ac side capacitor voltages ($v_{csa}^*, v_{csb}^*, v_{csc}^*$) required to force the input current to follow its control reference (i_{sa}^* ,i_{sb}^* ,i_{sc}^*) and ensure power balance between the ac and dc sides.

Fig. 3(b) summarises the control structure used to control the proposed converter in Fig. 2(a) under DCM operation, which consists of inner and outer control loops. The outer control loop regulates the total output dc voltage V_{dc}, where a PI controller estimates the reference peak fundamental supply current I^*_{p} to achieve any desired dc link voltage V_{dc}, a current limiter is added in the outer control loop to protect the converter from over load. The inner loop forces the peak of the supply current to follow its reference set by the outer loop and estimates the duty cycle δ of switch S.



(a) Proposed controller for CCM operation



(b) Proposed controller for DCM operation .

Fig. 3: Proposed controller for topology ‘C’

IV. SIMULATION RESULTS

This section presents simulation results obtained from PSCAD/EMTDC models of the proposed buck-boost converters topologies. This simulation section consists of four parts. The first part shows the closed loop results of the proposed converter shown in Fig.1(b), while the second and the third parts show the simulation results of the proposed converter shown Fig. 2(a) under CCM and DCM respectively. The converter parameters are listed in Table 1. To highlight the features of the proposed converters, they are simulated under the same operating scenarios. Initially, the dc voltage across a 150Ω load resistance is set to 10kV. At time *t*=0.75s, the load resistance reduced to 100 Ω to test the dynamic response of both converters.

Table 1: Simulation parameters of the three buck-boost converter topologies presented in Fig.1(b) and Fig. 2(a).

Parameter	Topologies 'B'	Topology 'C' CCM	Topology 'C' DCM
Rated power	1MW	1MW	1MW
Supply voltage	3.3 kV L-L	3.3kV L-L	3.3kV L-L
Supply frequency	50Hz	50Hz	50Hz
Switching frequency	1.2kHz	5kHz	2.4kHz
Transformer rated power	5MVA phase shift transformer	Three single-phase transformers 1.7MVA	Three single-phase transformers 1.7MVA
Transformer rated voltage	Primary side 3.3kV / two secondary sides 3.3kV	Three single-phase transformers 1.9/1.9kV	Three single-phase transformers 1.9/1.9kV
Ac-side C-filter	Two 36 μF three-phase bank(0.123MVAr)	Three 5 μF (0.017MVAr)	Three 50 μF (0.17MVAr)
dc-side inductance	Central taped 8mH inductance	Three 3mH	Three 750 μH
dc-side capacitance	Two 2200 μF	Three 2200 μF	Three 2200 μF

a) Buck-boost converter (topology 'B')

The simulation results for topology 'B' are shown in Fig. 5. The transformer primary side inductance plus the supply inductance is 0.15pu, and the secondary leakage inductance is 0.1 pu for each winding. The ac-side C-filter value is selected such that the cut-off frequency is nine times the base frequency ($9\omega_B$), according to equation (3), the capacitance is 0.123pu. Using these filter parameters, the plot for the power factor profile in Fig. 4 is obtained from simulations of topology 'B' when the load is varied from no load to full load. This profile is also valid for topology 'A', independent of buck or boost modes. With this filter design topologies 'A' and 'B' operate at unity power factor from 90% of full load to rated load. The input power factor is higher than 0.95 lead when loading is between 60% to 90% of rated power, see Fig. 5(b).

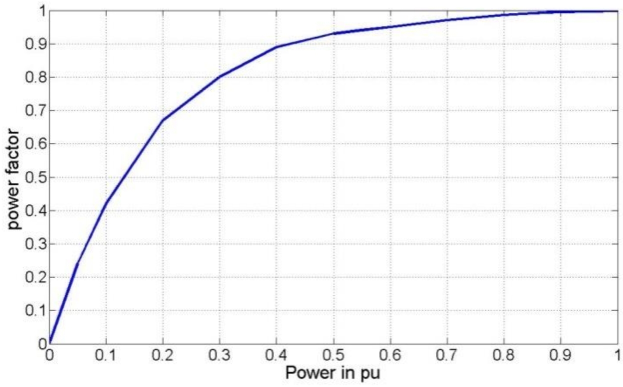
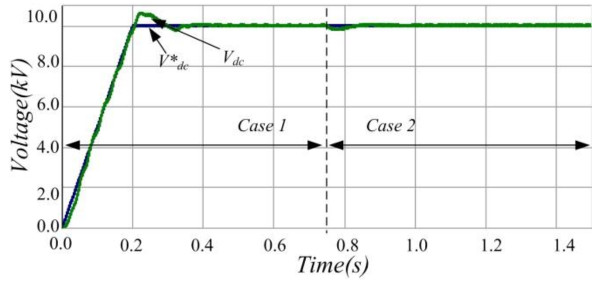


Fig. 4: Power factor profile of topologies ‘A’ and ‘B’

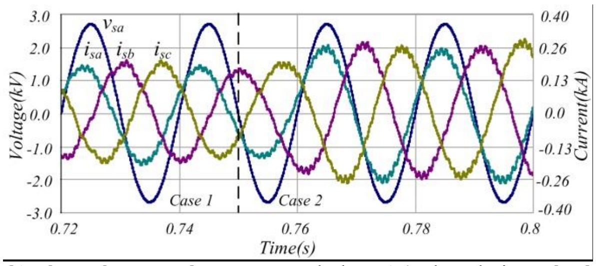
Fig. 5(a) show that the proposal converter is able to track the reference output voltage, with minimum overshoot when the load resistance is halved. Fig. 5(b) shows the three-phase supply currents and phase ‘*a*’ voltage during the step increase in load. From Fig. 5 (b) the proposed converter draws sinusoidal current from the supply, with 0.935 power factor leading in case 1 and unity power factor when the load resistance decreases to 100Ω. The switch S is exposed to a voltage stress of 10kV approximately; see Fig. 5(c). Fig. 5(d) shows the dc-link inductor current where the current increases to compensate the step load change

b) Buck-boost converter (topology ‘C’) in CCM

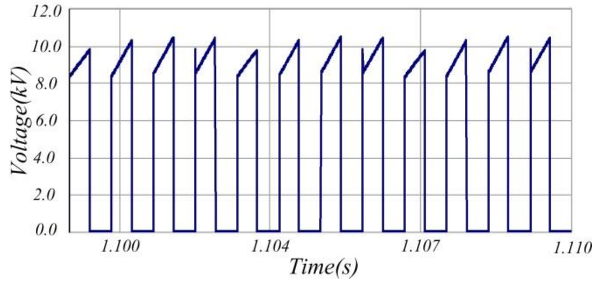
The closed loop results of the converter shown in Fig. 2(a) under CCM conditions are shown in Fig. 6. Fig. 6(a) shows the proposed converter is able to force its dc output voltage to follow the reference voltage in buck and boost modes, including when the load resistance is decreased from 150Ω to 100 Ω. The under-shoot observed in Fig. 6(a) takes longer to be corrected, due to the large dc side inductances needed for CCM. These inductors do not allow rapid dc current change; thus, produce a slowed dynamic performance compared to the DCM case to be presented in the following subsection. Fig. 6(b) shows samples of the three-phase current inputs and phase ‘*a*’ voltage, all zoomed around the instant when the load resistance changes. Fig. 6(c) shows a sample of the voltage stress across the switch S_1. The voltage stress across this switch is comparable to the theoretical value stated in section III, with a magnitude associated with a small ac-side C-filter (discontinuous input capacitor currents). Fig 4(d) shows the dc-side inductor current is continuous as expected and increases when the load resistance is decreased.



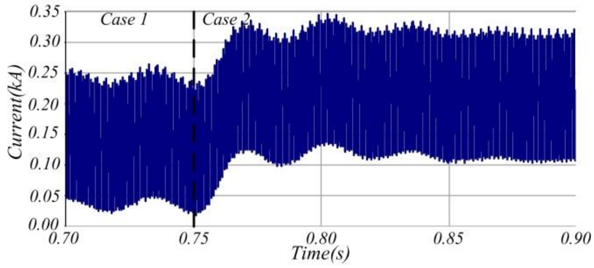
(a) dc-output voltage.



(b) Three-phase supply currents and phase '*a*'voltge during a load increase

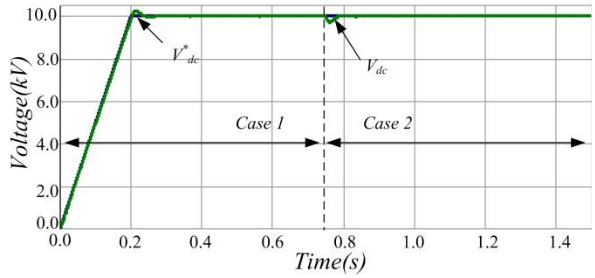


(c) Voltage stress per switch.

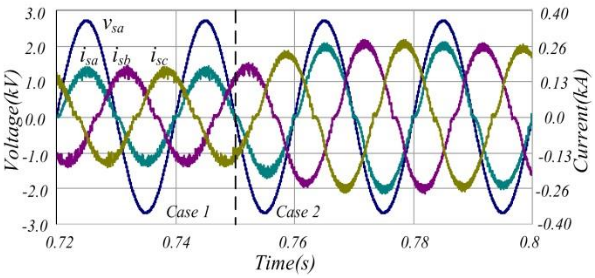


(d) dc-link inductance current.

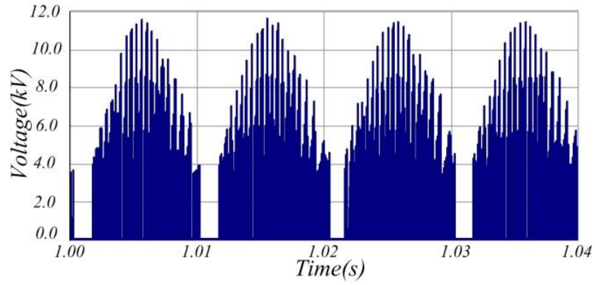
Fig. 5: Simulation results for the proposed six-phase buck-boost converter.



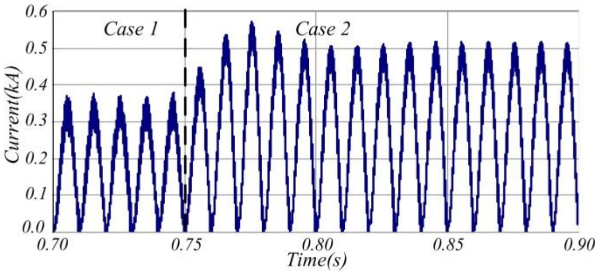
(a) dc ouput voltge



(b) Three-phase supply currents and phase 'a'voltage during the load increase



(c)Voltage stress per switch.



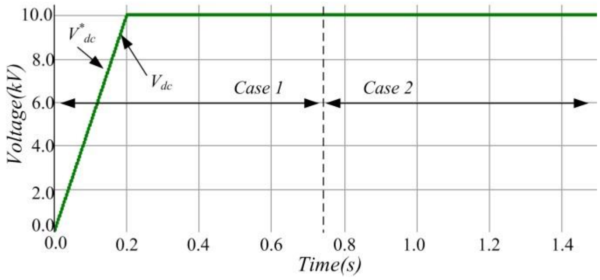
(d) dc-link inductance current operating at CCM

Fig. 6 Simulations illustrate the performance of the proposed three-phase buck-boost converter (topology 'C') under CCM.

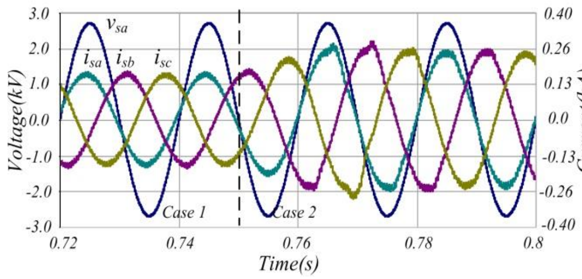
c) Buck-boost converter (topology C) under DCM operating conditions

Fig. 7 shows the closed loop operation waveforms of the three-phase buck-boost converter operating under DCM. Fig. 7(a) shows that the converter is able to track the reference output voltage, including during a step change in load resistance, and this is achieved rapidly and with minimum under-shoot (compared to CCM presented in subsection IVb). From Fig. 7(b) the supply current is sinusoidal and in phase with the supply voltage. Fig. 7(c) shows the voltage stress on switch S_1 is inline with the theoretical prediction stated in section

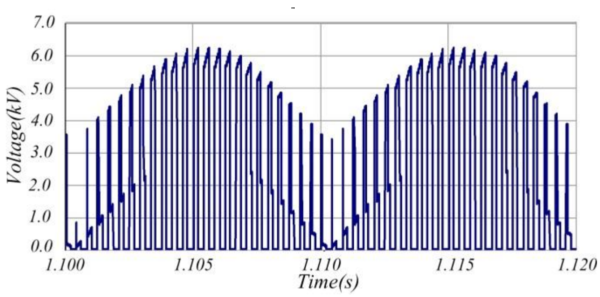
III. Fig. 7(d) shows a zoomed version of the dc-link inductor current, and the converter is seen to operate on boundary between CCM and DCM.



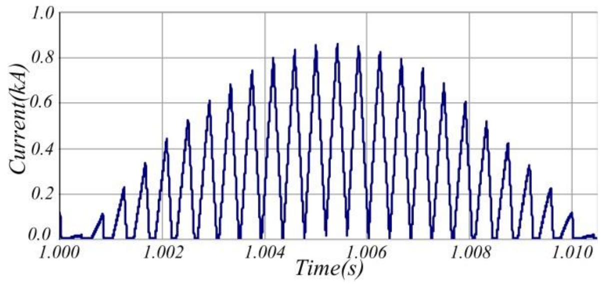
(a) dc output voltage.



(b) Three-phase supply currents and phase '*a*' voltage during the stepped increase in load.



(c) Voltage stress per switch.



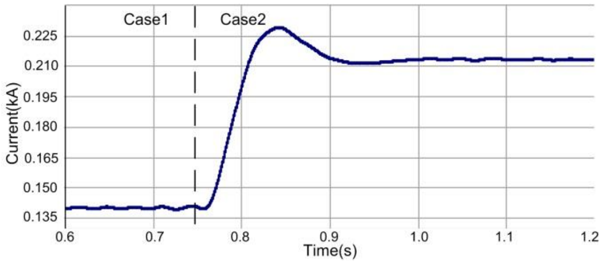
(d) dc-link inductor current.

Fig. 7: Simulation results of the perofrmance of the three-phase buck-boost converter under DCM.

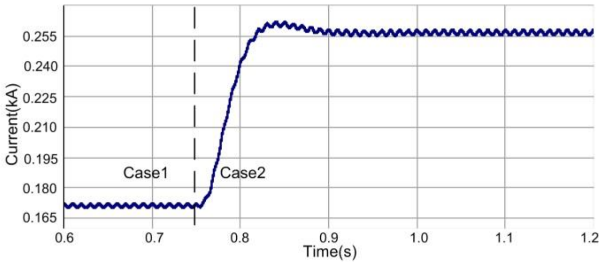
d) Comparison between the proposed buck-boost converters in Fig.1 (a) and Fig. 2 (a)

- The three-phase converter under DCM has a faster dynamic response due to using smaller dc-side inductance and a medium size ac-side C-filter, see Fig. 5(a), Fig. 6(a) and Fig. 7 (a)
- Sinusoidal current with near unity pf is achieved with topology 'C' in both CDM and DCM modes, over a wide range of operating conditions. This is unlike the dual three-phase buck-boost converters in Fig. 1(a) and (b) that ensure nearly unity power factor over a limited range according to a pre-defined profile.
- Topology 'C' under DCM has lower semiconductor voltage stress, but the highest current stress per switch.
- For the same supply voltage and rated output power, the three-phase buck-boost converter (topologies 'A' and 'B') have the lowest average dc-link inductor current as shown in Fig.8. This is because their rectified dc output voltages are higher than that of the three series connected single phase case, by a factor of $\sqrt{\frac{2}{3}}$.

The simulation results in Fig. 5, Fig. 6 and Fig. 7 show that the proposed buck-boost converters provide high-quality sinusoidal input current with stable dc output voltage. This qualifies the proposed converters to operate as an interfacing converter for permanent magnetic wind-turbine generators, and for operation as a front-end converter for grid-connected current and voltage source converters, with black-start and shutdown capabilities. Also the modified dual three-phase buck-boost converter (Topology ‘B’) has the advantage of lower current stress per device, and the three-phase buck-boost converters under DCM (Topology ‘C’) has the advantages of lower voltage stress per switch and lower supply current THD.



(a) Average dc-link inductor current of topology ‘B’.



(b) Average dc-link inductor current of topology ‘C’

Fig.8: Average dc-link inductor current.

V. EXPERIMENTAL RESULTS

A 10kW prototype of the proposed three-phase buck-boost converter (topology ‘C’, see Fig. 9) was assessed to establish its steady state and dynamic performance during DCM operation, with system parameters listed in Table 2. To demonstrate the soft start and shut-down capability, the output dc link voltage (V_{dco}) is increased from 0 to 1250V and then reduce to zero within 30s. The results are displayed in Fig. 10. From Fig. 10(a) the proposed converter provides high boost with good dynamic response during soft start up, steady state and shutdown. Fig. 10 (b) shows the steady state output voltage and the voltage stress across switch S, where the voltage stress across the switch is 600V, as expected ($130\sqrt{2}+\frac{1}{3}\times1250\approx600$ V, which is much lower than in topologies A and B). Fig. 10(c) shows that the supply current is sinusoidal with nearly unity power factor (this is achieved without any dedicated control to force unity power factor operation). The dc-side inductor current (i_L) in Fig. 10(d) confirms DCM operation of the proposed buck-boost converter.

Table 2 Experimental setup parameters.

Parameter	Value
Supply voltage	$260V_{L\_N}$
Transformer rated power	8kVA
Transformer rated voltage	$440/220V_{L-L}$
ac-side capacitance	80 µF
dc-side inductance	330 µH
dc-side capacitance	2200 µF

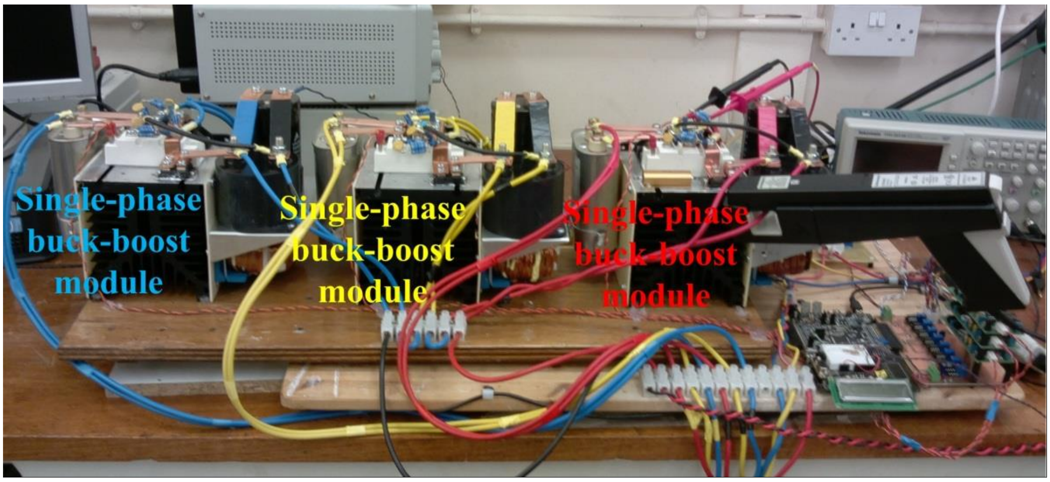
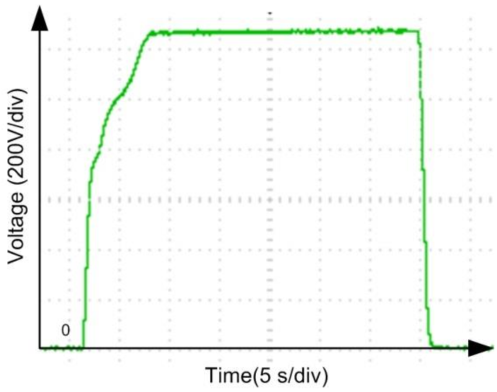
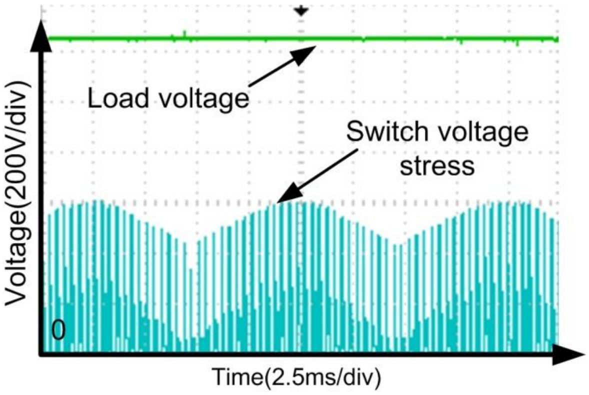


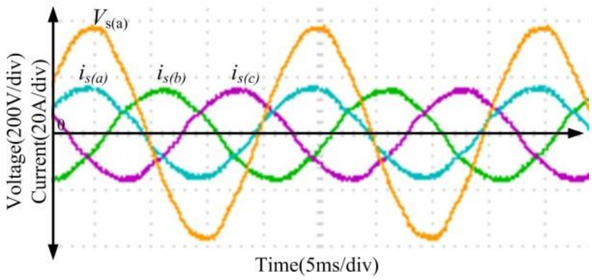
Fig. 9: Experimental test rig.



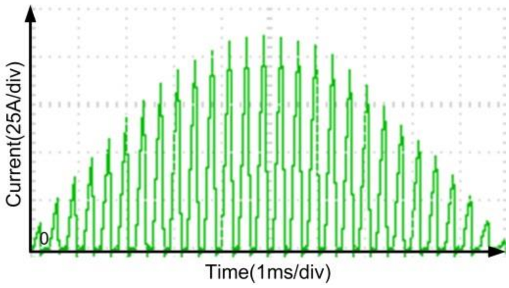
(a) Output voltage.



(b) Load output voltage and switch voltage stress on switch S_1.



(c) Three-phase supply currents and phase '*a*' voltge at steady state.



(d) dc-link inductor current.

Fig. 10: Waveforms showing the overall performance of the proposed three-phase buck-boost converter.

VI. Conclusion

In this paper, three single-stage three-phase ac-dc buck-boost converter topologies suitable for high-power medium-voltage applications were proposed. The ac side filter design for topologies 'A' and 'B' ensures high power factor at rated power, and low input current THD. They expose some of the switching devices to excessive voltage stress. The simulation and experiments conducted on topology 'C' under DCM showed that it can operate both in buck and boost modes, likes topologies 'A' and 'B', but with reduced voltage stress on the blocking diodes and switch S. Also, it has better harmonic performance and input power factor profile, from no-load to full-load conditions, than topologies ‘A’ and ‘B’. But the switching devices are exposure to higher current stresses. The theory, simulations, and experimental results presented establish that the proposed ac-dc buck-boost converters are viable for medium-voltage, high-power, ac-dc conversion applications, including grid interfacing of wind energy systems.

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