MOSFET Parallel-Connection of Low-Voltage MMC for LVDC Distribution Networks

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Abstract

A highly efficient DC-AC converter is key to the success of low-voltage DC (LVDC) distribution networks. Calculated power losses in a conventional IGBT 2-level converter, a SiC MOSFET 2-level converter, a Si MOSFET modular multilevel converter (MMC) and a GaN HEMT MMC are compared. Calculations suggest that the parallel-connected Si MOSFET MMC may be the most efficient topology for this LVDC application. In this paper, the current unbalance limits for the parallel-connected MOSFETs and the optimal number of parallel-connected MOSFETs for MMC are investigated. Experimental results are presented for current sharing in parallel-connected MOSFETs and for the verification of power loss in a single Si MMC module.

1 Introduction

230/400V AC distribution networks today face the challenges of both increasing load demands and the connection of new technologies such as embedded generation and E.V. charging. Studies show that LVDC distribution technologies are able to provide large power capacities without reactive and harmonic power flows [1-3]. Moreover, rapidly increasing distributed generation such as photovoltaics and wind turbines are intrinsically DC. LVDC networks could remove many conversion stages when connecting to household and office DC loads such as TVs, PCs and printers, as well as variable frequency AC loads such as washing machines, air conditioners and refrigerators [4-6].

Defined by the EU low voltage directive (LVD 72/23/EEC), the range of low voltage rating is between 75 and 1500V [7]. Therefore, ±750V is chosen to be the DC bus voltage for the Finnish LVDC test network to gain the highest power capacity for the same thermal limit [8, 9]. In this paper, input DC voltage is chosen as 600V (±300V) to conform with the thermal and isolation limits of the existing cables. Lack of information on existing cable reliability above current LVAC peak voltages (340V), as well as the convenience of 600VDC for power device selection, suggest that 600V is a good choice for an LVDC network.

However, there are still large numbers of AC loads, requiring DC-AC power conversion to be highly efficient whilst meeting user power quality requirements. In this paper, the low-voltage Modular Multilevel Converter (MMC) is proposed for this application, giving good waveform quality and high efficiency [10]. The modular structure of MMC reduces slew-rate and stress on each switch, hence reducing total harmonic distortion (THD). Energy is distributed and stored in each submodule capacitor, so that DC current can be controlled without an input filter [11, 12]. MMC also enjoy low switching frequency and smaller AC filters. However, MMC capacitor volume can be greater than that for an equivalent 2-level converter.

Emerging wide-bandgap devices such as the SiC MOSFET and GaN high electron mobility transistors (HEMT) are suitable for LVDC distribution networks. Therefore, in this paper, a Si MOSFET MMC, a SiC MOSFET converter and a GaN HEMT MMC will be compared. Since MOSFETs are simple to parallel-connect due to their positive temperature coefficient, parallel-connection of these three types of converter will be analysed and the optimal number of the devices chosen in Section 3. Static and dynamic current sharing experimental results will be presented in Section 4.

2 Outline Modelling - Power Loss Calculations

To choose the optimal converter topology for an LVDC network, power loss calculation is important. In this section, calculations for semiconductor conduction and switching losses, capacitor losses and inductor losses are introduced.

The modular structure of the MMC enables the converter to use low on-state resistance (R_{on}) MOSFETs and GaN devices instead of IGBTs, thus lowering conduction loss. Parallel-connected switches lead to a further reduction of conduction losses. Submodule switching frequency is approximately $1/N$ times the overall converter switching frequency, where N is the number of submodules in one converter arm [13].

2.1 Conduction Loss

Conduction loss is caused by the on-state voltage drop across switching devices. The conduction loss for MOSFETs and GaN transistors is given by (1)

$$P_{con} = \frac{1}{T}\int_0^T \left(i_{DS}(t)\right)^2 \cdot R_{on} dt \qquad (1)$$

where i_{DS} is the drain-source current and R_{on} is the on-state resistance.

Due to the positive temperature coefficient, R_{on} increases with junction temperature T_j as given in (2) [14]

$$R_{on} = R_{on\_25} + k_{Ron} \cdot (T_j - 25) \quad (2)$$

where R_{on-25} is the on-state resistance when the junction temperature is 25°C and k_{Ron} is the temperature coefficient obtained from the datasheet.

During synchronous rectification, diodes only conduct during dead time [10, 15] and diode conduction loss is neglected.

2.2 Switching Loss

SiC MOSFET switching loss can be estimated by the product of switching energy and switching frequency f_S. Assuming a linear relationship between the switching energy and drain current, curve fitting can be applied to obtain the switching energy loss. SiC MOSFET switching power loss is therefore given by (3).

$$P_{SW\_SiC} = (E_{on} + E_{off}) \cdot f_s = \frac{1}{T}\int_0^T \left[(K_{on\_0} + K_{off\_0}) + (K_{on} + K_{off}) \cdot i_{DS}(t)\right] \cdot f_s dt \quad (3)$$

where K_{on-0} and K_{off-0} are offsets, and K_{on} and K_{off} are gradients, obtained from curve fitting to E_{on} and E_{off} respectively.

Switching loss for lower voltage rating Si MOSFETs and GaN transistors is relatively small and is given by (4) [16, 17]

$$P_{SW} = \frac{1}{2} I_{DS} V_{DS} (t_{off} + t_{on}) f_s \quad (4)$$

where t_{on} and t_{off} are the turn-on and turn-off times respectively, and are obtained from the division of switching gate charge Q_{SW} by the average gate current I_{GS} [18].

$$t_{on} = t_{off} = \frac{Q_{SW}}{I_{GS}} = \frac{(Q_{gs} - Q_{g(th)}) + Q_{gd}}{I_{GS}} \quad (5)$$

I_{GS} can be approximated by the Miller plateau gate current

$$I_{GS} = \frac{V_{GS} - V_P}{R_g} \quad (6)$$

where V_P is the Miller plateau voltage, and R_g represents the total gate resistance.

Diode switching loss is mainly caused by reverse recovery behaviour, therefore reverse recovery charge *Qrr* is used to calculate the diode switching loss.

$$P_{rr\_D} = Q_{rr} \cdot V_D \cdot f_s \quad (7)$$

2.3 Capacitor Loss

Capacitors in MMC are distributed in each submodule, and are key to the generation of the AC output voltage. Input DC capacitors are also required by conventional 2-level converters to limit the voltage ripple. Network operators allow a maximum ±10% fluctuation [19]. Capacitances can be sized accordingly by calculating the peak to peak energy deviation [20].

The equivalent series resistance (ESR) of a capacitor can be used to estimate the dissipated power [21]. Capacitor power loss is given by (8)

$$P_{cap} = {I_{cap}}^2 \cdot R_{ESR} \quad (8)$$

where I_{cap} is the average capacitor charging current, and R_{ESR} is the equivalent series resistance of the submodule capacitor.

Electrolytic capacitors are used in this study due to their smaller volume. If volume is not critical, DC film capacitors can be used, thereby almost eliminating capacitor power loss.

2.4 Inductor Loss

The existence of arm inductors is one of the major features of MMC, as shown in Figure 1. The arm inductors can suppress the circulating current and limit the fault current [22]. By meeting the requirement of limiting the circulating current ripple to 5% of the DC side current, arm inductance can be sized accordingly [22, 23]. It is assumed that the value of inductance in each arm is similar to the required output filter inductance for 2-level converters. Because the AC component of the MMC arm current (i_{a1} in Figure 1) is half of the output AC current, the inductors core and AC winding losses can therefore be assumed to be the same.

$$i_{a1} = i_d + \frac{i_{ao}}{2} \quad (9)$$

where i_d is the circulating current and i_{ao} is the AC output current.

The only difference in the inductor power loss between MMC and the 2-level converter considered is caused by i_d. The inductor DC resistance loss is given by (10)

$$P_{Larm} = {I_d}^2 \cdot R_{DC} \quad (10)$$

where I_d is the RMS value of the circulating current and R_{DC} is the DC resistance of the inductor winding.

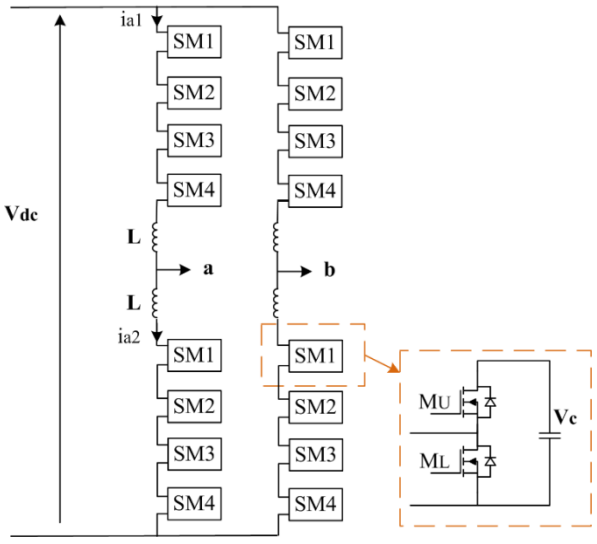


Figure 1 Topology of a Si MOSFET 5-level MMC

3 Converter Comparison

In this section three types of converters are compared. The total power for each converter in this study is set as 10kW based on anticipated power demand per household, and switching frequency is assumed to be 10kHz.

3.1 Si MOSFET 5-level MMC

Based on the loss calculation methods of Section 2, losses in a conventional 2-level IGBT converter and Si MOSFET MMC with different numbers of levels are illustrated in Figure 2. It shows that with increasing number of levels, capacitor and inductor power losses are constant, that conduction and switching losses decrease gradually, and that parallel-connection (Figure 3) of 2 MOSFETs dramatically reduces conduction loss. Therefore, the practicalities and potential performance improvements of parallel-connected MOSFETs will be explored. Since the complexity of the control circuit increases with the number of levels, a 5-level MMC with parallel-connected Si MOSFET is chosen for this study.

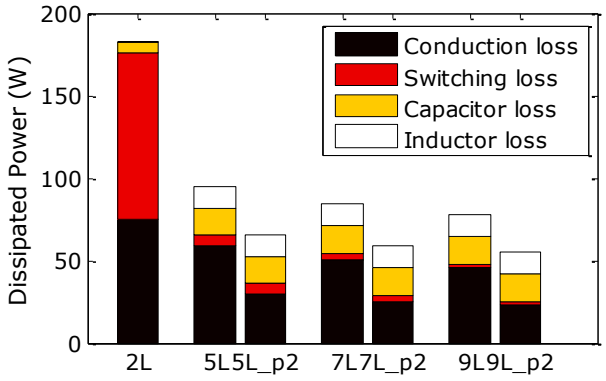


Figure 2 Loss comparison for two-phase-leg 2-level IGBT converter and different levels of Si MOSFET MMC at 10kHz, 10kW. 2L=2 level IGBT; 5L/7L/9L= 5/7/9 level MMC without parallel connection; 5L_p2/7L_p2/9L_p2= 5/7/9 level MMC with 2 parallel-connected devices (Devices used in model are: N=2: IRG7PSH50UD; N=5:IRFP4768; N=7:IRFP4668; N=9:IRFP4568)

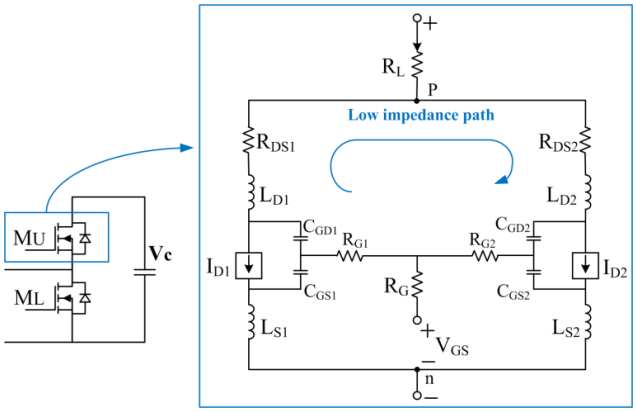


Figure 3 Parallel-connection of 2 MOSFETs in a submodule

3.2 SiC MOSFET 2-level Converter

For the SiC MOSFET, conduction loss does not reduce with increasing numbers of levels due to the lack of low on-state resistance devices available at lower voltage rating. For a 600VDC application, the lowest loss SiC MOSFET converter is 2-level, as shown in Figure 4. The 1.7kV Cree CAS300M17BM2 is used because of its lower on-state resistance compared to 1.2kV SiC MOSFET devices [24].

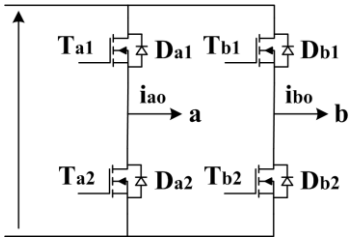


Figure 4 SiC MOSFET-based 2-level converter

3.3 GaN HEMT 3-level MMC

For GaN devices used in a 600VDC application, 3-level and 11-level GaN MMC can be adopted, based on the availability of 650V and 100V devices at this time. Conduction losses dominate any MOSFET MMC so that R_{on} dictates device and topology choice. Compared with the 100V IRFP4110PbF Si MOSFET (R_{on}=3.7mΩ), the 100V GS61008T GaN HEMT (R_{on}=7.4mΩ) yields no benefit. Therefore, a GaN 3-level MMC using GaN Systems GS66516T devices is chosen.

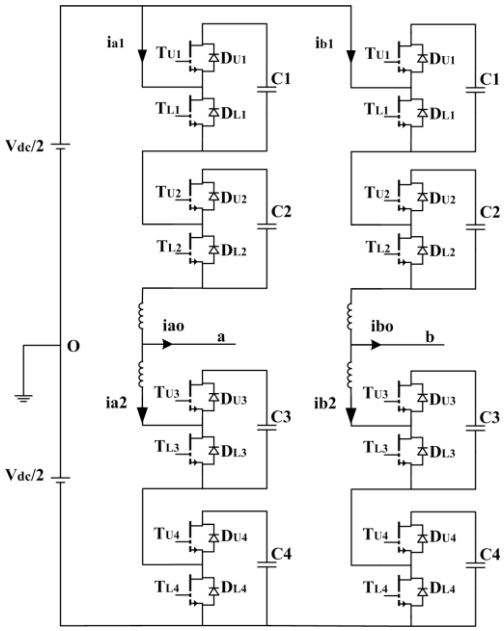


Figure 5 Topology of a GaN 3-level MMC

3.4 Comparison of Technologies using Parallel Connection

In this section, loss will be compared between Si MOSFET 5-level MMC, SiC MOSFET 2-level and GaN 3-level MMC. In these calculations, all the devices are assumed to be identical, hence the expression for R_{on} (2) can be modified by dividing by m, where m is the number of parallel-connected devices, and their current sharing is assumed to be ideal. Parasitic track resistance and solder joints must also be considered, particularly for very low R_{on}.

It is estimated [15] that track resistance consists of two parts: 0.2mΩ (R_{DS}) for each individual device connection to the

drain (p) and source (n) joints in Figure 3, and 0.4mΩ (R_L) from these joints to the bus. Therefore, the new total on-state resistance can be given by (11).

$$R_{on} = 0.4 + \frac{1}{m}\left(R_{on_{25}} + k_{Ron} \cdot \left(T_j - 25\right) + 0.2\right) \text{ m}\Omega \quad (11)$$

Power losses for different numbers of parallel-connected devices in the chosen converters are illustrated in Figure 6. Track resistance is included in the calculation, which explains why power loss reduces less dramatically when the number of parallel-connected devices exceeds approximately 4. From Figure 6, it is concluded that the Si MOSFET 5-level MMC with 4 parallel-connected MOSFETs is the most optimal topology in this study due to its relatively lower power loss.

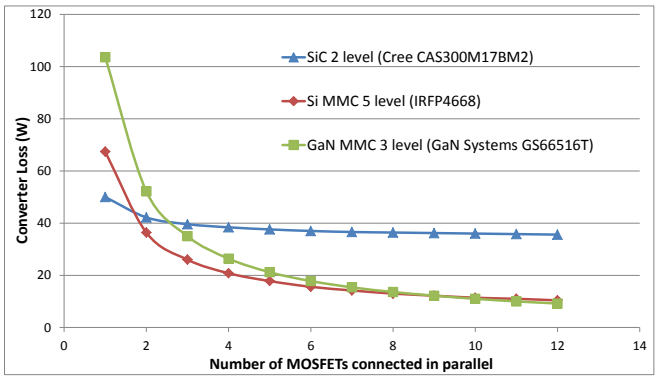


Figure 6 Loss comparison for two phase-leg Si MOSFET 5-level MMC, SiC 2-level, and GaN 3-level MMC converters

4 Experimental Results

In this section, the static and dynamic current sharing in four parallel-connected Si MOSFETs is investigated.

4.1 Circuit Layout

A non-symmetrical layout will give rise to current unbalance during switching transients, resulting in the unbalance of switching losses between devices [25]. Figure 7 shows the symmetrical circuit layout used in this test.

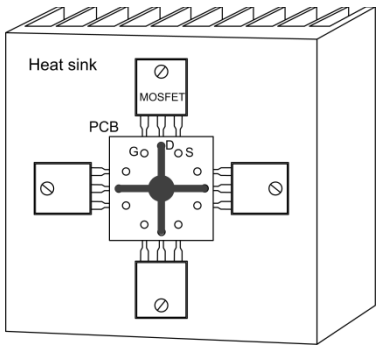


Figure 7 Layout of 4 parallel-connected Si MOSFETs

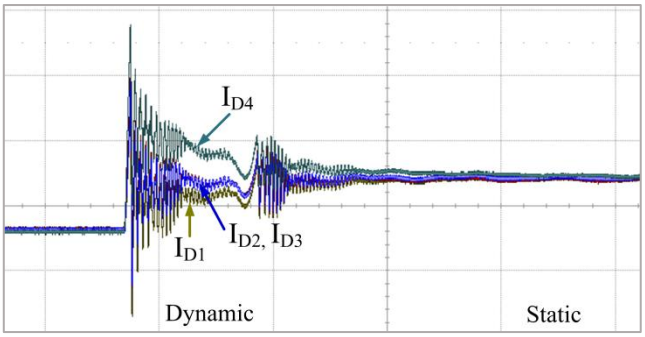
A small 2-layer PCB connects the four MOSFETs symmetrically. Drain connection is on the top layer and the gate and source connections are on the bottom layer. Since the submodule switching frequency is relatively low for the 10kHz 5-level MMC (approximately 2.5kHz for each submodule), the main priority is to keep drain and source connections symmetrical. The gate connection track lengths are designed to be the same. As shown in Figure 3, an individual gate resistor R_{Gi} is required to damp potential gate oscillations caused by the low impedance path.

With all the devices on the same heat sink, the parallel-connected MOSFETs are closely thermally coupled, and therefore junction temperature variations can be minimised, leading to a minimum value of total resistance [26].

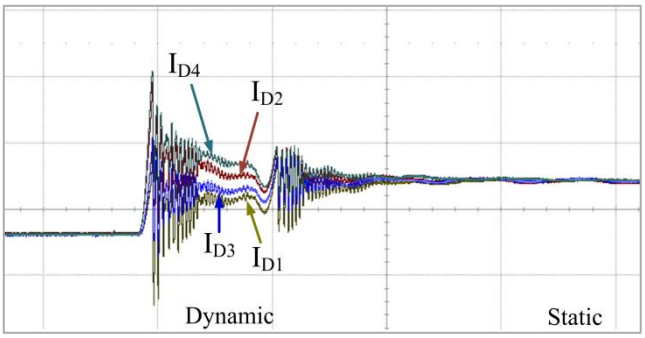
4.2 Static Sharing

To examine current sharing, a single MMC submodule was used as a chopper circuit with 0.5 duty cycle, 3kHz switching frequency and 16A load current. Previously, slowed gate drive has been proposed to address EMC concerns in Si MOSFET MMC [15], therefore dynamic sharing was examined under normal and slowed switching.

The dominant cause of static current unbalance is R_{on} mismatch. Figure 8 shows the experimental result of current sharing between 4 MOSFETs. The results show that the four MOSFETs share current well during the static state.



(a) With R_{Gi}=1Ω, i=1-4 [current: 5A/div, time: 2μs/div]



(b) With R_{Gi}=100Ω, i=1-4 [current: 5A/div, time: 2μs/div]

Figure 8 Current sharing between 4 parallel-connected MOSFETs during turn-on

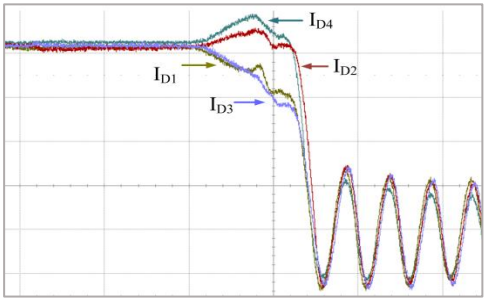
4.3 Dynamic Sharing

Different threshold voltages and individual device transconductances lead to varying switching rates as seen in Figure 8 where MOSFET4 has the lowest threshold voltage and turns on first. The Miller effect then slows down the rise in V_{GS} in the other 3 devices. During turn-on, MOSFET4 takes slightly larger current than the others. The large current overshoot is caused by reverse recovery of the body diode.

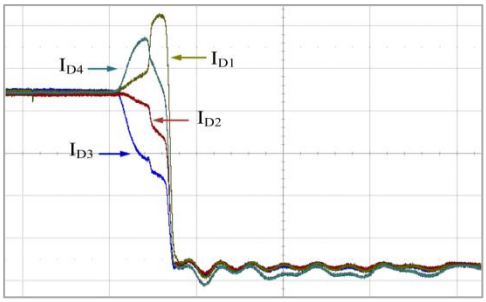
This dynamic current unbalance and the parasitic oscillations are also caused by the combined effects of the drain and source inductances ($L_{D,}$ L_S in Figure 3), the gate and drain resistances ($R_{G,}$ R_{DS} in Figure 3), the gate-source capacitance (C_{GS} in Figure 3), and the drain-source capacitance [26, 27]. With so many factors affecting switching performance, it is practically impossible to match MOSFET switching transients [26].

With increased gate resistance, the turn-on and turn-off processes slow down. Oscillation at turn-on and turn-off are attenuated significantly, reducing EM emissions. However, with slowed switching, dynamic current unbalance is exaggerated at turn-off (Figure 9) due to the increased *R-C* time constant in the gate circuit.

The four parallel-connected MOSFETs face dynamic current unbalance but submodule switching frequency is relatively low so that dynamic unbalance has no appreciable effect on either overall or individual device loss, and is not sufficient to exceed pulse power rating for any individual device.



(a) With R_{Gi}=1Ω, i=1-4 [current: 1A/div, time: 200ns/div]



(b) With R_{Gi}=100Ω, i=1-4 [current: 1A/div, time: 2μs/div]

Figure 9 Dynamic current sharing between 4 parallel-connected MOSFETs during turn-off

5 Heatsink Sizing

Heatsink thermal resistance is calculated using (12) [10]

$$T_J - T_{amb} = \sum_1^{4n} P_i \cdot (R_{\theta(J-S)} + R_{\theta(S-A)}) \qquad (12)$$

where T_{amb} is the ambient temperature, P_i is the power loss of each device, n is the number of submodules in one arm, and $R_{\Theta(J\text{-}S)}$ and $R_{\Theta(J\text{-}A)}$ are the thermal resistances for junction to heatsink and heatsink to ambient respectively.

Based on loss calculations from Section 3, $R_{\Theta(J\text{-}A)}$ for each type of converter, and therefore heatsink size, can be calculated assuming operating junction temperature of 125°C. Table 1 lists the heatsinks and their volumes, showing that the Si MOSFET 5-level MMC heatsink has less than half the volume of that for the SiC MOSFET 2-level converter. For top side cooled GaN HEMT devices, a small central pedestal copper block is required to make contact with the thermal pads [28]. The heatsink volume required for a conventional IGBT 2-level converter is 1600cm^3 for two phase legs [10]. In comparison, the heatsink volume for the three types of converter proposed in this paper is approximately 10 times smaller.

Converter Type	Power Loss (W)	Required $R_{\theta(S\text{-}A)}$ (°C/W)	Heatsink Part No.	$R_{\theta(S\text{-}A)}$	Volume (cm^3)
SiC MOSFET 2-level	38.4	2.53	05DN-01500-A-200	2.3	226.8
GaN 3-level MMC	26.4	3.09	02HN-01500-A-200	3	149.8
Si MOSFET 5-level MMC	20.8	4.28	02HN-01000-A-200	3.9	99

Table 1: Heatsink Comparison between 3 types of converters with 4 devices in parallel-connection

6 Conclusion

Calculated efficiency has been compared for a SiC 2-level converter, a GaN HEMT MMC and a Si MOSFET MMC. Of the three types of converters, the Si MOSFET 5-level MMC with 4 parallel-connected MOSFETs promises lowest loss and requires the smallest heatsink. Parallel connection of MOSFETs to improve efficiency has also been explored, and promises significant loss reductions. Experimental measurements demonstrated excellent static current sharing between parallel-connected devices. Dynamic current showed unbalanced sharing, but since the switching frequency for each submodule is sufficiently low, dynamic current unbalance is not considered to be a problem for MMC.

For MMCs, submodule capacitor size is large. However, the bulky AC filters required for 2-level converters are vastly reduced and the DC filter is eliminated for MMC. SiC MOSFET 2-level converter control is the simplest, whilst that for the Si MOSFET 5-level converter is the most complicated. However the Si MOSFET 5-level MMC provides the highest output waveform quality.

This study is based on currently available Si MOSFET, SiC MOSFET and GaN HEMT devices. It can be concluded that the 4 parallel-connected Si MOSFET 5-level MMC is the most practical choice for LVDC distribution networks.

Acknowledgements

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