THE RISING ROLE OF PHOTONICS IN TODAY'S DATA CENTRES

EL PAPEL CRECIENTE DE LA FOTÓNICA EN LOS ACTUALES CENTROS DE DATOS

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In recent years there has been a rapid growth in demand for ultra high speed data transmission with end users expecting fast, high bandwidth network access. This growth has put data centres under increasing pressure to provide greater data throughput and ever increasing data rates while at the same time improving the quality of data handling in terms of reduced latency, increased scalability and improved channel speed for users. However, data networks are becoming increasingly difficult to scale to meet this growing demand using current well established CMOS technology and architectures. As a result electronic bottlenecks are becoming apparent despite improvements in data management. The inter-related issues of electronic scalability, power consumption, copper interconnect bandwidth and the limited speed of CMOS electronics will be discussed, and the tremendous potential of optical fibre based networks to provide the necessary bandwidth will be illustrated. In addition, some applications of photonics to alleviate speed, throughput and latency issues in data networks will be discussed. Finally, progress in the form of a novel and highly scalable optical interconnect will be reviewed.

En años recientes ha habido un rápido crecimiento en la demanda para la transmisión de datos de velocidad ultra alta con usuarios finales que esperan un rápido acceso a redes de computadoras de alto ancho de banda. Este crecimiento ha puesto a los centros de datos bajo una creciente presión para proporcionar un mayor volumen e incremento de la tasa de datos, al mismo tiempo que se mejora la calidad de los datos que se manejan en términos de latencia reducida, incremento de la expansión y mejoramiento de la velocidad del canal para los usuarios. Sin embargo, las redes del datos están sometidas a un aumento en la dificultad de expandirse encontrando la demanda creciente que emplea la actualmente bien establecida tecnología y arquitecturas CMOS. Como resultado los cuellos de botella electrónicos se hacen manifiestos a pesar de las mejoras en el manejo de los datos. Los problemas inter-relacionados de posibilidades de expansión electrónica para necesidades futuras, el consumo de energía, el ancho de banda de la interconexión de cobre y la limitada velocidad de la electrónica CMOS se discutirán, así como también será ilustrado el tremendo potencial de las redes basadas en fibra óptica para proporcionar el necesario ancho de banda. Además, se discutirán algunas aplicaciones de la Fotónica para mitigar limitaciones en la velocidad, el volumen de datos y los problemas de latencia en las redes de datos. Finalmente, se revisará el desarrollo en la forma de una nueva y altamente expandible interconexión óptica.

PACS: Electronic Bottleneck, Data Centre Networking, Optical Switching, OCDMA

I. INTRODUCTION

Global ICT (information and communications technology) energy consumption has been estimated by the Digital Power Group to be around 1500TWh. This is equal to the total electricity generated annually by Japan and Germany combined and amounts to nearly 10 % of global generation. In addition, the volume of data passing through communication networks is forecast to more than double by 2018 with the largest share of this rise attributable to growth in smart phone and machine to machine (M2M) devices [1]. Smart phones alone generate between 10 and 20 times more data traffic than conventional mobile phones [2]. This growing demand for high speed, low latency data transmission has generated a need for substantially increased capacity and improved connectivity within data centres. However, current data centres performing all data processing based on electronic switching and routing use copper interconnects limited to a capacity of around 1 Gb/s to 10 Gb/s, are becoming less able to meet demand into the future [3]. Issues of increased latency and reduced bandwidth to the user are therefore becoming apparent. In fact Google have reported that an additional latency of 400 ms costs 0.44 % in lost search sessions; while Amazon have reported that an additional latency of 100 ms costs 1 % in lost sales. The reason for this inability to meet demand is two fold. Firstly, the scaling of copper interconnects has resulted in increasing switching delays and an increased additional contribution to chip power density. Secondly, the scaling of CMOS electronics has resulted in significant leakage currents that incur an increase in static power consumption. This has in part been mitigated by the end of supply voltage scaling. However the dynamic switching power is proportional to the square of the supply voltage and therefore the maximum switching speed must be restricted to maintain total power dissipation at a sustainable level. If device power density is not controlled, providing adequate cooling will present an intractable problem and result in an increased risk of

thermal runaway and reduced system reliability. In effect, device thermal density has become a limiting design criterion threatening to bring Moore's law of scaling [4] to an end.

These power consumption considerations have spurred a move to parallel processing using multi-core central processing units (CPUs). However, there is a maximum speed-up beyond which adding more cores gives no additional advantage and the fastest CPUs in data centres today are limited to handling data at around 10 Gb/s. It is apparent that the already significant power consumption of data centre switching and cooling will grow rapidly with data network throughput resulting in sustainability problems in fuel costs and carbon emissions compliance. Furthermore, it has been suggested that the fundamental limits of data center switching which relies on bandwidth limited CMOS electronics is now perhaps being reached [4]. Since intra data centre traffic accounts for some 76 % of total traffic with inter data centre traffic at 17 % and data center to user traffic accounting for only 7.5 %, it is clearly desirable to tackle electronic speed, bandwidth and power consumption issues within the data centre.

Optical fibre has a tremendous bandwidth potential. Only a small fraction of this bandwidth has been utilised for transmission and routing of wavelength division multiplex (WDM) channels in modern metro and long-haul networks. At the data centre, the signal processing, serial MUX/DEMUX and buffering necessary is achieved using relatively slow and power hungry optical-electronic-optical (OEO) transceivers. It is therefore suggested that disruptive technologies are required to tackle power consumption and electronic bottleneck issues within data centres to ensure sustainable data network growth with minimal latency.

All-optical systems using photonic integrated circuits and highly scalable optical interconnects may provide an answer to improve data throughput, reduce power consumption and at the same time provide data rates exceeding Terabits per second.

II. LIMITATIONS OF CURRENT CMOS ELECTRONICS

So what's the problem with CMOS technology? The mobility of silicon imposes a fundamental maximum speed on the silicon transistor of around 100GHz [5]. However, while this speed has been demonstrated for simple cmos devices, microprocessor speed has plateaued at around the 4GHz mark. The limiting factor here is power dissipation. It would be impossible for the millions of transistors in a processor to operate at much faster than 4GHz without thermal runaway and overheating causing the destruction of the chip. This problem has it's root in CMOS transistor scaling.

II.1. CMOS scaling

The well-known CMOS transistor scaling rules first described by Robert Dennard in 1974 describes how transistor size can be reduced while at the same time increasing switching speed and reducing power consumption [6]. Dennard scaling states that as transistor size reduces, power consumption will reduce while maximum clock speed can be increased. An important observation of Dennard scaling is that power density (Watts/unit chip area) has remained approximately constant as transistor density has increased. In addition, the density of transistors has been increasing by a factor of about two every 18 months for over 40 years. Gordon Moore first suggested such an exponential improvement in transistor density back in 1965 with an estimated doubling of transistor density every two years [4]. What has actually happened since then has validated what became known as 'Moore's law' despite the increasing technical challenges of integration. This trend is forecast by Intel to continue until around 2020 [7].

II.2. CMOS SPEED

Despite the continuing validity of Moore's law, Dennard scaling came to an end in 2005 with the development of 90 nm lithography. At this level, transistor gates become too thin to prevent current from leaking into the substrate. In addition, threshold voltage scaling resulted in an increase in junction leakage currents. The relationship $P_d = CV^2F$ relating the switching power consumption P_d to the frequency F in a CMOS inverter [8] illustrates the past success of CMOS scaling. C is the CMOS switch lumped capacitance (sum of junction and gate capacitances) and V is the supply voltage. As transistor dimensions scale smaller, C reduces and the supply voltage can be reduced (since CMOS threshold voltage scales with the gate oxide layer thickness). Power consumption per inverter is therefore reduced and therefore overall chip power density can be maintained at a sustainable level. However, in 2005 leakage current became a problem at the 90 nm technology node due to the scaling of the gate oxide thickness which increases gate oxide tunneling; and the scaling of the threshold voltage which increases sub-threshold currents. These leakage currents have resulted in a rise in chip static power density, P_s and, in the case of junction leakage currents, present the risk of spontaneous transistor state switching and corruption of data. Supply voltage scaling ended at around 1V and helped mitigate the rise in junction leakage current by increasing the threshold voltage, however this has been at the expense of the dynamic power consumption which is proportional to V^2 and chip power density has therefore been increasing as a result. It therefore became necessary to limit the overall chip power consumption, $P_d + P_s$ by reducing the clock frequency F to avoid excessive power density.

High power density runs the risk of causing thermal runaway and destruction of the chip in addition to creating cooling challenges and power consumption cost issues when scaled to the size of a data centre. In the short term it is clear that increasing clock speeds to satisfy demand is therefore not a realistic option.

II.3. *Electronic interconnect scaling*

With the advancement of Moore's Law, both chip speed and chip power consumption are increasingly being affected by on-chip copper interconnect limitations. There are two main types of interconnect at chip level. Local interconnects are very short connections at the device level; and global interconnects are long connections between blocks, carrying for example power and clock signal. The resistance (R) of local interconnects that connect individual MOS transistors increases while the capacitance (C) reduces by the scaling factor. This serves to maintain the RC delay of local interconnects approximately constant with scaling. Since chip size and its complexity has been increasing, global on-chip interconnects have actually increased in length and in number resulting in increased R and C with scaling and increased RC delay as a consequence. This situation is compounded in both local and global interconnects by increasing parasitic capacitance and increasing copper resistivity at very small scales. The consequence of increasing C and R is not limited to increased delay and limits on chip speed. The power consumption of interconnects is directly proportional to capacitance. It therefore follows that power consumption particularly in global interconnects will rise with scaling, and therefore that the interconnect contribution to overall chip power density will increase. While progress has been made to reduce the capacitance of interconnects by using low dielectric constant interconnect separating layers, this approach has not fully mitigated the rise in capacitance and the issue persists [8].

As data centres scale to meet demand, rack and switching/routing copper interconnects must get longer to connect server racks to each other and to routers and switches. The number and total length of interconnects will therefore increase exponentially with scaling. As a consequence, increasing power consumption will result since the capacitance of each interconnect rises with the length of interconnect; and the bandwidth of the copper interconnects will reduce as the delay increases as a result of increasing resistance and capacitance. Thus copper interconnects and electronic switches in data centres are limited to 10 Gb/s serial data rates per channel with a maximum range in the 10's metres with 100 m only possible at very high power consumption.

II.4. *Computing speed*

As discussed, leakage current and global interconnect problems have made it necessary to limit power consumption by reducing the clock frequency and therefore also the processing speed. Consequently, since 2005 chip manufacturers Intel and AMD have concentrated on introducing parallel processing CPUs using multicore processors to increase processing power with the latest high performance server processors capable of supporting up to 10 Gb/s data rates. While parallelism can do nothing to reduce power consumption or help overcome interconnect bandwidth limitations, it can contribute to reducing latency by speeding up the processing of requests. Parallel processing can, to a degree compensate for limited clock frequencies but clearly results in increased power consumption since an effective doubling in performance requires at least two processors. In addition, Amdahl's parallelism law states that 'If a computation has a serial component f % and a parallel component p %, then the maximum speed-up given an infinite number of processors is $(f+p)/f$. Clearly, the greater the parallel portion p, the higher the speed-up [9]. However *there is a fundamental maximum improvement in computational speed that is dependent upon the proportion of serial computation, beyond which further additional parallel processors will contribute a rapidly diminishing improvement in processing speed.*

The performance per watt which is initially constant will eventually decrease rapidly as the number of processors is increased beyond the optimum number. As the number of parallel processors n increases the maximum speed-up value is achieved, beyond which adding more processors provides diminishing additional computational advantage and increases power consumption.

In fact, when a request is implemented in a parallel computing system, the overall response time is dictated by the distribution of parallel operations and therefore by the slowest operation. Latency in any of the parallel operations will therefore reduce the ideal speed-up discussed above.

In the short term, while effective cooling can be achieved, Moore's law will hold. However power density is no longer approximately constant as previously predicted by Dennard's Law but will increase with transistor density. The maximum power density that can be sustained together with the limitations of parallelism and copper interconnect bandwidth lead to a fundamental limit on the processing power of present electronic data centres. Research into reducing CMOS leakage currents has demonstrated improvements in data handling capacity and power efficiency [10]. However, these improvements have been slow with only modest gains in reduced leakage current achieved. Graphene [11] and nanowire [12] technologies are being investigated as a replacement for current CMOS based devices. However, research in these areas is in its infancy and operational devices are many years from market. The solution to satisfying the rapid increase in demand for processing power in data centres is unlikely to be found using present CMOS technology.

III. OPTICAL NETWORKING

III.1. *Optical fibre bandwidth*

The development of optical fibre based systems to provide all-optical interconnects and perform for example, switching and MUX/DEMUX operations may hold the key to improving data throughput, and reducing latency and power consumption. The very high bandwidth of optical fibre and the rapid increase in demand for data transmission bandwidth have already resulted in optical fibre technology becoming an important building block for point to point

transmission in data networks. In fact, optical fibre has become one of the fastest growing transmission media for new data network installations and upgrades [13]; and is now ubiquitous in long haul communications. Present transmission rates exceed 1 Tb/s over long distances on a single fibre. In a similar way, the use of optical fibre for interconnects within the data center opens up the possibility of alleviating the electronic bottleneck by greatly improved bandwidth, lower power consumption and lower attenuation than copper based interconnects. In addition to high bandwidth, optical fibre has several significant advantages over traditional copper cabling including:

- Low attenuation allowing much longer distances between repeaters.
- No resistive heating.
- Immunity to electromagnetic interference, crosstalk and corrosion.
- More durable, compact and lighter in weight.
- Higher CAPEX but lower overall cost in the long term.

To take full advantage of the low attenuation of around 0.15 to 0.2 dB/km in the 3rd window C-band frequency range (1525nm–1565nm) and the development of the Erbium Doped Fibre Amplifier (EDFA), Dense Wavelength Division Multiplexing (DWDM) was developed. Today, modern transmission systems can easily transmit 160 wavelength data channels at 10 Gb/s each over a single fibre, creating aggregate throughput of 1.6 Tb/s. Despite the low attenuation and without the availability of optical amplifiers signal regeneration was required particularly in long haul fibre optic systems. Around 1990, the EDFA (Raman Amplifiers [14]) became available allowing optical signal amplification without the need for OEO conversion.

The following analysis illustrates the immense theoretical capacity of optical fiber. The theoretical maximum capacity at the maximum sampling rate (or symbol rate) of a band-limited noise free channel is given by the well-known Nyquist theorem, $C = 2Blog_2(2n)$, where C is the channel capacity in bits per second (b/s); B is the bandwidth (in this case of the fiber) in Hertz (Hz); and n is the number of bits used to describe each symbol. This theorem states that the maximum symbol transmission rate is twice the bandwidth of the channel to avoid inter-symbol interference (ISI) with neighboring samples. It seems apparent that the channel can carry an infinite amount of information by simply increasing n, however a noise free channel is unattainable. Using the well-known Shannon-Hartley theorem, the theoretical maximum capacity in the presence of noise is given by, $C = Blog_2(1 + (\mathfrak{B}/Bh\gamma_o)^{1/2})$, where C and B are as before, $\mathfrak{B}$ is the power guided by the fiber in Watts, h is Planck's constant; and γ_o is the centre frequency of the fibre bandwidth in Hz. The quantity $(\mathfrak{B}/Bh\gamma_o)^{1/2}$ is the signal to noise ratio of the channel measured as the ratio of the average received signal power to channel quantum shot noise at the receiver. It is assumed that the potential bandwidth of fibre is of the order of 50 THz. In the use of this figure it is assumed that there is a sharp roll-off which is limited by the attenuation in the fibre medium increasing outside its transmission window. The center frequency γ_o is taken to be that corresponding to the minimum attenuation of fibre at a wavelength of 1550 nm. As a rule of thumb the maximum value of $\mathfrak{B}$ is around 100 W. This limitation is due mainly to heating in the fiber around imperfections which will result in the eventual catastrophic destruction of the fibre at power input levels above the rate at which the fiber can dissipate heat. High optical input powers will also cause various non-linear effects resulting in a reduction in capacity. In addition, stimulated Brillouin and Raman scattering will result in an increase in noise proportional to $\mathfrak{B}$ which will quickly outweigh the quantum shot noise and therefore result in a reduction in maximum channel capacity. Substitution of these values into the above equation for channel capacity, C results in an ideal theoretical maximum value of C at about a colossal 600 Tb/s for a single mode fibre. It's worth noting that the capacity of a very long fibre will be reduced due to attenuation. The present experimental limit is around 100 Tb/s using multi-core fibre over many 10's of kilometres [15]. It is therefore clear that optical fibre has the potential to meet future demand for very high serial data rates; and given the necessary serial WDM channel MUX/DEMUX and optical switching technology, optical fibre could be utilized to provide highly scalable, high speed all-optical interconnects in data networks.

III.2. Inter data centre networking

In today's broadband networks the use of state of the art optical technologies has vastly improved single wavelength channel data rates. Serial data rates per a single optical wavelength channel have grown from the adoption of OC-1 in 1980 to a maximum of OC-768 today. OC-n refers to the serial data capacity $n \times 51.84$ Mb/s of each optical carrier in a DWDM) configuration. As an example of the current state of the art, DWDM systems are commercially available which use OC-768 across 80 channels with a 50 GHz ITU grid. The bandwidth used is therefore 4THz and the total bit rate achieved is $80 \times 768 \times 51.48$ Mb/s or approximately 3.2 Tb/s. However, the vast optical channel bandwidth available cannot be fully exploited due to limited electronic switching speeds in the MUX/DEMUX electronics used for data processing at the fibre ends. For example, using a 50GHz ITU grid, the theoretical capacity of each channel is around 0.5 Tb/s per wavelength channel. However, the best OC-768 systems presently manage only 768×51.84 Mb/s or around 40 Gb/s per a single wavelength channel.

Despite the many technical challenges to the realisation of all-optical data networks, advances have been made in the use of optical routing. The recent development of the reconfigurable optical add/drop multiplexer (ROADM) has allowed the reduction in use of power hungry and band limited OEO transceivers in optical cross connects for data network metro and long haul nodes [16]. ROADMs allow individual DWDM wavelengths to be added or dropped. However wavelength granularity is low and the best systems

use 80 channel wavelengths. The capacity of each of these channels could be better utilised by, for example using optical time division or optical code division MUX/DEMUX.

III.3. Intra data centre networking

With intra data center traffic accounting for 76 % of total data network traffic, the use of low power high bandwidth fibre based optical switching and routing systems within the data center could provide a significant contribution toward reducing power consumption and latency. Many such schemes for intra data center all-optical switching and routing have been proposed for optical circuit switching (OCS). These schemes employ dense wavelength division multiplexing (DWDM) and highly scalable, high port count all-optical switches; and promise reduced contention, latency and power consumption.

Helios [17] is a hybrid 2-layer WDM based architecture using modular performance optimized data center (POD) units. At the POD layer, packet switching is achieved using conventional electronic commodity switches; and at the core layer, optical circuit switching is used in parallel with commodity packet switching. Optical circuit switching is achieved using MEMS switches in WDM links, facilitating the use of optical interconnects and reducing the requirement for power hungry transceivers and commodity switches. This scheme is ideally suited to long-term transfers between racks, however, using MEMS switches it suffers from high reconfiguration times of around 15ms. However, ultimately both systems are limited by the need for electronic packet switching since the optical buffering required for all-optical packet switching (OPS) has not yet been realized.

Mordia [18] is a hybrid network that uses wavelength selective switches (WSS) for optical circuit switching in WDM links. Each node contains a WSS and Ethernet 10G commodity packet switches. Wavelengths can be added or dropped at each node using the OCS. The main advantage of this system over Helios is a faster optical circuit reconfiguration time of 11.5 μs.

A recent approach to achieving a form of optical packet switching is the DOS (Datacenter Optical Switch) architecture [19]. Here the switching of optical packets is based on an arrayed waveguide grating router (AWGR) switching fabric where different inputs can reach the same output simultaneously using different wavelengths avoiding contention in the wavelength domain. This non-blocking switching is achieved using a tunable wavelength converter at each node. By selectively tuning the wavelength converter, a node can access any other node via the AWGR and packets are therefore routed accordingly. This system is power efficient too since the signal is delivered to the output port via a specific wavelength rather than using broadcast and select where associated power dividing losses occur. In simulations low latency, high-throughput switching was reported. In addition, latency was found to be almost independent of the number of input ports and saturation did not occur even at 90 % input loads. The AWGR with tunable wavelength converter switch uses mechanisms such as the third order non-linearity four-wave mixing (FWM) and cross-phase modulation (XPM) in addition to second order non-linear effects to achieve wavelength conversion. Tuning is achieved by changing the wavelength of the pump laser. The non-linear processes outlined above produce an output from the wavelength conversion medium at a different wavelength to the input signal wavelength. The AWGR will therefore route the wavelength shifted signal to a different port. Fast tuneable lasers and non-linear media are required to ensure switching rates suitable for packet switching. Successful tuning of an input signal with wavelength 1546 nm to generate an output signal over the range 1535 to 1557 nm at 40 Gb/s has been achieved [20].

Data centres have widely employed optical fibre interconnects. While these have solved the issues of space and reach, they use CMOS based optical/electronic/optical (OEO) transceivers which until recently have been limited to 10 Gb/s. However, Intel have announced a new MXC type optical interconnect which is designed to connect top of the rack (ToR) switches to each other and to the core switches or to connect servers to extra storage or graphic processing units (GPU's). This interconnect is capable of 800 Gb/s in total each way with a maximum of 25 Gb/s serial data rate per fibere (64 fibres with 32 each way) [21]. It can operate up to 300 m at reduced power consumption compared with copper cables. However, while this technology can overcome the attenuation and bandwidth limits of copper cables, it still requires bandwidth-limited and power hungry OEO transceivers.

The use of Optical Code Division Multiple Access (OCDMA) has also be considered for improving interconnect scalability. An analysis and proof-of-concept demonstration of such a system has been presented [22]. Here, an incoherent Optical Code Division Multiplexing (OCDM) implemented over Optical Time Division Multiple Access (OTDMA) system demonstrated very significant improvements of the overall scalability with no significant degradation in system performance when compared with conventional multiple access approaches. Further improvement in system scalability has been reported in [23].

IV. ADVANCES IN (ALL) OPTICAL SIGNAL PROCESSING

IV.1. III-nitride photonics

To realize fast, low power all-optical systems for both circuit and packet switching and routing in the data center, both passive and non-linear devices will be required at on-chip, chip to chip and intra data center levels. Current research is aimed squarely at integrating optoelectronic devices with electronic CMOS devices on the same substrate. Successful integration would greatly reduce power consumption and improve the bandwidth at board level. It is highly desirable for this optoelectronic technology to be compatible with CMOS fabrication techniques since compatibility would negate the requirement to develop

new fabrication technology, cut the cost of fabrication and allow conventional CMOS devices to be integrated with optoelectronic devices on the same chip. In 2012, IBM reported the successful monolithic integration of the optical modulators, photodetectors, waveguides and WDM multiplexers (using a ring resonator design for add/drop functionality) with CMOS electronic components (transistors, capacitors, resistors) using a low cost standard 90 nm CMOS fabrication process [24]. The modulator employs a Mach-Zehnder interferometer design with one arm using a p-i-n diode to introduce a phase shift using carrier injection which takes advantage of the first order susceptibility of silicon through free carrier absorption (FCA) change and free carrier index (FCI) change. IBM have reported serial data rates of 25 Gb/s, using four-channel wave-division multiplexing (WDM) using this device.

However silicon photonics have a major drawback – with a centro-symmetric structure and indirect bandgap it exhibits no second order non-linear effects and therefore cannot easily be applied to electro-optic amplitude modulation or for lasing. The existence of the second order ($\chi^{(2)}$) non-linearity allows the electro-optic effect to be used for higher speed modulation and switching in data networks. Such devices would also reduce the need for OEO transceivers and electronic switching in addition to reducing power consumption. Despite attempts to artificially induce a second order non-linear characteristic by, for example introducing strain to the crystal. However the field of strained silicon photonics is still in its infancy.

Recently, III-nitride semiconductors have been identified as contenders for the development of high speed inter sub-band (ISB) devices for application in data networks and in other areas. III-nitride semiconductors that show promise are Gallium Nitride (GaN) and Aluminium Gallium Nitride (AlGaN) and their alloy. These III-nitride wide bandgap semiconductor materials are compatible with CMOS fabrication techniques and they exhibit the second order non-linearity required for lasing and high speed electro-optic devices for modulation and switching in data networks. Such devices would reduce the need for OEO transceivers and electronic switching and reduce power consumption.

III-nitride materials may therefore hold the answer to reducing interconnect power consumption and allow single channel serial data rates (which maxed out at 40 Gb/s (OC-768) around 2007) to be exceeded. With a large conduction band offset of about 1.8 eV and a sub-picosecond ISB relaxation time, these materials are therefore attractive for the development of the ultrafast photonic devices in the near infra-red ideal for use in data networks. In addition, these materials can operate at high temperatures, high power and they exhibit low attenuation in the near infrared wavelength region because of their wide band-gap. Modulation of III-nitride refractive indexes is possible by carrier injection making these materials compatible for use as modulators in fibre optic based communication systems. These features make III-nitride materials attractive for the development of tuneable optical phased array devices not possible with silicon such as AWGRs used in data networks for WDM MUX and DEMUX. Devices that have been realised in the lab include 2×2 directional couplers and an eight wavelength AWGR.

IV.2. Quantum cascade photodetectors

Unlike quantum well infrared photodetectors (QWIPs), quantum cascade detectors (QCDs) are photovoltaic devices that can be operated at zero bias and therefore need no power supply. In both types of devices, detection relies on photon absorption by electronic sub-band transitions in semiconductor quantum wells (QWs) and the operating wavelength can be widely tuned by choice of the QW thickness.

A room temperature QCD employing a GaN/AlGaN/AlN heterostructure has been reported [25]. The design takes advantage of the large internal field that exists in III-nitride semiconductors to generate the essential saw tooth energy level structure. This device operates in the near-IR spectral range covering the all important optical fiber low attenuation c-band. It was shown to exhibit room temperature responsivity of 10 mA/W or 1000 V/W at zero bias and at a wavelength of 1700 nm. A GaN/AlGaN QCD has been demonstrated [26]. It was suggested that speeds in excess of 80 GHz could be achieved by reducing the mesa size.

IV.3. Electro-optic modulators

The realization of an efficient electro-optic modulator requires strong second order susceptibility ($\chi^{(2)}$). A strong $\chi^{(2)}$ susceptibility was demonstrated using a device based on the integration of a single crystal of GaN on a Si (100) substrate heterostructure [27]. This device uses engineered GaN micro-rings to provide dual resonance at wavelengths of 1560 nm and 780 nm. Efficient tunable second harmonic generation at 780 nm was demonstrated and the $\chi^{(2)}$ susceptibility was measured as high as 16 ± 7 pm/V. Since GaN has a wide transparency window, this device structure was suggested to be a viable route for the second harmonic generation of optical wavelengths in the range from far-IR to near-UV enabled by a combination of $\chi^{(2)}$ sum and difference frequency processes. It is suggested that the strong $\chi^{(2)}$ susceptibilities reported using GaN on Si platform will be useful in the development of electro-optic modulators and optical parametric oscillators.

An electro-optic modulator based on three periods of 1.3 nm thick GaN QWs with 3 nm thick AlN barriers grown on a 1 μm AlN template has been demonstrated [28]. The wells were n-doped with Si at 2×1019 cm^{-3} with the active region sandwiched between two 500 nm thick $Al_{0.5}Ga_{0.5}N$ bottom and top contact layers which were n-doped with Si at 5×1018 cm–3. These layers also acted as confinement layers for the waveguide. Under negative bias, the three QWs were depleted and therefore transparent and under positive bias, the electron population of the QWs gave rise to ISB

absorption at a wavelength of 1500 nm. Modulation depths of 14db for a voltage swing of −9V/ + 6V; and 10db for a voltage swing of ±5V was recorded. A 12 db modulation depth of 12db is required for optical modulators to comply with the 10 − 12 bit error rate (BER) standard used in fiber optic data networks.

A room temperature electro-optic modulator based on electroabsorption modulation over the wavelength ranges 1200 nm to 1670 nm and 2100 nm to 2400 nm in GaN/AlN coupled QWs has been demonstrated [29]. The electro-modulation reported is due to electron tunneling between a wide well reservoir and a narrow well separated by an ultrathin AlN barrier. The maximum modulation depth reported was 44 % at a wavelength of 2200 nm. The −3 db cut-off was measured at 11.5 MHz with a device mesa size of 700 μm^2 and is limited by the RC time constant. It was suggested that a much larger cut-off frequency should be attainable with smaller mesa sizes.

Arrayed waveguide gratings. III-nitride materials are better suited for the development of AWG's than silicon or InP since the refractive index of III-nitrides is less than 2.3 making them more compatible with coupling with silica fibers; and intrinsic losses are lower due to a wide band gap compared to the 1550nm application wavelength. A 1x8 GaN-AlGaN based WDM demultiplexer AWG with one input waveguide and 8 output waveguides has been demonstrated [30]. The fabrication process involved photolithographic patterning and dry etching. The AWG was designed to give an output spacing of 2nm. The reported rejection ratio of 10 was measured for most of the output ports.

IV.4. All-Optical Switches

The non-linear properties of Silicon doped GaN/AlN quantum dot (QD) and quantum well (QW) superlattices were evaluated for the development of all-optical switches and wavelength converters for data networks operating at room temperature and at a wavelength of 1550 nm [31]. The third order non-linear susceptibility measured was 5 times larger in the QD samples than in the QW samples and this result is attributed to higher quantum confinement. The ultrafast nature (100 fs) of ISB transitions in addition to the higher third order susceptibility make GaN/AlN heterostructures good candidates for the development of all-optical high speed, high contrast ratio and low saturation intensity devices suitable for applications in multi terabit data networks.

ISB transitions in GaN QWs for use as an all-optical switch were investigated [32]. For a −3 db extinction, a switching power of 100 pJ was reported improving to 25 pJ. All-optical switching was verified for wavelengths of 1550 nm and 1700 nm and the device was able to operate for 4 pulses with an interval of 1 ps. An extinction ratio better than 10 dB was reported.

V. TOWARD AN ALL-OPTICAL FUTURE

It is clear that the fundamental limits on electronic switching speeds, power consumption and parallel processing will in the near future severely affect the ability of data networks to satisfy, both quantitatively and qualitatively, the exponentially increasing demand for data. While the introduction of all-optical switching schemes [33–36] and optical interconnects can improve latency, contention and capacity, a new solution is required to improve processing speed to take full advantage of the potential serial data rate capacity of such systems. The requirement for a new disruptive technology is therefore inevitable. Ideally, development of a photonic transistor allowing faster switching which is compatible with CMOS fabrication techniques would allow cheaper to market solutions than developing an all new ground-up fabrication technology. Silicon photonics devices can be fabricated using present CMOS fabrication techniques and therefore this technology is being investigated for the development of future optical signal processing systems [37].

Given a future where networks will need to perform ultra-high speed serial data processing all optically; there will be basic requirements for all optical MUX/DEMUX devices capable of performing at speeds well beyond that available today. To overcome this electronic bottleneck Glesk *et al* developed an ultrafast all optical photonic switch known as TOAD (Terahertz Optical Asymmetric Demultiplexer [33]. The device is based on a fiber version of a Sagnac interferometer with built in Semoconductor Optical Amplifier (SOA). The SOA serves as the very fast all optically controlled optical nonlinearity which changes interferometrical properties of the Sagnac interferometer in a controlled manner thus enabling all optical switching. A 250 Gbit/s all optical demltiplexing of OTDMA signal has been demonstrated with the TOAD device [34]. However the SOA suffers from the currier recovery time limitations. To evercome this bottleneck a novel all optical device was dveloped, manufactured and demonstrated [34, 35]. The device has a Mach-Zehnder interferometric structure with one arm composed of a Si nanowire. The second arm is a subwavelength waveguide grating (SWG) structure. Device is capable of self-switching and its all optical switching operation was demonstrated at 1 Tbit/s.

VI. CONCLUSIONS

Optical fibre networks have a vast potential data handling capacity. However this capability is becoming severely limited by serial data processing speed abilities of currently available CMOS electronics. Speed-up using parallel processing is confounded by the fundamental limits of Amdahl's Law. This scenario will soon hinder the ability of data networks to scale up to meet exponentially increasing demand for capacity. While all-optical wavelength routing can help improve data network throughput, ultimately at network endpoints any such improvement will be choked by fundamentally limited CMOS electronic signal

processing capabilities. There is a need for the development of a disruptive technology to overcome this bottleneck. A promising candidate is all-optical signal processing. Progress has been made in the development of the photonic devices necessary to achieve this goal. However any further progress will require speedy development of ultrafast "all-optical transistor" based photonic logic gates.

REFERENCES

[1] "Cisco Global Cloud Index: Forecast and Methodology, 2012-2017," Cisco, *http://www.cisco.com /c/en/us/solutions/collateral/service-provider/global-cloud-index gci/Cloud_Index_White_Paper.html* (March 30, 2014).

[2] "Explosive Growth in Data Traffic and the future of Global Communications Infrastructure," Ntt, *http:// www.ntt.com/ resource-centre/ article/ data/ global -watch-02.html* (March 30, 2014).

[3] D. Barney, "The great cloud bottleneck: How capacity issues can kill your cloud project." Redmondmag, *http://redmondmag.com/articles/2011/12/01/cloud-bottleneck -issues.aspx* (March 30, 2014).

[4] G. Moore, "Cramming More Components onto Integrated Circuits," Electron. Mag. 38 (8) (1965).

[5] Heydari, Babak *et al.* "Millimeter-wave devices and circuit blocks up to 104 GHz in 90 nm CMOS." Solid-State Circuits, IEEE Journal of 42.12 (2007): 2893-2903.

[6] R. H. Dennard, *et al.*, "Design of ion-implanted MOSFETs with very small physical dimensions," IEEE Journal of Solid-State Circuits 9 5, (1974).

[7] J. Hruska, "Intel's former chief architect: Moore's law will be dead within a decade," Extremetech, 30 August 2013, *http//www.extremetech.com/computing/165331-intels-chief-architect-moores-law-will-be-dead-within-a-decade* (March 30, 2014).

[8] R.H. Havemann, J.A. Hutchby, "High-performance interconnects: an integration overview," Proceedings of the IEEE 89 5, (2001).

[9] T. Brian, "Putting multicore processing in context: Part One," Embedded, 9 January 2006, *http://ww.embedded.com/design/mcus-processors-and-socs/4 006507/Putting-multicore-processing-in-context-Part-One* (22 September 2014).

[10] S. K. Singh, B. K. Kaushik, D.S. Chauhan, S. Kum, "Reduction of Subthreshold Leakage Current in MOS Transistors," World Applied Sciences Journal 25 3, (2013).

[11] D. Graham-Rowe, "Better Graphene Transis- tors," Technologyreview, 17 March 2008, *http://www.technologyreview.com/news/ 409775/ better-graphine-transistors/* (30 March 2014).

[12] "New '4-D' Transistor is preview of future computers," Purdue, 4 December 2012, *http://www.purdue.edu /newsroom/releases/2012/Q4/new-4-d-transistor-is-preview-of-future-computers.html* (March 30, 2014).

[13] "The Optical Fibre Advantage," Syringanetworks, *http://www.syringanetworks.net/resources/industry_library/ the_optical_fiber_advantage/* (September 22, 2014).

[14] S. Singh, R.S. Kaler, "Flat-Gain L-Band Raman-EDFA Hybrid Optical Amplifier for Dense Wavelength Division Multiplexed System," Photonics Technology Letters IEEE 25, 3 (2013).

[15] J. Sakaguchi, Y. Awaji, N. Wada, A. Kanno, T. Kawanishi, T. Hayashi, T. Taru, T. Kobayashi, and M. Watanabe, "Space Division Multiplexed Transmission of 109-Tb/s Data Signals using Homogeneous Seven-core fiber," IEEE Journal of Lightwave Technology 30, 4 (2012).

[16] "Advances in Roadm Technologies and Subsystems," Enablence, *http:// www. enablence. com/ media/ media-manager/pdf/375-enablence-rl-article-advancesinroadm.pdf* (22 September 2014).

[17] N. Farrington, "Helios: a hybrid electrical/optical switch architecture for modular data centres" ACM SIGCOMM Computer Communication Review 41,4 pp. 39-350 (2011).

[18] Porter, George, *et al.* "Integrating microsecond circuit switching into the data center." Proceedings of the ACM SIGCOMM 2013 conference on SIGCOMM. ACM, (2013).

[19] Y. Xiaohui, Y. Yin, S.J.B. Yoo, P. Mejia, R. Proietti, and V. Akella. "DOS: A scalable optical switch for datacenters." In Proceedings of the 6th ACM/IEEE Symposium on Architectures for Networking and Communications Systems. p.24. ACM, (2010).

[20] H. Hao, *et al.* "Tunable all-optical wavelength conversion based on cascaded SHG/DFG in a Ti: PPLN waveguide using a single CW control laser." Photonics Journal IEEE 4, 5 (2012).

[21] Brodkin, J., "Intel's 800 Gbps cables headed to cloud data centers and supercomputers," Arstechnica, 10 March 2014, *http//www.arstechnica.com/information-technology/2014/03/intels-800gbps-cables-headed-to-cloud-data-centers-and-supercomputers/* (September 22, 2014).

[22] T. B. Osadola, S. K. Idris, I. Glesk, and W. C. Kwong, "Network Scaling Using OCDMA over OTDM," IEEE Photon. Tech. Lett. 24, 5 (2012)

[23] I. Glesk, A. Buis, A. Davidson, "How Photonic Networking Can Help Data Centres," in 15th International Conference on Transparent Optical Networks (ICTON 2014), 6-10 July 2014, Graz, Austria, paper TuC2.2,

[24] A. Solomon, *et al.* "A 90 nm CMOS integrated nano-photonics technology for 25Gbps WDM optical communications applications." Electron Devices Meeting (IEDM) (2012).

[25] A. Vardi, *et al.* "Near infrared quantum cascade detector in GaN/AlGaN/AlN heterostructures." Applied Physics Letters 92,1 011112 (2008).

[26] A. Vardi, *et al.* "High-speed operation of GaN/AlGaN quantum cascade detectors at $\lambda \approx 1.55$ μm." Applied Physics Letters 93, 19 (2008).

[27] X. Chi, et al. "Integrated GaN photonic circuits on silicon (100) for second harmonic generation," Optics express 19, 11 (2011).

[28] H. Machhadani, *et al.* "GaN/AlGaN intersubband optoelectronic devices." New Journal of Physics 11,12 125023, (2009).

[29] L. Nevou, *et al.* "Short-wavelength intersubband electroabsorption modulation based on electron tunneling between GaN/AlN coupled quantum wells." Applied Physics Letters 90, 22 (2007).

[30] H. Rongqing, *et al.* "III-nitride-based planar lightwave circuits for long wavelength optical communications." Quantum Electronics, IEEE Journal of41.1 (2005): pp. 100-110.

[31] F. Guillot, *et al.* "Si-doped GaN/AlN quantum dot superlattices for optoelectronics at telecommunication wavelengths." Journal of applied physics 100, 4 (2006).

[32] N. Iizuka, K. Kaneko and N. Suzuki. "All-optical switch utilizing intersubband transition in GaN quantum wells.ÏEEE Journal of Quantum Electronics" 42, 8 (2006).

[33] J. P. Sokoloff, P. R. Prucnal, I. Glesk, and M. Kane, "A Terahertz Optical Asymmetric Demultiplexer (TOAD)," IEEE Photonics Technology Letters 5, 61 (1993).

[34] I. Glesk, J. P. Sokoloff and P. R. Prucnal, "Demonstration of all-optical demultiplexing of TDM Data at 250 Gb/s," Electronics Letters 30, 4 (1994).

[35] I. Glesk, P.J. Bock, P. Cheben, J.H. Schmid, J. Lapointe and S. Janz, "All-optical switching using nonlinear subwavelength Mach-Zehnder on Silicon," Optics Express 19, 15 (2011).

[36] I. Glesk, P.J. Bock, P. Cheben, J.H. Schmid, J. Lapointe and S. Janz, "Picosecond all-optical switching using nonlinear Mach-Zehnder with silicon subwavelength grating and photonic wire arms," Optical and Quantum Electronics, 44, 12 (2012).

[37] M. Glick, S. Rumley, G Dongaonkar, Q. Li, K. Bergman, and R. Dutt. "Silicon Photonic Interconnection Networks for Data Centers." In Proceedings of the 2013 IEEE Photonics Society Summer Topical Meeting Series, Waikoloa, HI, USA, pp. 8-10 (2013).