Hybrid Multilevel Converter with Cascaded H-bridge Cells for HVDC Applications: operating principle and scalability

G.P. Adam, I.A.M Abdelsalam, K.H. Ahmed and B.W. Williams

Abstract —**Hybrid multilevel converters are contemplated in an attempt to optimize the performance of voltage source converters in terms of magnitude of semiconductor losses and converter footprint, and to achieve additional features such as dc short circuit proof, which is essential for a high integrity multi-terminal HVDC grid. Therefore, this paper considers an emerging hybrid cascaded converter that offers the dc side short circuit proof feature at reduced loss and footprint compared to the existing multilevel and other hybrid converters. Its operating principle, modulation and capacitor voltage balancing strategies are described in detail. Furthermore, hybrid converter scalability to high voltage applications is investigated. The validity of the modulation and capacitor voltage strategy presented are confirmed using simulation and experimentation. The hybrid cascaded converter is extendable to a large number of cells, making it applicable to high voltage applications, and operation is independent of modulation index and power factor. On these ground, the converter is expected to be applicable for both real and reactive power applications**.

Key words— **DC fault reverse blocking capability; half and full-bridge modular multilevel converters; hybrid multilevel converters; and voltage source converter based high-voltage direct current transmission systems.**

I. INTRODUCTION

The recent increased in use of voltage source converters in medium and high voltage applications has motivated academics and industrial researchers to develop alternative converter topologies that address some of the limitations of the modular converter regarding level of semiconductor losses and footprint[1-17].

Currently the modular multilevel converter (MMC) is widely adopted by many HVDC manufacturers for high dc and flexible ac transmission system applications[7, 18-28]. However, the flow of three current components in the converter arms that are associated with the converter's ac and dc power exchanges, plus the circulating currents between converter arms, represent a major concern as these increase semiconductor losses significantly [11, 16, 19-22, 25, 29-38]. Furthermore, the large number of sizeable cell capacitors in the modular converter arms is seen as a major barrier, hampering its adoption in offshore applications where platform costs represents a significant portion of the overall capital cost. These concerns are exacerbated by vulnerability to dc side faults, as the half-bridge modular converters are unable to block an ac grid contribution so as to suppress dc link faults [10, 39, 40]. A full bridge modular topology can suppress this dc fault vulnerability, but with significant increase in conversion losses as the number of semiconductor devices in the active conduction path is twice that of the half-bridge modular converter. Many transmission system operators see the later solution as no go area as it is perceived to increase the operational losses over the lifetime of the transmission systems. These difficulties have initiated research into new generation of voltage source converters known as hybrid multilevel converters or mixed topologies voltage source converters. These new converter generations can potentially optimize the performance for a given application. For example, the hybrid converter with ac side H-bridge cells presented in [41-43] offers a small footprint as it requires a quarter the number of cell capacitors as the modular converter, plus offers dc short circuit protection. Another hybrid converter version that can optimize both conversion losses and footprint is presented in [42, 44, 45], where this converter also offers dc fault reversed blocking capability feature (dc link short circuit proof). A new hybrid converter that uses H-bridge cells is presented in [46], but no details are presented on its operational principle or capability at the device or system level.

This paper describes the operational principle, modulation and capacitor voltage balancing of the hybrid converter presented in [46], which is called throughout this paper as hybrid cascaded converter with dc side H-bridge cell. Additionally, this paper presented simulation and experimental results in sections I and 0 to substantiate the theoretical discussion presented II. The scalability of the hybrid cascaded converter to medium and high applications is investigated in section IV. The discussions presented in sections II, III, and IV show that the hybrid multilevel converter being investigated in this paper is promising in wide range of applications as well as its scalability to a large number of cells, with minor modifications needed to the control and modulation of the established modular converter.

II. HYBRID MULTILEVEL OPERATING PRINCIPLE

Fig. 1(a) shows a single-phase hybrid cascaded converter with two dc side H-bridge cells. When the capacitor voltage across each dc side H-bridge cell is regulated at $½V_{dc}$, five output voltage v_a, levels (V_{dc}, $½V_{dc}$, 0, $-½V_{dc}$, $-V_{dc}$) can be generated between terminals a_1 and a_2. The switch states that generate these five voltage levels are summarised in Table 1. The switch states of the H-bridge cells that can be utilised to generate voltage levels V_{dc} and $½V_{dc}$ are the same as those for generation of voltage levels $-V_{dc}$ and $-½V_{dc}$. The converter output voltage is synthesized according to:

G.P. Adam and B.W. Williams are with the Electronic and Electrical Engineering Department, University of Strathclyde, Glasgow, UK (email: grain.adam@strath.ac.uk and barry.williams@strath.ac.uk).

I.A.M Abdelsalam with the Electronic and Electrical Engineering Department, University of Strathclyde, Glasgow, UK, and on leave from Arab Academy for Science Technology and Maritime Transport, Cairo branch(email: Ibrahim.abdallah@strath.ac.uk).

K.H. Ahmed is with the School of Engineering, University of Aberdeen, Aberdeen, AB24 3UE, UK (email: Khaled@eee.org).

$$v_a = [V_{dc} - V_{HB}(t)](S_1 - S_3) \quad (1)$$

where V_{dc} is dc link voltage, N is the number of dc side H-bridge cells, V_{cj} is the cell capacitor voltage of the j^{th} cell, and S_1 and S_3 represent the switch states of the two upper switches of the main bridge connected to the load, see Fig. 1. Since the main H-bridge uses switches S_1 and S_4 to synthesize positive half cycle of the output voltage v_a, and S_2 and S_3 to generate the negative half; S_1 and S_4 are the complementary pair of S_2 and S_3. Also, in the series connected H-bridge cells, the switching devices of the same leg, such, as (S_{j1} and S_{j2}) and (S_{j3} and S_{j4}) are complementary pairs.

To generate sinusoidal fundamental output voltage and current waveforms from the hybrid converter with a reduced number of cells as in Fig. 1, high frequency carrier based pulse width modulation (PWM) or selective harmonic elimination with a large number of notches must be used: so sinusoidal pulse width modulation (SPWM) is adopted. To generate the fundamental sinusoidal output voltage, the voltage across dc side cascaded H-bridge cells is modulated according to:

$$V_{HB}^{*}(t) = 1 - m|\sin \omega t| \quad (2)$$

where m and ω represent modulation index and fundamental frequency in rad/s. In this manner, the voltage across dc side cascaded bridge cells which represents the term $\sum_{j=1}^{N} V_{cj}$ in equation (1), can be expressed by:

$$V_{HB}(t) = V_{dc}\left[1 - m|\sin \omega t|\right] \quad (3)$$

This means the dc voltage applied across the dc input of the main H-bridge cell is:

$$V_m(t) = V_{dc} - V_{dc}\left[1 - m|\sin \omega t|\right] = mV_{dc}|\sin \omega t| \quad (4)$$

The dc voltage across the dc input of the main bridge is a rectified form of the desired output voltage. Thus the main bridge needs to operate only at the fundamental frequency, following the modulating signal $v_a^{*}(t) = m\sin \omega t$ in order to synthesize both positive and negative halves of the output voltage $v_a(t)$. On this basis converter, the output voltage can be expressed as:

$$v_a(t) = V_m(t) \times \text{sign}(v_a^{*}) = V_{dc}|m\sin \omega t| \times \text{sign}(v_a^{*}) = mV_{dc}\sin \omega t \quad (5)$$

In order words, the main bridge operates every negative half cycle to flip the input dc rectified voltage to produce the negative half of the output voltage. A phase disposition (PD) carrier arrangement is adopted because it minimizes the number of switching transitions per carrier period, compared to the phase shifted (PS) carriers for the same carrier frequency and produces centred aligned pulses (improved harmonic performance at reduced switching frequency per device). A two-cell version of the hybrid cascaded converter requires two PD carriers arranged in a contiguous band between 1 and 0 as shown in Fig. 1(b). The DC side cascaded H-bridge cells generate voltage level $V_{HB}(t)=V_{dc}$ when the modulating signal $V_{HB}^{*}(t)$ is greater than the upper carrier, and voltage level $V_{HB}(t)=0$ when its less than lower carrier. Otherwise, the cells generate voltage level $V_{HB}(t)=½V_{dc}$.

Capacitor voltage balancing is achieved by rotating the cell capacitor every sampling period depending on the polarity of the limb current I_d, and voltage magnitude of each individual cell. For this two-cell version of the hybrid cascaded converter in Fig. 1(a), assume current direction shown is the positive, the cell capacitor with a minimum voltage is selected to charge when $I_d>0$, while that with a maximum voltage is selected to discharge, and the opposite is true when $I_d<0$. But the exact number of cell capacitors to be selected in each sampling period is determined by the voltage level to be synthesized, according to modulation function of the H-bridge cells $V_{HB}^{*}(t)$.

Table 1summarises the number of cell capacitors to be selected at each voltage level, and the charging and discharging behaviour of each individual cell for a given limb current I_d polarity. A voltage band of 10% of $½V_{dc}$ is imposed on the cell capacitor voltages to prevent extreme discharge or overcharge at voltage levels $\pm V_{dc}$. Within these voltage extremes, switch state (i) is used to bypasses all the cell capacitors is used (the capacitor voltages of both cells are within the band), otherwise switch states (ii) or (iii) that exploit bipolar capability of the H-bridge cell are used to prevent voltage deviation outside the pre-defined voltage-band $\pm V_{dc}$.

Fig. 1(c) shows the three-phase version of the generic hybrid cascaded multilevel converter with N dc side cascaded H-bridge cells per limb. When the number of H-bridge cells is sufficiently high, high frequency pulse width modulation can be replaced by amplitude (staircase) modulation as shown in Fig. 1(c). The three-phase version of the hybrid cascaded converter in Fig. 1(c) requires a three-phase line frequency transformer with isolated windings at the converter side. Additionally, the dc side cascaded H-bridge cells of each limb must be able to block the full dc link voltage in order to be able to generate the fundamental output voltage of $v_a=mV_{dc}\sin\omega t$. This means that the hybrid converter can generate the same fundamental output voltage as the MMC ($v_a=½mV_{dc}\sin\omega t$), but with half the dc link voltage of the MMC, where the switching devices and cell capacitors in both converters have the same voltage stresses and equivalent current stresses. Furthermore, it generates the same voltage levels per phase as the MMC but with half the number of cells. Moreover, the hybrid cascaded converter is inherently dc short-circuit proof, where this feature is activated by inhibiting the gating signals to the converter switches, as the H-bridge cell capacitors will oppose any current flow; thus there is no current in converter switches and no power exchange between the converter ac and dc sides. However, the issues related to short circuit proof feature is out of scope of this paper. With a lossless power conversion assumption in both the dc side cascaded H-bridge cells and main bridge power stages, the power balanced equation assumes the ac side active power equals the dc power, so:

$$V_{dc}\bar{I}_d = \tfrac{1}{2}I_m V_p \cos\varphi \Rightarrow \bar{I}_d = \tfrac{1}{2}mI_m \cos\varphi \quad (6)$$

where the modulation index of the H-bridge converter is defined as $m = V_p / V_{dc}$ (not $m = V_p / \frac{1}{2}V_{dc}$ as for half-bridge based topologies), $\bar{I}_d$ represents the mean dc current, I_m is the peak of the fundamental output current 'i_a' and V_p is the peak phase load voltage.

Table 1: Summary of switch states of the hybrid converter with two dc side H-bridge cells and their influence on the cell capacitor state of charge (↑, ↓ and → indicate charging, discharging and unchanged respectively)

Voltage levels	Main bridge switch states	H-bridge cells switch states	$I_d>0$	$I_d<0$
V_{dc}	S_1=1 and S_3=0	i. S_{11}=S_{13}=1 and S_{21}=S_{23}=1	C_1→ and C_2→	C_1→ and C_2→
		ii. S_{11}=1, S_{13}=0 and S_{21}=0, S_{23}=1	C_1↓ and C_2↑	C_1↑and C_2↓
		iii. S_{11}=0, S_{13}=1 and S_{21}=1, S_{23}=0	C_1↑ and C_2↓	C_1↓ and C_2↑
$½V_{dc}$	S_1=1 and S_3=0	iv. S_{11}=0, S_{13}=1 and S_{21}=S_{23}=1	C_1↑ and C_2→	C_1↓ and C_2→
		v. S_{11}=S_{13}=1 and S_{21}=0, S_{23}=1	C_1→ and C_2↑	C_1→ and C_2↓
0	S_1=1 and S_3=0 or S_1=0 and S_3=1	vi. S_{11}=0, S_{13}=1 and S_{21}=0, S_{23}=1	C_1↑ and C_2↑	C_1↓ and C_2↓
$-½V_{dc}$	S_1=0 and S_3=1	vii. S_{11}=0, S_{13}=1 and S_{21}=S_{23}=1	C_1↑ and C_2→	C_1↓ and C_2→
		viii. S_{11}=S_{13}=1 and S_{21}=0, S_{23}=1	C_1→ and C_2↑	C_1→ and C_2↓
$-V_{dc}$	S_1=0 and S_3=1	ix. S_{11}=S_{13}=1 and S_{21}=S_{23}=1	C_1→ and C_2→	C_1→ and C_2→
		x. S_{11}=1, S_{13}=0 and S_{21}=0, S_{23}=1	C_1↓ and C_2↑	C_1↑and C_2↓
		xi. S_{11}=0, S_{13}=1 and S_{21}=1, S_{23}=0	C_1↑ and C_2↓	C_1↓ and C_2↑

In the time interval, $0 \le \omega t \le \pi$, the instantaneous dc current in the converter limb can be approximated by:

$$I_d(t) = i_a(t) = I_m \sin(\omega t + \varphi) \quad (7)$$

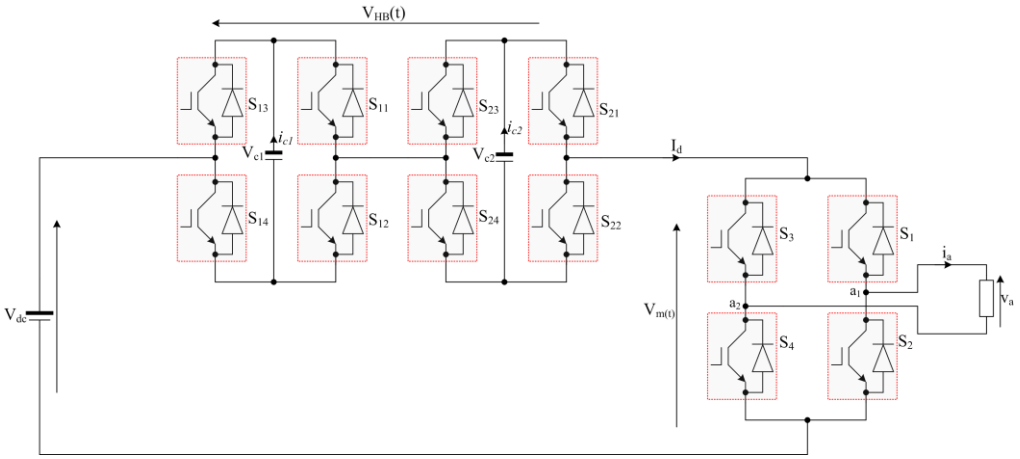
The instantaneous power flow through the dc side cascaded H-bridges is:

$$\begin{aligned} p_{HB}(t) &= v_{HB}(t) \times I_d(t) \\ &= V_{dc}(1 - m\sin\omega t) \times I_m \sin(\omega t + \varphi) \\ &= -\tfrac{1}{2} m I_m V_{dc} \cos\varphi + m V_{dc} I_m \sin(\omega t + \varphi) + \tfrac{1}{2} m V_{dc} I_m \cos(2\omega t + \varphi) \end{aligned} \quad (8)$$

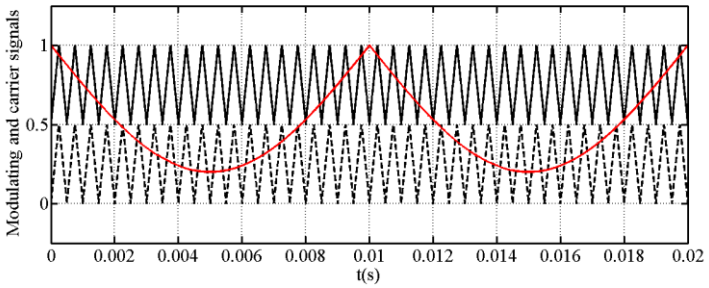
In equation (8), the(8) first term indicates that the dc power balances the ac power flow as in the MMC. Therefore, the capacitor voltage balancing must exploit the bipolar capabilities of the H-bridge cells in order to force the average power that the dc side cascaded H-bridge cells exchange with the ac side, to zero. This is necessary to maintain voltage balancing of the H-bridge cell capacitors. Assuming that the capacitors of the two-cell version of the hybrid converter in Fig. 1(a) are uniformly utilized over one or multiple half fundamental periods, the continuous equivalent current through each cell capacitor can be approximated using the concept of local average over one sampling period:

$$\begin{aligned} I_c(t) &= \tfrac{1}{2}(1 - m\sin\omega t) \times I_d(t) \\ &= -\tfrac{1}{4} m I_m \cos\varphi + \tfrac{1}{2} I_m \sin(\omega t + \varphi) + \tfrac{1}{4} m I_m \cos(2\omega t + \varphi) \\ &= -\tfrac{1}{2} \bar{I}_d + \tfrac{1}{2} I_m \sin(\omega t + \varphi) + \tfrac{1}{4} m I_m \cos(2\omega t + \varphi) \end{aligned} \quad (9)$$

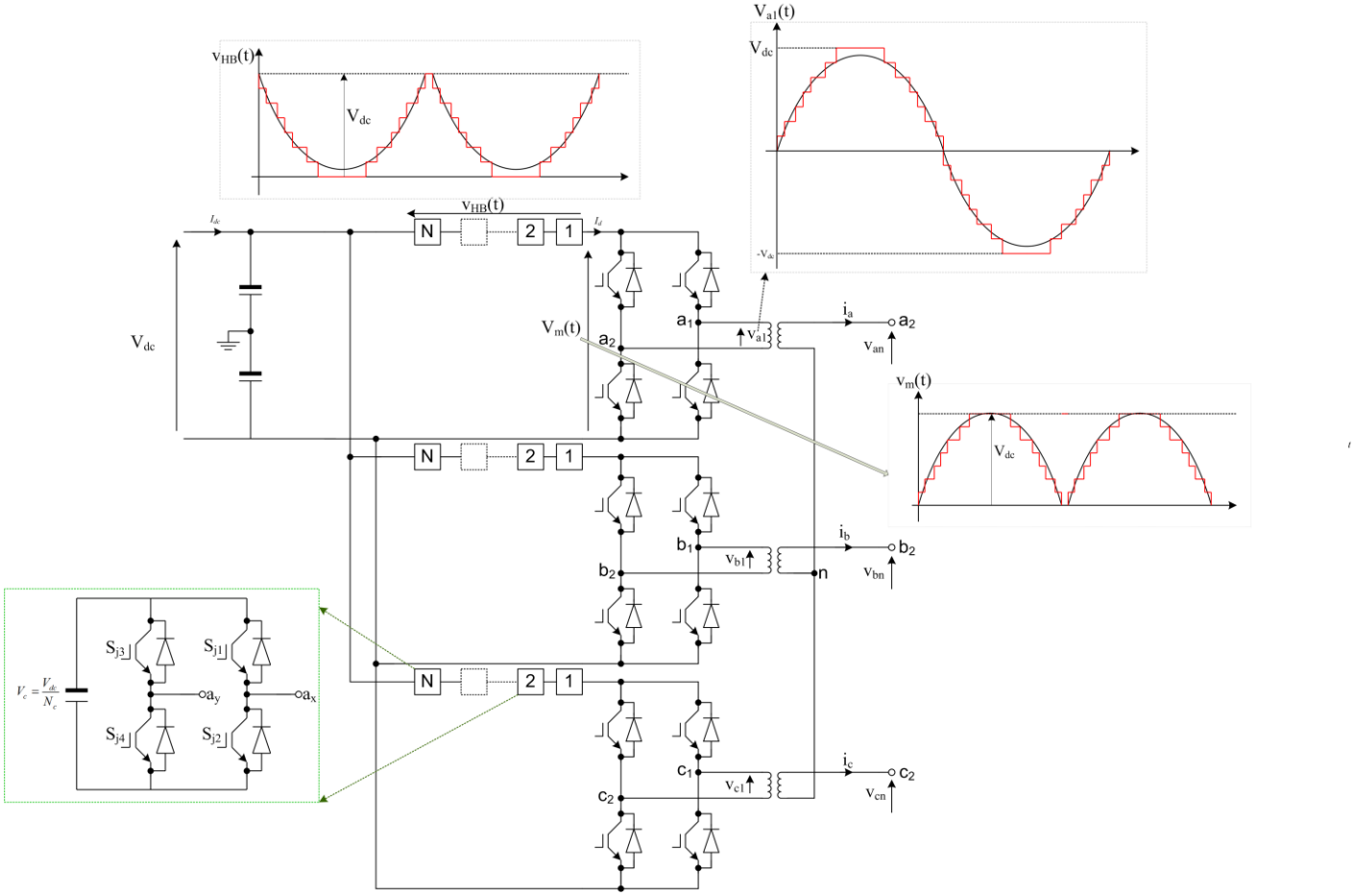
This approximation of the cell capacitor instantaneous continuous current in (9) confirms the previous interpretation of the equation (8), and confirms that the H-bridge cells of this hybrid cascaded cannot be replaced by the half-bridge cells as in the MMC case.



(a) Illustrative two-cell version of the hybrid cascaded converter with dc side H-bridge cells



(b) Phase dispossition carriers and H-bridge cells modulation signal



(c) Generic version of the hybrid cascaded converter with dc side H-bridge cells

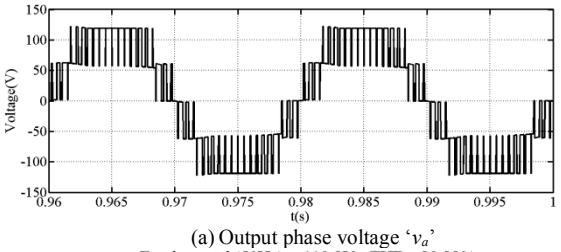
Fig. 1: Hybrid cascaded multilevel converter with dc side H-bridge cells

III. SIMULATIONS

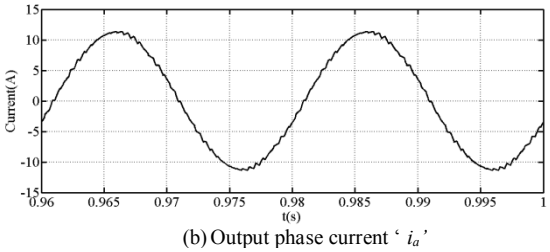
This section presents simulation results when a single-phase hybrid converter with two H-bridge cells per limb is operated from a 120V supply. The simulation parameters are: V_{dc}=120V, cell capacitance C=2.2mF, and the converter is controlled using SPWM with a 2kH carrier frequency.

Fig. 2 shows simulation results when the converter operates with a modulation index m=1, and supplies a passive load of 10Ω resistance and 10mH inductance, which is equivalent to 0.95 power factor lagging at 50Hz. Fig. 2 (a) and (c) show that the two-cell version of the hybrid cascaded converter generates a phase voltage with five voltage levels, with relatively low total harmonic distortion (THD) and low *dv/dt* voltage stresses on ac side equipment. The output voltage spectrum in Fig. 2 (c) shows the harmonics distribution is similar to a typical multilevel converter such as the MMC when controlled with SPWM. Fig. 2 (b) shows hybrid converter produces good quality sinusoidal output current. Fig. 2 (d) and (e) display voltage waveforms across the dc side cascaded H-bridge cells and at the dc input of the main bridge when PWM is used. They are complementary as explained section II , with their sum equal to the full dc link voltage. Fig. 2(f) shows that the hybrid cascaded converter is able to operate in applications with predominantly real power exchange (high power factors), with the voltage balancing of the H-bridge cell capacitors maintained tightly around $½V_{dc}$. Fig. 2 (g) displays the input dc link current of the hybrid converter, where the theoretical I_d is expected to be an image of the output current i_a, as assumed in equation (7);(7) however, the actual input dc link current I_d exhibits some switching. The switching action observed in I_d is due to fluctuation of the cell capacitor voltages around $½V_{dc}$,

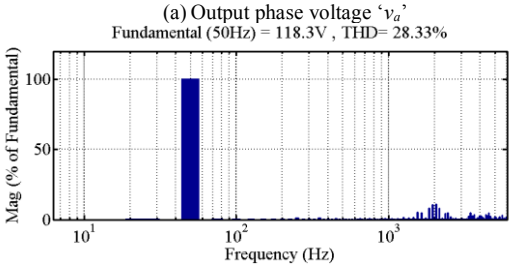
occurring when the hybrid converter synthesizes a '0' voltage level using switch combination (vi) V_{dc}-V_{c1}-V_{c2} inTable 1, and the commutation instances of the main bridge at zero voltage but not necessarily zero current. Positive current pulses are created when V_{dc}-V_{c1}-$V_{c2}>0$ and negative current pulse when V_{dc}-V_{c1}-$V_{c2}<0$. The current pulse magnitudes are limited by the load impedance, provided the main-bridge two upper or lower switches are not simultaneously on during the '0' voltage at its input $V_m(t)=0$. This phenomena of I_d tending to be a switched current disappears when a large number of cells are used with staircase modulation, as the '0' voltage level can be treated as an instant, not an extended period as in the case of the illustrative two-cell hybrid converter being considered here.



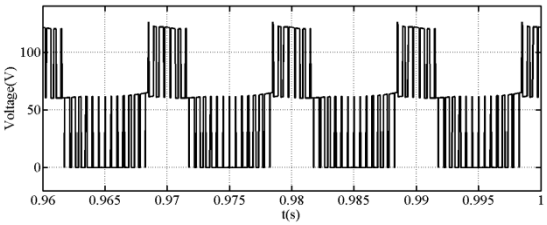
(a) Output phase voltage 'v_a'



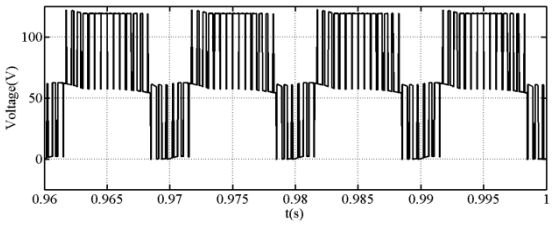
(b) Output phase current 'i_a'



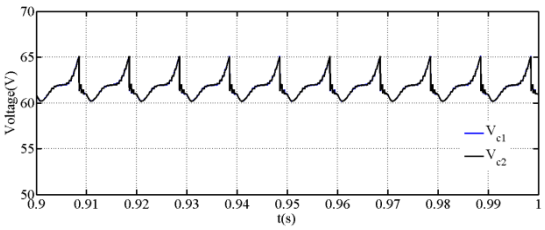
(c) spectrum of the normalized phase voltage to peak fundamental voltage



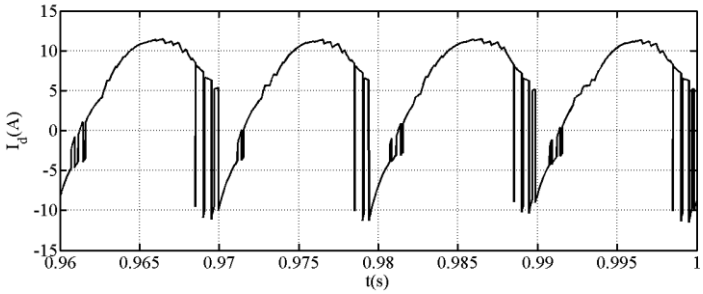
(d) Voltage waveforms across H-bridge cascaded cells, '$V_{HB}(t)$'



(e) Voltage waveforms across dc input of the main bridge 'V_m'



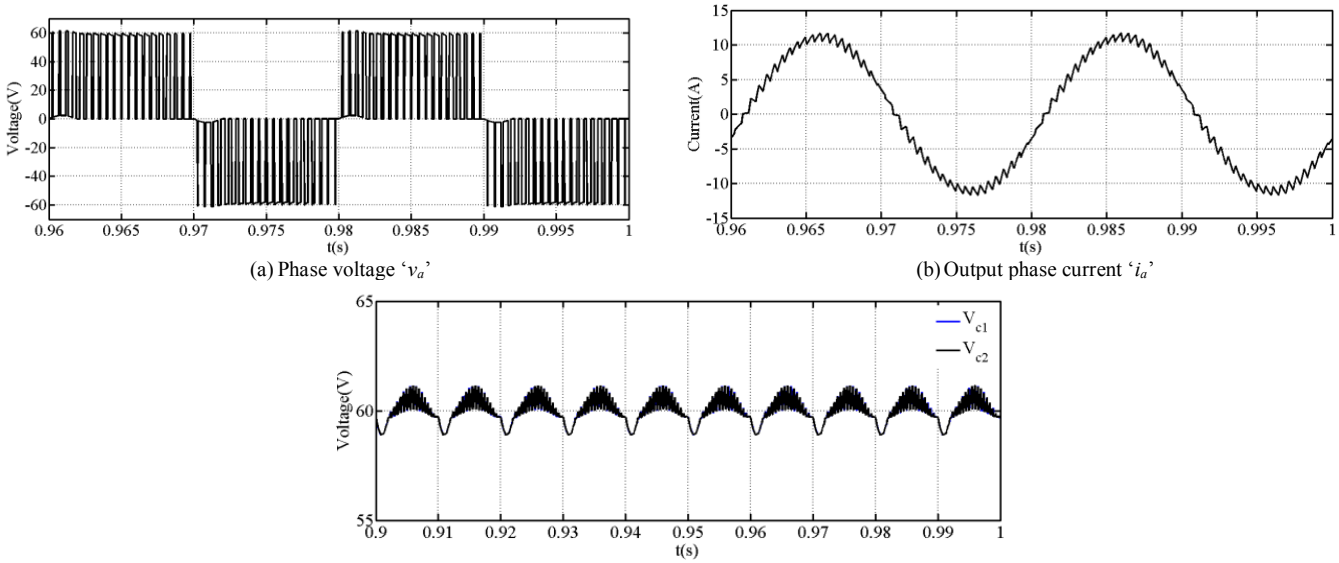
(f) Voltage across H-bridge cell capacitors



(g) Input dc link current (I_d)

Fig. 2: Waveforms obtained when hybrid cascaded inverter operates with unity modulation index and 0.95 power factor. (V_{dc}=120V, C=2.2mF and a 2kHz switching frequency)

To illustrate the suitability of the hybrid cascaded for applications that require the converter terminal voltage to be varied, such as in HVDC applications, the modulation index is reduced to 0.4, and the load is reduced to 40% to maintain the load current near constant. The waveforms in Fig. 3 show that the hybrid converter is able to operate at reduced modulation, while exchanging power with the ac at near unity power factor. Additionally, at a low modulation index such as 0.4, the hybrid cascaded converter continues to present relatively high quality voltage and current waveforms to the load, with its H-bridge cell capacitor voltages maintained balanced, Fig. 3(a), (b) and (c).



(a) Phase voltage 'v_a'

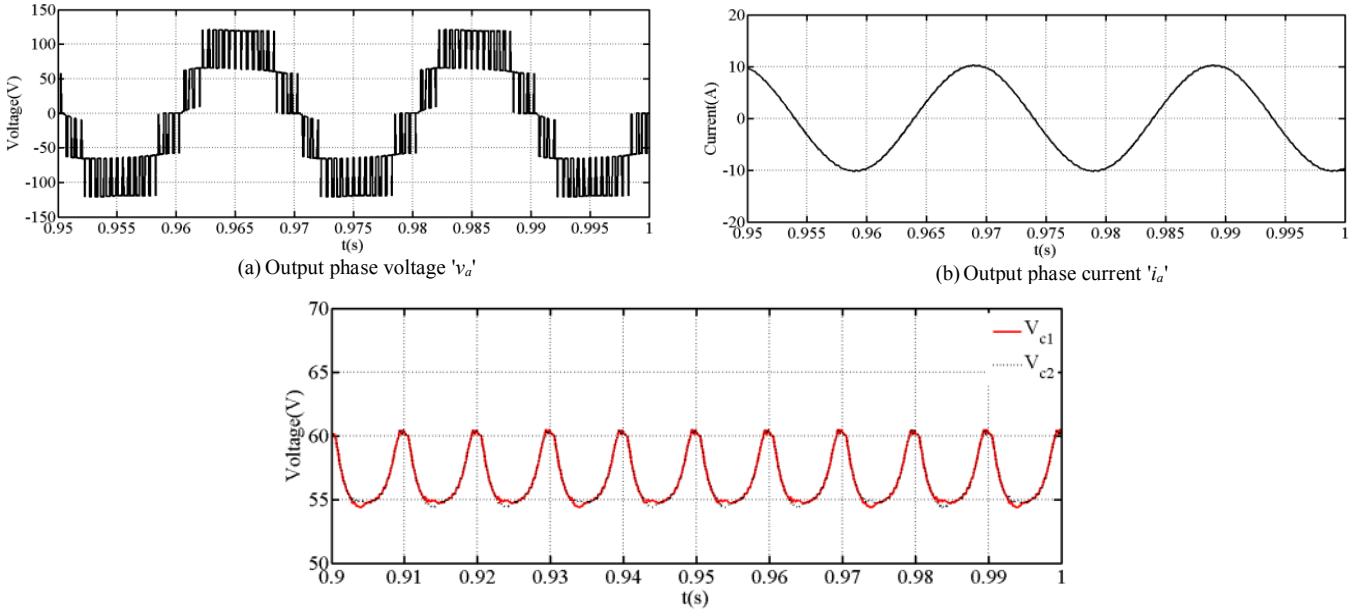
(b) Output phase current 'i_a'

(c) Voltage across H-bridge cells

Fig. 3: Waveforms illustrate hybrid cascaded converter operation at reduced modulation indices while delivering real power. (V_{dc}=120V, C=2.2mF, 2kHz switching frequency, and a load 4Ω and 4mH)

To demonstrate the hybrid cascaded multilevel converters reactive power capability, the load power factor is reduced to 0.37 lagging (R=4Ω and L=31.8mH) when the modulation index is m=0.9. The system is able to operate successfully with voltage stresses across switching devices controlled since voltage balancing of the H-bridge cell capacitors is maintained. However, at low power factor where phase angle between the phase current and voltage approaches ½π, the cell capacitor energy storage requirements increase to those of the MMC. This means larger cell capacitance is needed in reactive power applications.

Additional case is presented in Fig. 5 that illustrates operation of the hybrid converter at zero power lagging and unity modulation index (typical operation of static synchronous series and shunt compensators, SSSC and STATCOM). The output phase voltage and current, capacitor voltages and main bridge dc input current show output waveform quality and cell capacitor voltage balancing are maintained as in the previous cases. However, the input dc current to the main bridge I_d exhibits less switching despite large cell capacitor voltage ripple as previously mentioned.

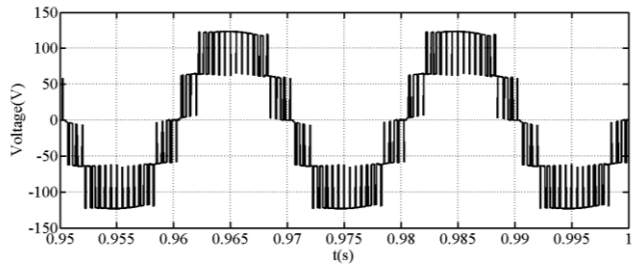


(a) Output phase voltage 'v_a'

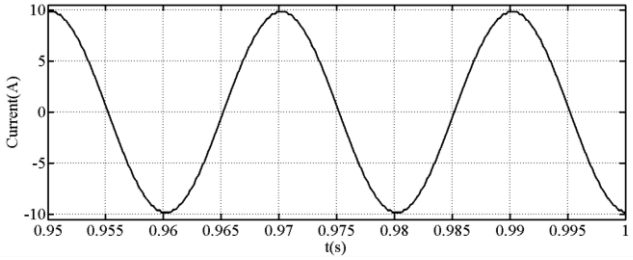
(b) Output phase current 'i_a'

(c) Voltage across H-bridge cell capacitors

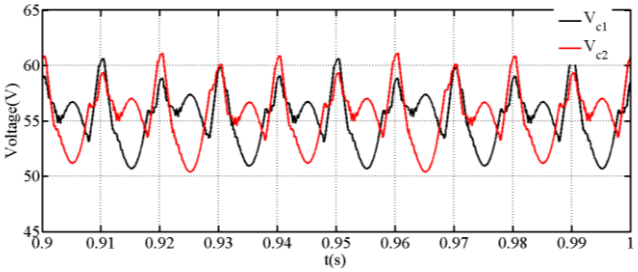
Fig. 4: Waveforms illustrative operation of the hybrid cascaded converter at low power factor . (V_{dc}=120V, C=2.2mF, 2kHz switching frequency, and load 4Ω and 31.8mH)



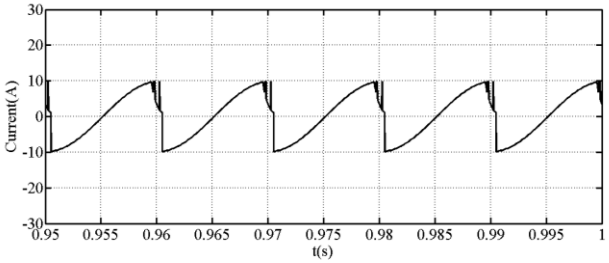
(a) Output phase voltage 'v_a'



(b) Output phase current 'i_a'



(c) Voltage across H-bridge cell capacitors



(d) Main bridge dc input current 'I_d'

Fig. 5: Waveforms illustrative operation of the hybrid cascaded converter at zero power factor lagging and unity modulation index. (V_{dc}=120V, C=2.2mF, 2kHz switching frequency, and load 0.05Ω and 39.8mH)

IV. EXPERIMENTAL VALIDATION

This section presents experimental results for the prototype two-cell hybrid cascaded converter being considered in this paper. Modulation and capacitor voltage balancing is implemented in a 32-bit microcontroller Cypress CY8CKIT-050 PSoC® 5LP. A 2kHz switching frequency and 2.2mF H-bridge cell capacitance are used. Fig. 7(a) illustrates the PSoC microcontroller implementation of the hybrid cascaded converter modulation and capacitor voltage balancing. Fig. 7(b) presents block diagram that illustrates generic implementation of the hybrid converter modulation and capacitor voltage balancing. Fig. 8 shows experimental results obtained when the prototype hybrid converter operates at unity modulation index, and supplies a passive load of 13Ω resistance and 5mH, which is equivalent to a 0.99 power factor lagging. Fig. 8(a), (b), and (c) show the output voltage and its spectrum, and output current waveform The two-cell version of the hybrid cascaded converter with dc side H-bridge cells produces high quality output voltage and current waveforms, with low *dv/dt*. Fig. 8(d) shows the two H-bridge cell capacitor voltages remain balanced and settled around $½V_{dc}$ when the converter operates at unity modulation index and a power factor approaching unity (applications with predominantly real power exchange). Fig. 8(e) shows a sample of the voltage waveform across dc side cascaded H-bridge (upper plot), and voltage across the dc input of the main bridge that is connected to the load (lower plot). The two voltage waveforms are complementary as described in theoretical discussion and obtained in the simulations in sections II and I.

Fig. 9 demonstrates that the hybrid converter is able to operate in applications with dominantly reactive power exchange The experimental waveforms are obtained when the hybrid cascaded converter is connected to the passive load of 4Ω and 35mH, which corresponds to a 0.34 load power factor lagging. The converter is able to operate satisfactory, and produces high quality output voltage and current waveforms, with balanced H-bridge cell capacitor voltages.

Fig. 10 presents experimental results when the converter is operated at a low modulation index (m=0.6) to demonstrate its ability to operate in variable voltage applications that require modulation index to be varied over a wide range. The converter is connected to 22Ω and 10mH load, which corresponds to a 0.99 power factor, lagging. The hybrid cascaded converter operates successfully, with balanced H-bridge cell capacitor voltages, and relatively good quality output voltage and current waveforms, as seen in Fig. 10(a), (b) and (c).

Based on the simulation and experimental results presented in sections I and 0 it can be concluded that the hybrid cascaded converter with dc side cascaded H-bridge cells can operate over the entire power factor and modulation index linear range, without cell capacitor voltage balancing problems. This means it can be employed for both real and reactive power applications such as motor drives, dc transmission systems, and as a static synchronous compensator.

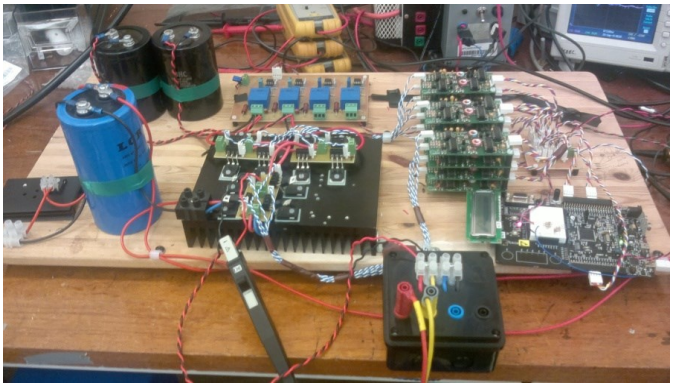
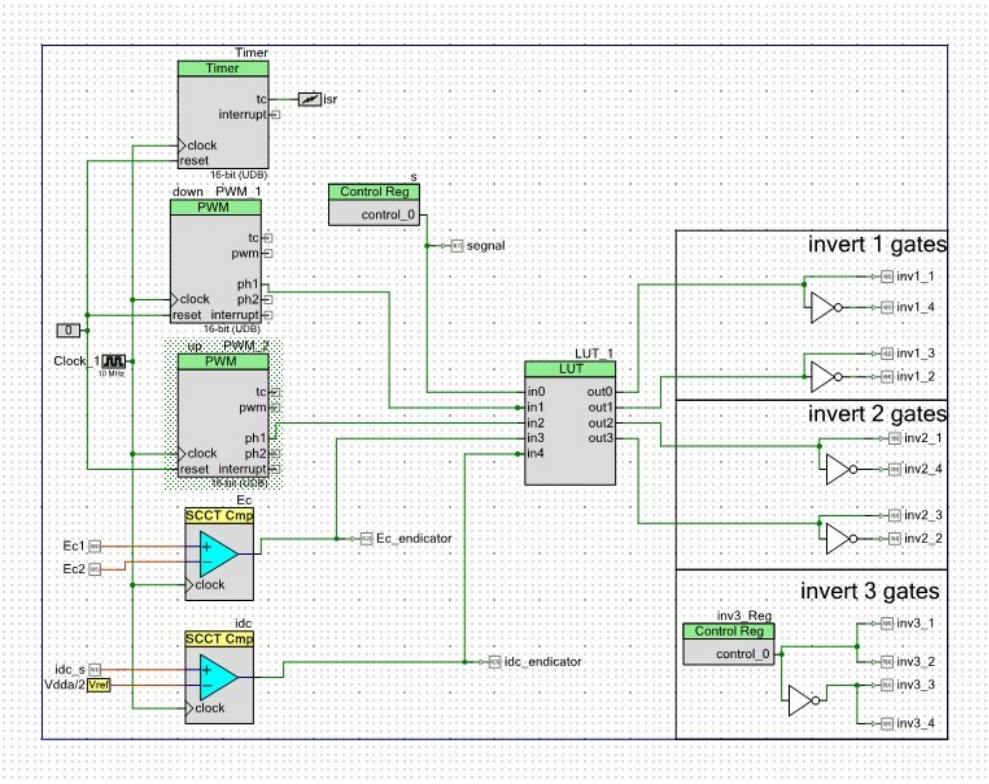
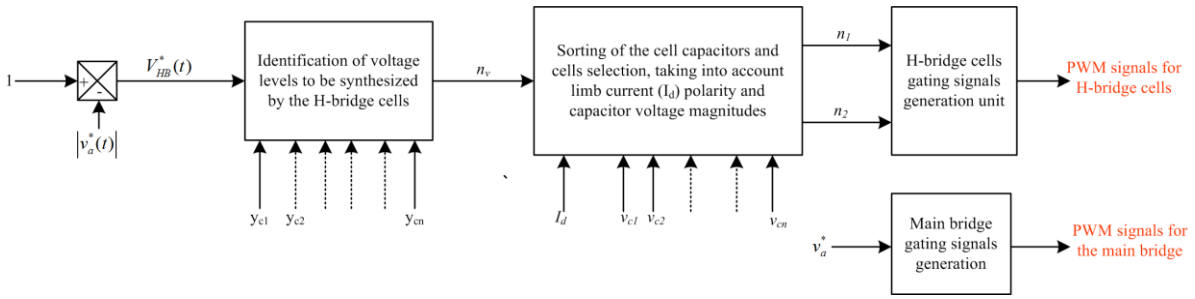


Fig. 6: Prototype of single-phase hybrid cascaded converter with two H-bridge cells per limb

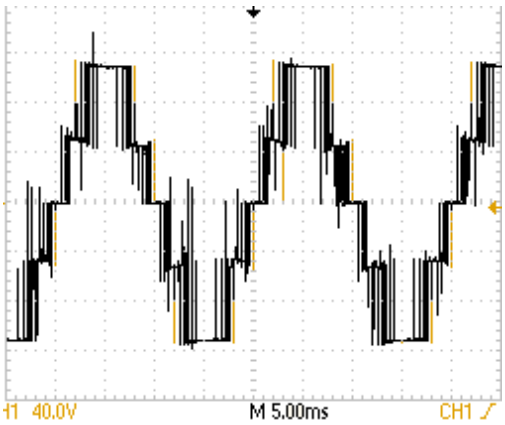


(a)

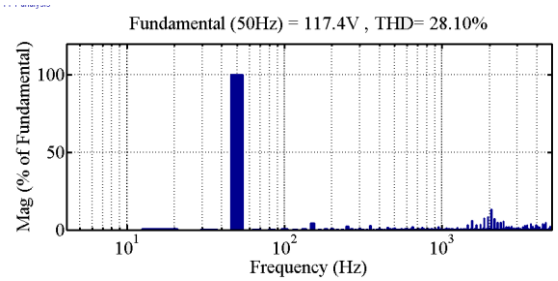


(b)

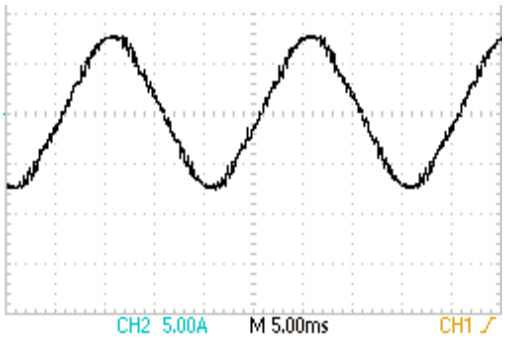
Fig. 7: (a) Diagram showing implementation of the modulation and capacitor voltage balancing in PSoC 5.0., and (b) generic implementation of the hybrid converter modulation and capacitor voltage balancing (n_v is the voltage level to be synthesis, and n_1 and n_2 are two vectors used to identify the cell capacitors to be bypassed from that to be inserted in the power path to synthesize the desired voltage levels)



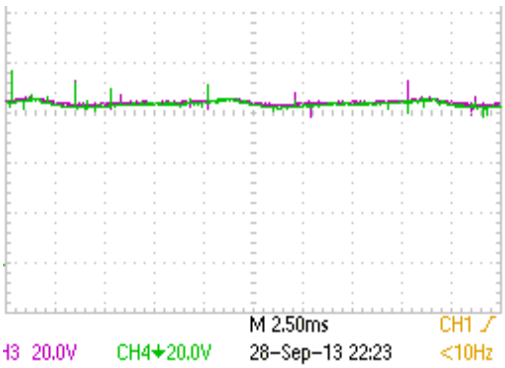
(a) Output phase voltage 'v_a' (x-axis:5ms/Div, y-axis:40V/Div)



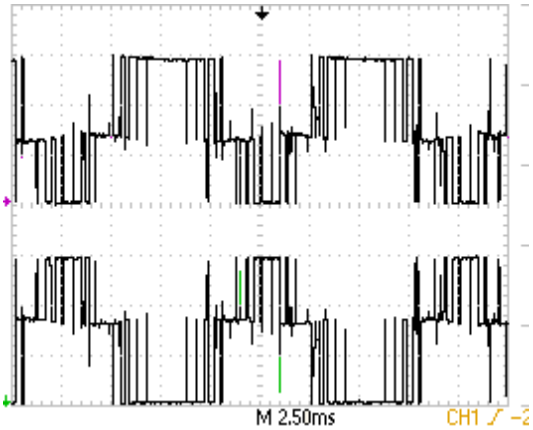
(b) Spectrum of the output voltage



(c) Output phase current (x-axis:5ms/Div, y-axis:5A/Div)

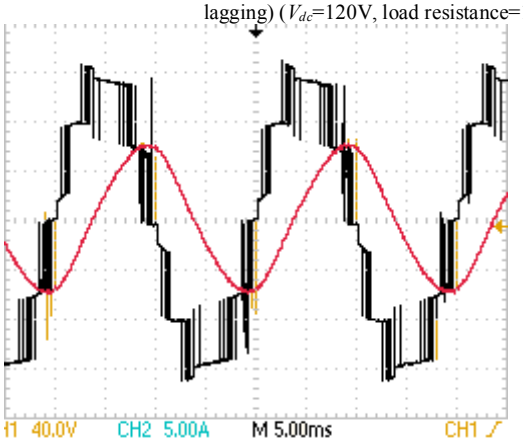


(d) Voltage across H-bridge cell capacitors (x-axis:2.5ms/Div, y-axis:20V/Div)

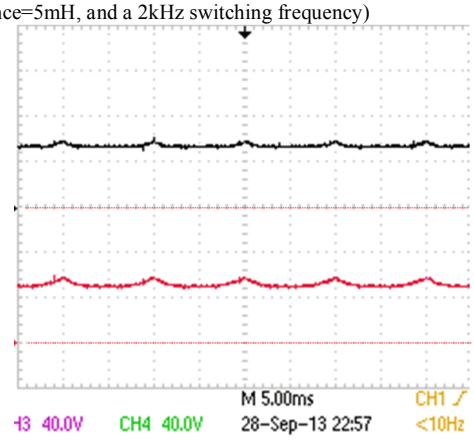


(e) Upper and lower plots represent voltage waveforms across dc side cascaded H-bridge cells, and at the dc input of the main H-bridge connected to the load (x-axis:2.5ms/Div, y-axis:40V/Div)

Fig. 8: Waveforms when prototype of two-cell version of hybrid converter operates with unity modulation index and power factor approaching unit (0.992 lagging) (V_{dc}=120V, load resistance=13Ω and inductance=5mH, and a 2kHz switching frequency)

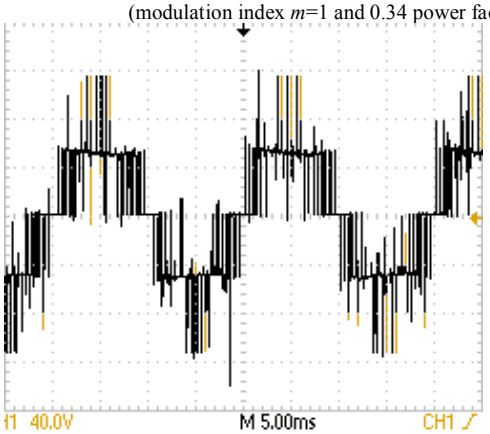


(a) Converter output voltage and current waveforms (x-axis:5ms/Div, y-axis:40V/Div for voltage and 5A/Div for current)

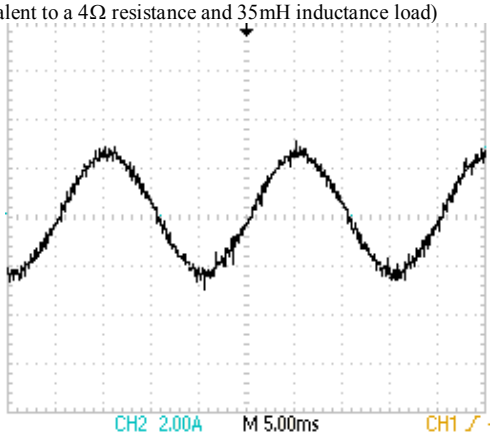


(b) Voltages across the H-bridge cell capacitors (x-axis:5ms/Div, y-axis:40V/Div)

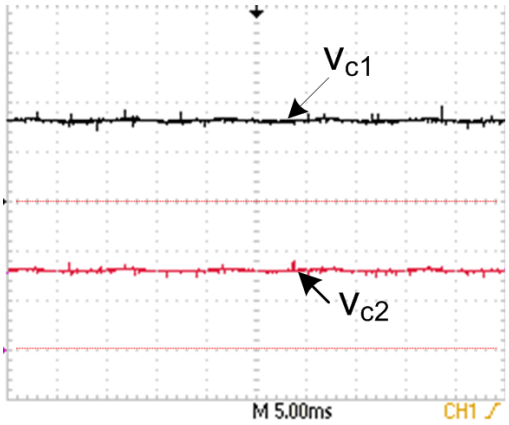
Fig. 9: Waveforms illustrate operation of hybrid converter in a predominantly reactive power application. (modulation index m=1 and 0.34 power factor lagging, equivalent to a 4Ω resistance and 35mH inductance load)



(a) Output voltage (x-axis:5ms/Div, y-axis:40V/Div)



(b) Output current (x-axis:5ms/Div, y-axis:2A/Div)



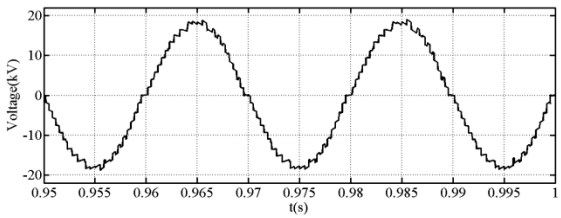
(c) Voltages across the H-bridge cell capacitors (x-axis:5ms/Div, y-axis:40V/Div)

Fig. 10: Waveforms illustrate operation of hybrid converter at reduced modulation index. (m=0.6 and 0.99 power factor lagging, a load of 22Ω resistance and 10mH inductance)

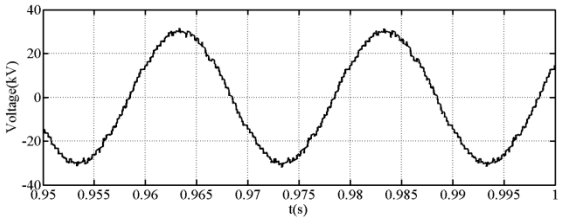
V. SCALABILITY OF THE HYBRID CASCADED MULTILEVEL CONVERTER

The previous sections have confirmed the applicability of the hybrid cascaded converter in a wide range of applications. This section demonstrates its scalability to high-voltage applications where a large number of H-bridge cells per limb is necessary to permit the use of 3.3/4.5/6.5kV low-voltage rated switching devices. This demonstration uses a three-phase hybrid cascaded converter rated at 20MVA with a 20kV dc link, supplying a passive load of 20Ω resistance and 15Ω inductive reactance, through a 50Hz 13.8kV/24kV interfacing transformer, at 0.9 modulation index. The low-voltage (13.8kV) represents the phase voltage of the interfacing transformer winding that is connected to each main H-bridge stage, while the high-voltage (24kV) represents the line voltage across the load. The simulated hybrid cascaded converter has 11 cells per limb, which means each capacitor and switching device within the H-bridge cells blocks 1.82kV approximately. The cell capacitance within each H-bridge cell is 4mF, and the interfacing transformer is rated at 20MVA with 20% leakage reactance. The hybrid cascaded converter is controlled using amplitude (or staircase) modulation with a sinusoidal reference.

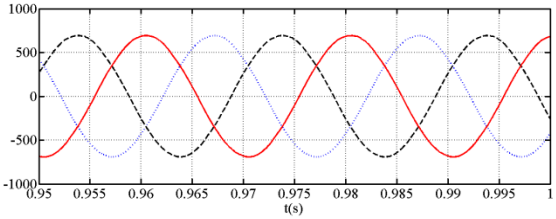
Simulation results are displayed in Fig. 11, where with a relatively large number of cells per limb, hybrid cascaded converter produces high quality three-phase output voltage and currents with extremely low THD and *dv/dt* (Fig. 11(a), (b) and (c)). Additionally, the voltage across dc side cascaded H-bridge cells and that across the dc input of the main bridge connected to interfacing transformer in Fig. 11(d) and (e) are in line with the theoretical waveforms depicted in Fig. 1(c) in section II. Fig. 11(f) shows that the voltages across converter cell capacitors remain tightly balanced around the desired settle point of $\frac{1}{11}\times 20\text{kV} \approx 1.82\text{kV}$. These results have shown that the hybrid converter being investigated in this paper has potential for high voltage applications.



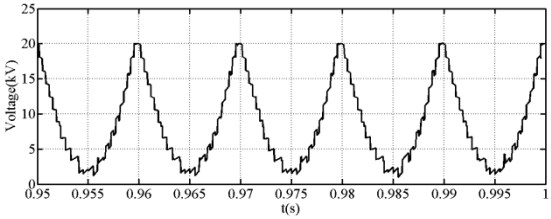
(a) Sample of phase voltage converter presents to interfacing transformer (v_{a1})



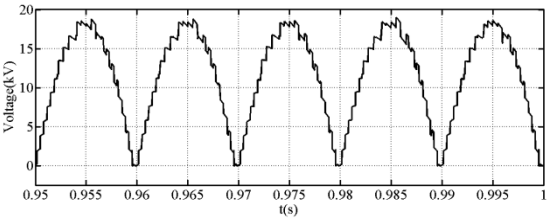
(b) Sample of line-to-line voltage across the load



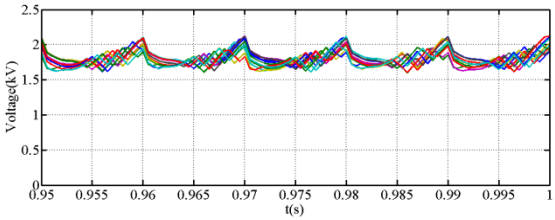
(c) Three-phase output currents



(d) Voltage waveform across dc side cascaded H-bridge cells



(e) Voltage waveform at dc input of the main H-bridge connected to interfacing transformer of phase '*a*'



(f) Voltages across the H-bridge cell capacitors

Fig. 11: Waveforms demonstrating the scalability of the hybrid cascaded multilevel converter with dc side cascaded H-bridge cells, to high voltage applications.

Table **2** compares hybrid converter being discussed and some of the recently proposed multilevel converters. Based on Table **2** no single converter provides all the desirable features (DC short circuit proof at reduced semiconductor losses, small footprint, and applicable to long and short distance transmission line). The converter topologies are referenced to converter 'A' , where N and V_{dc} are number of cells and dc link voltage.

Table 2: high level comparison between hybrid cascaded with dc side full-bridge cells which designated as (A), 'B' stands for H-bridge alternative arm MMC **[42]**, 'C' for hybrid cascaded with ac side cascaded full-bride cells **[42]**, 'D' for mixed cells MMC (50% full-bridge plus 50% half-bridge cells)**[47]**, 'E' for three-level MMC cells **[47]**, and 'F' for five-level cross connected cells **[47]**

	A	B	C	D	E	F
Input dc voltage in (kV)	V_{dc}	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$
Number of cell capacitors per phase	N	$2N$	N	$4N$	$4N$	$4N$
Voltage stress per device	V_{dc}/N	V_{dc}/N	V_{dc}/N	V_{dc}/N	V_{dc}/N	V_{dc}/N
Rated dc link current	I_{dc}	$½I_{dc}$	$½I_{dc}$	$½I_{dc}$	$½I_{dc}$	$½I_{dc}$
Number switches in conduction path	$4N$	$3N$	$4N$	$6N$	$6N$	$6N$
Semiconductor losses per phase	(Moderate	low	moderate	high	high	high
Applications	Back-to-back or short distance HVDC link	Back-to-back, short and long distance HVDC link	Back-to-back, short and long distance HVDC link	Back-to-back, short and long distance HVDC link	Back-to-back, short and long distance HVDC link	Back-to-back, short and long distance HVDC link

VI. CONCLUSIONS

This paper presented the basic operational principle, modulation and capacitor voltage balancing of an emerging hybrid cascaded multilevel converter with dc side cascaded H-bridge cells. Simulations and experimentation were used to confirm the practicality of the hybrid cascaded converter, including its scalability to high-voltage applications. It has been shown that the hybrid cascaded converter with dc side cascaded H-bridge cells can operate over the entire P-Q envelope normally required for HVDC converters, without capacitor voltage balancing problems, and with voltage stresses on the converter switches evenly distributed. The main H-bridge converter that is connected to the load or interfacing transformer operates at fundamental frequency, while the effective switching frequency per device within the dc side cascaded H-bridge cells are low (in order of 150Hz or lower) when a large number of cells is used. Thus, low H-bridge switching loss is expected.

VII. REFERENCES

[1] S. Debnath and M. Saeedifard, "A New Hybrid Modular Multilevel Converter for Grid Connection of Large Wind Turbines," *Sustainable Energy, IEEE Transactions on,* vol. PP, pp. 1-14, 2013.

[2] L. Mihalache and X. Yaosuo, "A new three-phase hybrid five-level inverter with reduced number of high-frequency switching devices," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, 2011, pp. 3720-3727.

[3] Z. Shuai, *et al.*, "New control method of injection-type hybrid active power filter," *Power Electronics, IET,* vol. 4, pp. 1051-1057, 2011.

[4] L. Yen-Shin, *et al.*, "New Hybrid Pulsewidth Modulation Technique to Reduce Current Distortion and Extend Current Reconstruction Range for a Three-Phase Inverter Using Only DC-link Sensor," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 1331-1337, 2013.

[5] C. Xia, *et al.*, "Integrating Wind Farm to the Grid Using Hybrid Multiterminal HVDC Technology," *Industry Applications, IEEE Transactions on,* vol. 47, pp. 965-972, 2011.

[6] M. P. Aguirre, *et al.*, "Multilevel Current-Source Inverter With FPGA Control," *Industrial Electronics, IEEE Transactions on,* vol. 60, pp. 3-10, 2013.

[7] L. Angquist, *et al.*, "Open-Loop Control of Modular Multilevel Converters Using Estimation of Stored Energy," *Industry Applications, IEEE Transactions on,* vol. 47, pp. 2516-2524, 2011.

[8] P. Acuna, *et al.*, "Improved Active Power Filter Performance for Renewable Power Generation Systems," *Power Electronics, IEEE Transactions on,* vol. PP, pp. 1-1, 2013.

[9] M. Zhang, *et al.*, "Circulating Harmonic Current Elimination of a CPS-PWM Based Modular Multilevel Converter with Plug-In Repetitive Controller," *Power Electronics, IEEE Transactions on,* vol. PP, pp. 1-1, 2013.

[10] Y. Zhang, *et al.*, "Hybrid Multilevel Converter: Capacitor Voltage Balancing Limits and its Extension," *Industrial Informatics, IEEE Transactions on,* vol. PP, pp. 1-1, 2012.

[11] L. Zixin, *et al.*, "An Inner Current Suppressing Method for Modular Multilevel Converters," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 4873-4879, 2013.

[12] A. Lopez, *et al.*, "Analysis and Comparison of Three Topologies of the Ladder Multilevel DC/DC Converter," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 3119-3127, 2012.

[13] C. Wai-Hei, *et al.*, "Analysis of DC-Link Voltage Controls in Three-Phase Four-Wire Hybrid Active Power Filters," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 2180-2191, 2013.

[14] B. Gultekin and M. Ermis, "Cascaded Multilevel Converter-Based Transmission STATCOM: System Design Methodology and Development of a 12 kV ±12 MVAr Power Stage," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 4930-4950, 2013.

[15] X. Dawei, *et al.*, "Condition Monitoring Power Module Solder Fatigue Using Inverter Harmonic Identification," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 235-247, 2012.

[16] G. Congzhe, *et al.*, "A DC-Link Voltage Self-Balance Method for a Diode-Clamped Modular Multilevel Converter With Minimum Number of Voltage Sensors," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 2125-2139, 2013.

[17] F. Krismer and J. W. Kolar, "Closed Form Solution for Minimum Conduction Loss Modulation of DAB Converters," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 174-188, 2012.

[18] D. Peftitsis, *et al.*, "High-Power Modular Multilevel Converters With SiC JFETs," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 28-36, 2012.

[19] L. Angquist, *et al.*, "Inner control of Modular Multilevel Converters - An approach using open-loop estimation of stored energy," in *Power Electronics Conference (IPEC), 2010 International*, 2010, pp. 1579-1585.

[20] A. Antonopoulos, *et al.*, "Global Asymptotic Stability of Modular Multilevel Converters," *Industrial Electronics, IEEE Transactions on,* vol. PP, pp. 1-1, 2013.

[21] A. Antonopoulos, *et al.*, "On interaction between internal converter dynamics and current control of high-performance high-power AC motor drives with modular multilevel converters," in *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, 2010, pp. 4293-4298.

[22] K. Ilves, *et al.*, "A New Modulation Method for the Modular Multilevel Converter Allowing Fundamental Switching Frequency," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 3482-3494, 2012.

[23] K. Ilves, *et al.*, "Steady-State Analysis of Interaction Between Harmonic Components of Arm and Line Quantities of Modular Multilevel Converters," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 57-68, 2012.

[24] F. Deng and Z. Chen, "A Control Method for Voltage Balancing in Modular Multilevel Converters," *Power Electronics, IEEE Transactions on,* vol. PP, pp. 1-1, 2013.

[25] C. Dong, *et al.*, "Optimal Design of a Multilevel Modular Capacitor-Clamped DC–DC Converter," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 3816-3826, 2013.

[26] S. Jianjiang, *et al.*, "Research on Voltage and Power Balance Control for Cascaded Modular Solid-State Transformer," *Power Electronics, IEEE Transactions on,* vol. 26, pp. 1154-1166, 2011.

[27] D. Ludois and G. Venkataramanan, "Simplified Dynamics of a Modular Multilevel Converter Based on a Terminal Behavioral Model," *Power Electronics, IEEE Transactions on,* vol. PP, pp. 1-1, 2013.

[28] S. Qiang, *et al.*, "A Steady-State Analysis Method for a Modular Multilevel Converter," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 3702-3713, 2013.

[29] M. K. Alam and F. H. Khan, "A high-efficiency modular switched-capacitor converter with continuously variable conversion ratio," in *Control and Modeling for Power Electronics (COMPEL), 2012 IEEE 13th Workshop on*, 2012, pp. 1-5.

[30] E. Amankwah, *et al.*, "Experimental validation of a parallel hybrid modular multilevel voltage source converter for HVDC transmission," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, 2013, pp. 1607-1614.

[31] E. K. Amankwah, *et al.*, "Cell capacitor voltage control in a parallel hybrid modular multilevel voltage source converter for HVDC applications," in *Power Electronics, Machines and Drives (PEMD 2012), 6th IET International Conference on*, 2012, pp. 1-6.

[32] A. Antonopoulos, *et al.*, "On dynamics and voltage control of the Modular Multilevel Converter," in *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on*, 2009, pp. 1-10.

[33] C. D. Barker and N. M. Kirby, "Reactive power loading of components within a modular multi-level HVDC VSC converter," in *Electrical Power and Energy Conference (EPEC), 2011 IEEE*, 2011, pp. 86-90.

[34] H. Barnklau, *et al.*, "Derivation of an equivalent submodule per arm for modular multilevel converters," in *Power Electronics and Motion Control Conference (EPE/PEMC), 2012 15th International*, 2012, pp. LS2a.2-1-LS2a.2-5.

[35] G. P. Adam, *et al.*, "Modular multilevel inverter: Pulse width modulation and capacitor balancing technique," *Power Electronics, IET,* vol. 3, pp. 702-715, 2010.

[36] Y. Zhang, *et al.*, "Analysis of modular multilevel converter capacitor voltage balancing based on phase voltage redundant states," *Power Electronics, IET,* vol. 5, pp. 726-738, 2012.

[37] M. K. Alam and F. H. Khan, "EFFICIENCY CHARACTERIZATION AND IMPEDANCE MODELING OF A MULTILEVEL SWITCHED CAPACITOR CONVERTER USING PULSE DROPPING SWITCHING SCHEME," *Power Electronics, IEEE Transactions on,* vol. PP, pp. 1-1, 2013.

[38] G. Minyuan and X. Zheng, "Modeling and Control of a Modular Multilevel Converter-Based HVDC System Under Unbalanced Grid Conditions," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 4858-4867, 2012.

[39] G. P. Adam, *et al.*, "Transient capability assessments of HVDC voltage source converters," in *Power and Energy Conference at Illinois (PECI), 2012 IEEE*, 2012, pp. 1-8.

[40] Y. Zhang, *et al.*, "Improved pulse-width modulation and capacitor voltage-balancing strategy for a scalable hybrid cascaded multilevel converter," *Power Electronics, IET,* vol. 6, 2013.

[41] G. P. Adam, *et al.*, "New Breed of Network Fault-Tolerant Voltage-Source-Converter HVDC Transmission System," *Power Systems, IEEE Transactions on,* vol. 28, pp. 335-346, 2013.

[42] G. P. Adam, *et al.*, "Hybrid converter with ac side cascaded H-bridge cells against H-bridge alternative arm modular multilevel converter: steady-state and dynamic performance," *Generation, Transmission & Distribution, IET,* vol. 7, 2013.

[43] G. P. Adam, *et al.*, "Network Fault Tolerant Voltage-Source-Converters for High-Voltage Applications," in *IET, the 9th International conference on AC and DC Power Transmission*, London, UK, 2010.

[44] M. M. C. Merlin, *et al.*, "A New Hybrid Multi-Level Voltage-Source Converter with DC Fault Blocking Capability," in *IET ACDC2010*, London,UK, 2010.

[45] Lu, *et al.*, "Performance of a DC/AC/DC VSC system to interconnect HVDC systems," in *AC and DC Power Transmission (ACDC 2012), 10th IET International Conference on*, 2012, pp. 1-6.

[46] C. C. DAVIDSON;, *et al.*, "A new hybrid voltage-sourced converter for HVDC power transmission," presented at the Cigre, Paris, 2010.

[47] A. Nami, *et al.*, "Five level cross connected cell for cascaded converters," presented at the European Power Electronics (EPE2013), Lille, France, 2013.

VIII. BIOGRAPHIES

G.P. Adam received a first class BSc and MSc from Sudan University for Science and Technology, Sudan in 1998 and 2002 respectively; and. a PhD in Power Electronics from University of Strathclyde in 2007. He has been working as a research fellow with Institute of Energy and Environment, University of Strathclyde in Glasgow, UK, since 2008. His research interests are fault tolerant voltage source converters for HVDC systems; control of HVDC transmission systems and multi-terminal HVDC networks; voltage source converter based FACTS devices; and grid integration issues of renewable energies. Dr Adam has authored and co-authored several technical reports, and journal and conference papers in the area of multilevel converters and HVDC systems, and grid integration of renewable power. Also, he is actively contributing to reviewing process for several IEEE and IET Transactions and Journals, and conferences.

Ibrahim Abdelsalam received a first class B.Sc. and M.Sc. degrees in electrical engineering from the Arab Academy for Science and Technology and Maritime Transport, Egypt, in 2006(Alexandria campus) and 2009(Cairo campus), respectively. He is currently pursuing his Ph D. degree in the area of wind energy conversions and power electronics at University of Strathclyde, Glasgow, U.K. Since 2006 Mr Abdelsalam was a teaching assistant in Electrical Power and Control Department, Arab Academy for Science and Technology, Alexandria. His research interests are power electronic converters and their applications in wind energy conversion systems, and advanced control strategies of the multilevel voltage and current source converters.

Khaled H. Ahmed received the B.Sc. (first class honours) and M.Sc. degrees from the Faculty of Engineering, Alexandria University, Egypt in 2002 and 2004, respectively. He received the Ph.D. degree in electrical engineering from the Electrical Department, Strathclyde University, Glasgow, UK, 2008. Since 2009, he has been a Lecturer at the Alexandria University, Alexandria, Egypt. He has authored or co-authored more than 39 technical papers in refereed journals and conferences. Dr. Khaled is a reviewer for the IEEE Transactions and several conferences. His research interests are digital control of power electronic systems, power quality, micro-grids, distributed generation, DC/DC converters, and HVDC.

B.W. Williams received the M.Eng.Sc. degree from the University of Adelaide, Australia, in 1978, and the Ph.D. degree from Cambridge University, Cambridge, U.K., in 1980. After seven years as a Lecturer at Imperial College, University of London, U.K., he was appointed to a Chair of Electrical Engineering at Heriot-Watt University, Edinburgh, U.K, in 1986. He is currently a Professor at Strathclyde University, UK. His teaching covers power electronics (in which he has a free internet text) and drive systems. His research activities include power semiconductor modelling and protection, converter topologies, soft switching techniques, and application of ASICs and microprocessors