Protection challenges in future converter dominated power systems

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Abstract —Converter interfaces, used to connect renewable energy sources, HVDC links and infeeds to the power system, will bring significant changes to the behaviour of power systems in the future, particularly in Great Britain (GB). Existing network protection schemes (both at transmission and distribution levels) may be seriously affected by the changed system behaviour during and after faults. Therefore it is necessary to establish how and when the protection schemes may start to malfunction under future scenarios in a "converter-dominated" environment.

In this paper, a Voltage Source Converter (VSC) model, with an appropriate and flexible controller, which is capable of regulating output voltages and currents in response to faults on the supplied AC power system, will be introduced. A set of tests of protection performance in a power system with varying degrees of converter penetration and fault responses are presented, and the results of tests are presented and analysed. In the tests presented, adjustments to the converter controller parameter are made, resulting in a range of converter outputs during faults (e.g. with different reaction delays and current magnitudes). The potential impact that these responses may have on protection performance are outlined, and on-going and future work to fully evaluate the performance of transmission protection under a range of future system scenarios are described.

Index Terms—converters; dual sequence control; inertia; non-synchronous sources; power system protection; VSC-HVDC.

I. INTRODUCTION

According to National Grid's "2014 UK Future Scenarios" document [1], the amount of renewable energy sources and HVDC transmission systems connected to the GB system will increase markedly in the near future. The development of converter technologies has greatly facilitated the grid integration of renewable energy source as well as enabling HVDC transmission networks to be introduced to global power systems. As stated in the future scenarios document, the usage of renewable energy could reach 15% in 2020 and 34% by 2030 in GB. The potential challenges that may be presented to power system protection by such high penetration levels of RES must be investigated to anticipate and respond in advance to any problems that may be encountered.

As the fault response of converters is directly influenced by the control strategies adopted in the converter, there is, at present, no universally accepted fixed form of a converter output under fault conditions. The European "Network Code on Requirements for Grid Connection applicable to all Generators" [2] published by ENTSO-E in 2014 and the UK "Grid Code" published by National Grid [3], have stated that generating units (regardless of interfacing technology) should be capable of providing "fast" symmetrical fault current during a symmetrical network fault, and if required, produce asymmetrical currents during asymmetrical fault conditions. However, the fault response from the converter units are still not specified in detail and many aspects of required performance during disturbances is left to be agreed at a national level between system operators and those connecting converter-interfaced sources and HVDC links to the transmission and distribution systems.

Therefore, it is necessary to introduce a flexible and credible converter-interfaced generation/infeed model that is capable of reproducing a range of voltage and current waveforms during network faults. Together with appropriate protection relay models and real injection to protective relays, tests shall be performed to analyse how a range of protection systems may be affected in the future.

II. Converter Characteristics

A. Fault Response

During a fault, traditional synchronous machines provide a current with a magnitude that is typically several times of their rated output currents - therefore protection systems can easily detect the fault and act to isolate the faulted network components. However, VSC-interfaced sources are incapable of providing high levels of fault current as this could potentially damage the semiconductor components in the VSC's IGBT switches, and therefore the VSC output current is limited by its controllers, typically to values of less than 2 pu [4]. The fault current provided by a traditional source is typically 3~6 pu of rated current (and in some cases as high as 10), whereas the fault current provided by a converter may only be in the range of 1~2 pu [4].

As previously stated, a converter's fault response is defined predominantly by its controller, and of course the thermal ratings of components and the capabilities of the source/infeed "behind" the converter. From discussions with several industry colleagues and from [5], a converter may not be capable of outputting required maximum current following an AC voltage collapse for a period of anything up to 60ms from fault inception [5]. This is due to delays associated with measuring, detecting, verifying and responding to the fault conditions. A comprehensive model that can represent such fault response characteristics in a flexible and configurable fashion is introduced later in this paper.

B. Grid Code Requirements

In April 2014 ENTSO-E (the European Network of Transmission System Operators for Electricity) prepared a draft network Code on HVDC Connections and DC-connected Power Park Modules [6] and submitted this to ACER (the Agency for Cooperation of Energy Regulators). ACER recommended the adoption of the codes for the second quarter of 2015. In the latest published version it is required that:

- *"The Relevant Network Operator in coordination with the Relevant TSO shall have the right to require the capability of a HVDC System to provide Fast Fault Current at a Connection Point in case of symmetrical (3-phase) faults.*

- *The Relevant Network Operator in coordination with the Relevant TSO shall specify the characteristics of the voltage deviation and the characteristics, timing and accuracy of the fault current.*

- *With regard to the supply of Fast Fault Current in case of asymmetrical (1-phase or 2-phase) faults the Relevant Network Operator in coordination the Relevant TSO shall have the right to introduce a requirement for asymmetrical current injection.*

- *The Relevant TSO shall define a Voltage-against-time-profile, having regard to the voltage-against-time-profile defined for Power Park Modules according to [NC RfG].This profile shall apply at the Connection Point(s) for fault conditions, under which the HVDC Converter Station shall be capable of staying connected to the Network and continuing stable operation after the power system has recovered following fault clearance.*

- *The Relevant Network Operator shall define and make publicly available the method and the pre-fault and post-fault conditions for the calculation of at least the minimum and maximum short circuit power at the Connection Point(s).*

- *The HVDC System shall be capable of operating within the range of short circuit power and Network characteristics defined by the Relevant Network Operator.*

- *The Relevant Network Operator shall define, in coordination with the Relevant TSO, the schemes and settings necessary to taking into account protect the Network the characteristics of the HVDC System"*

It is interesting to note from the above that while terms such as "fast fault current" and "timing and accuracy" of fault current and other aspects are mentioned, it remains up to the individual system operators to agree the exact quantification of terms such as "fast" with connecting parties (and

converter manufacturers). Therefore, uncertainty remains and the performance of protection under a range of possible converter responses in future scenarios must be investigated. The GB grid code documentation [3] states that under close-up three phase faults and imbalanced earth fault conditions, all generating units (including DC converters) must remain connected without any tripping for a period of 140 ms. It also states that *"during the period of the fault…(all generation) shall generate maximum reactive current without exceeding the transient rating limit…"*, however, the term "maximum" is not defined and again this introduces a degree of uncertainty, so a model that can be configured to output varying magnitudes of sustained fault current must be developed and used.

It is clear from the foregoing discussion that there is clearly a desire for converters to produce fast-rising, high-magnitude and sustainable current injections in response to AC system short circuits – for both balanced and unbalanced faults. However the requirements are somewhat non-specific in many instances, with no detailed specification of the required reaction speed, means of detection, or fault current magnitude when the converter is required to output fault current.

III.   SYSTEM DESIGN

A.   VSC-HVDC control system layout

Fig. 1 demonstrates how the VSC system used in this paper is arranged. A phase-locked loop (PLL) connected to the connection point(CP)is used to track the AC voltage's angular speed in a timely fashion as input to the Park and Inverse Park transformations which underpin the VSC control scheme. The control system consists of inner and outer controllers. The inner current controller aims to compute VSC output voltage references in order to regulate the VSC output currents. For the outer controllers, the VSC output current control can be transformed into other forms for regulating P, Q, V_{DC} or V_{AC}, and flexible combinations for the outer controllers can be selected to achieve various objectives. Detailed operating principles for such controllers can be found in [7].
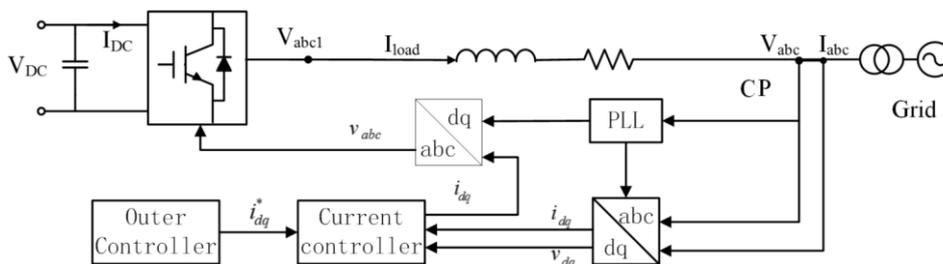

Fig. 1. Overall layout of the VSC system

In this system, a dual sequence control scheme is implemented as this permits the VSC to output both balanced and unbalanced three phase currents, facilitates stable, non-oscillating real and reactive power control and outputs, and minimises DC link voltage ripples during unbalanced network conditions [7].   The scheme can also enable the response of the converter to be similar to a synchronous generator, albeit with a lesser relative magnitude of fault current, during unbalanced fault conditions [8], which obviously is desirable in terms of complying with various grid code requirements.

B.   Fault detection, ride through and fault response

To provide performance that complies with grid codes, the outer controller should act to regulate the inner current control loop to output the maximum current during faults. An embedded fault detection logic function has been developed to initiate automatic fault response from the model. This is achieved by monitoring the positive and negative sequence voltage at the connection point – the thresholds for fault detection are configurable. The detection logic is as shown in the figure below:
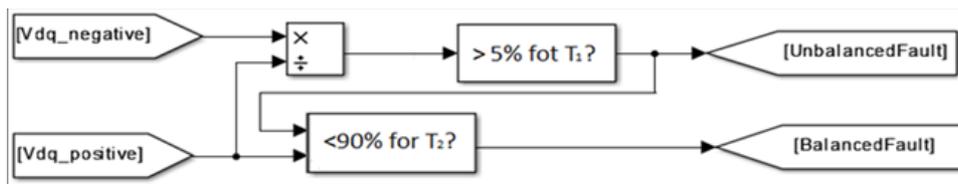

Fig. 2. Fault detection logic (T_1: required time for balanced fault detection; T_2: required time for unbalanced fault detection)

For a close-up fault, which will result in a severe voltage depression at the converter's AC terminals, the PLL unit may not be capable of determining phase and frequency information as the voltage measurement inputs to the PLL drop to near-zero values. Consequently, the converter may not be able to correctly inject current into the grid and the controller may shut down. In order to ride through such fault conditions, the fault detection function is essential. When a fault is detected, the PLL unit will retrieve phase and frequency information recorded from the historical data immediately before the fault in order to sustain the current injection into the grid. Although this may mean that it will not follow the true system frequency or inject the correct current phase angle relative to the voltage during the fault, it will mimic the converter's AC voltage waveforms under assumed steady state conditions and sustain continuous AC current injection to the system in order to facilitate grid fault ride-through.

After a fault is detected, the converter will begin to respond to the fault. The precise nature of the response can be varied according to the fault type and the nature of the fault. This is governed by the logic depicted in Fig.3:
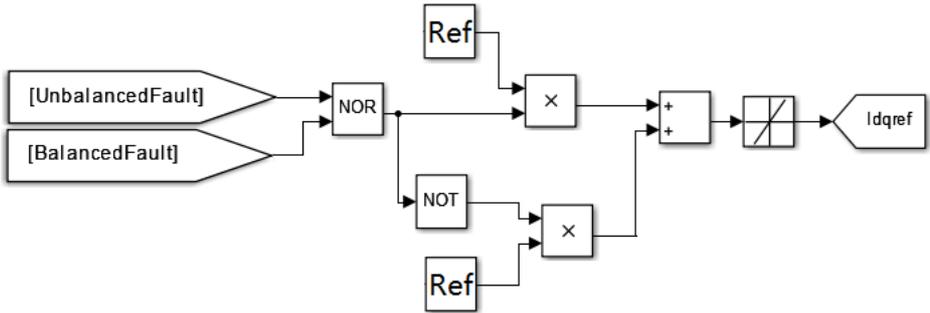

Fig. 3. Fault response logic（Ref: the reference value for the converter's inner control loop）

The fault response (including the initiation delay; the ramp rate/time and the final sustained magnitude of fault current) can be readily manipulated using the above model and configuration facilities. In a practical system, the capability of the energy source/system "behind" the VSC would also need to be considered to ensure that it is capable of supplying the required current during the fault and the that disturbances to the DC system (or other AC systems) on the source side of the converter would not be adversely affected by the faults on the supplied AC system.

C. Power system layout and fault level selection

In this paper, a simple two-bus system has been modelled for analysis of behaviour. A converter and a synchronous machine are connected to a transmission line which is modelled using actual system data as shown below.
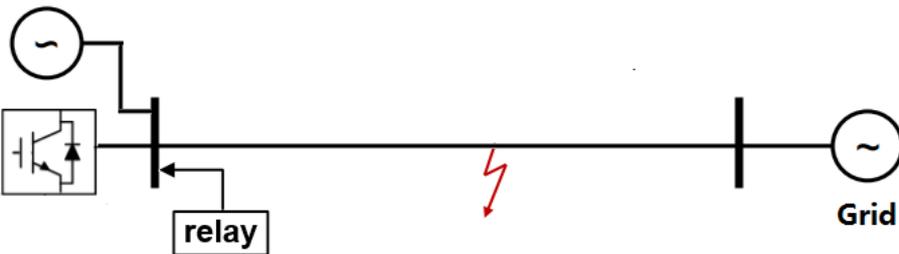

Fig. 4. Model of a transmission line supplied by a combination of synchronous/converter-interfaced sources.

According to National Grid's Electricity Ten Year Statement 2014 [9], a typical power flow on a specific transmission circuit is 1900MVA, with a three-phase fault level at the sending end of 21 GVA (30.77 kA per phase for a three phase fault) in 2014. In 2024, the power flow for this particular circuit drops to 1166 MVA with a slightly reduced fault level of 20 GVA (29.55 kA). However, according to National Grid's System Operability Framework[10], fault levels are anticipated to drop by anything up to 40%~55% between 2014 and 2024 under the "gone green" scenario. Therefore it is necessary to

define how the fault level may drop, but also to consider this fault current provision in the context of an increased penetration of converter-interfaced sources.

Since the fault level at the sending end bus is effectively supplied by "all" generation and infeeds that are connected to that bus (in relative contributions defined by their relative distances from the fault and their capacities and capabilities), every supply connected to the bus can be simplified and combined into one source that is capable of providing fault current during fault. Assumptions shall be made to define how much fault current can be provided during the fault. A single synchronous machine can typically supply around three-six times its rated current during faults [4], therefore it is reasonable to consider that the system in the 2014 state is a 3.4 GVA source, operating at part loading, capable of providing 21 GVA of apparent power during a fault (noting from earlier discussions that the system supplies approximately 2 GVA via the transmission line during normal operation but 21 GVA during fault).

In future scenarios with converter-interfaced sources, when modelling all converter-interfaced sources connected to the sending end bus as a single source, the capacity of the single converter-interfaced source may be selected to be 1-2.5 times the nominal power transfer rating of the line to provide an accurate representation of the many aggregated converters in an actual external system. This modelling approach requires further refinement and validation in the future, but is suitable for the purposes of the initial studies reported in this paper.

IV. SIMULATION RESULTS AND DISCUSSION

A. *Case study 1: impact of varying converter-interfaced source penetration levels*

In this case the setting of the converter fault response is fixed. The maximum fault current the converter can supply is of course variable, but to reflect multiple converters operating at part-loading in an actual system, it is selected to be 2.2 pu, with the pu value based on the proportion of power being supplied by the converter prior to the fault, i.e. the effective penetration level – at 50% penetration, the converter sources are assumed to be supplying 50% of the load being transferred through the transmission line.

The synchronous source is also set, in a similar fashion, to provide a fault current in relation to the penetration level being studied. The converter fault detection delay in this case is set to 1ms. This effectively ensures an instantaneous response, but later in the paper the impact of varying this delay is studied. The converter's output current ramp rate is set to 0.00112pu/ms – again the impact of varying this is also presented later.

To illustrate this, consider the following example. Firstly, when the penetration level of the converter sources is 0%, the fault level is selected to be 20.85 GVA as per National Grid data. When the penetration level of the converter source is set to 50% with an "assumed" fault level of 20.85 GVA but with 50% converter penetration, the fault level provided by the synchronous machine will be

$$20.85 \cdot 0.5 = 10.425 \text{GVA}.$$

The fault level provided by the converter infeed is set to be:

$$1.166(\text{the nominal transferred apparent power}) \cdot 0.5 \cdot 2.2 = 1.283 \text{GVA}.$$

Taking both infeeds together, the combined total fault level at the sending end bus is:

$$10.425 + 1.283 = 11.708 \text{GVA}.$$

Using this approach, the total fault level at the sending end bus would be 3.48 GVA and 2.5652GVA under 95% and100% converter penetration levels respectively. This method will be refined and validated as the project progresses

When applying a solid three phase fault at 70% of the line length (e.g. a zone 1 fault from the perspective of a distance protection relay at the source end) under 0%, 50%, 95% and 100% converter penetration level, the corresponding voltage and current wave forms at the converter station sending end station were produced as shown in Fig. 5.

(a) V and I (pu) - 0% converter penetration level

(b) V and I (pu) - 50% converter penetration level

(c) V and I (pu) - 95% converter penetration level

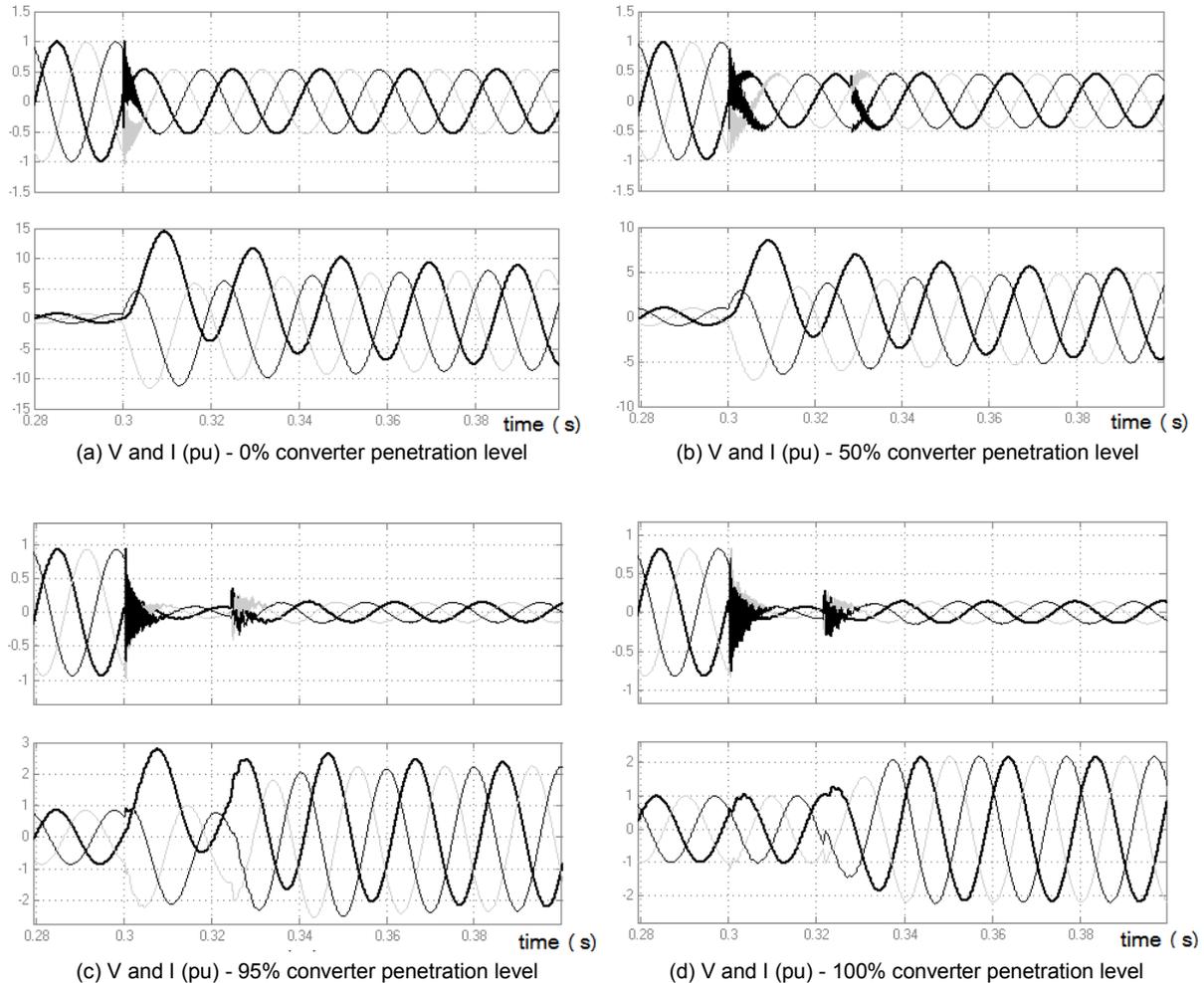(d) V and I (pu) - 100% converter penetration level

Fig. 5. Voltage (top traces) and current (bottom traces) (in pu) as measured at the sending end bus

It can be seen that the fault current magnitudes clearly decrease as expected with the increase of converter source penetration level. The outputs from the primary system simulation are "injected" into a dynamic software model (previously developed at Strathclyde) of a commercially available distance relay [11]. The impedance loci, i.e. the dynamic measurements of impedances with respect to time as viewed internally by the relay, are presented in Fig. 6. The green trace represents the measured impedance over time. It can be seen how it traverses from a large relatively resistive value to the right of the diagrams (equating to pre-fault load impedance) into a position just inside zone 1 (the pink circle on the diagrams). The zone boundaries according to the relay settings (which are from the actual circuit and relay under study) are also shown on the diagrams.
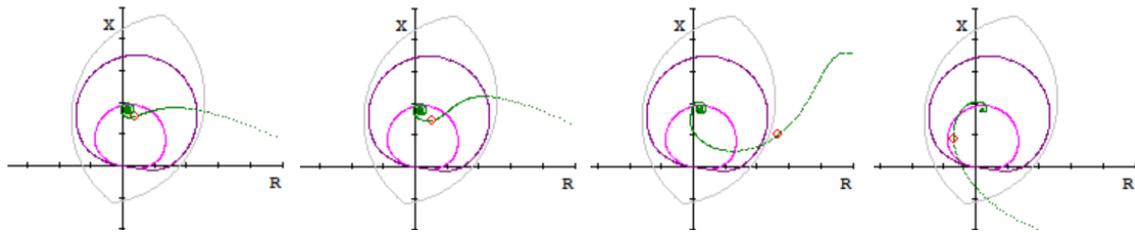
Fig. 6. Impedance loci as measured by the relay (from left to right: 0%, 50%, 95%, 100% penetration levels)

The corresponding tripping times for each of the tests are: 23.5ms; 18.8ms; 23.1ms; 19.5ms. So, in this case, it is clear that relay operated very quickly in every case, which indicates that the zone 1 performance of a traditional distance relay may not be significantly affected by the introduction of converters. However, tests for different levels of fault infeed, different fault types and locations (e.g. unbalanced and remote zone 2 and 3 faults) and to consider operation when converter-interfaced sources are applied at remote line ends to study responses to remote faults and to test back-up protection operation remain to be conducted, as do tests using different types of relays (differential, overcurrent, etc.).

B. Case study 2: impact of varying converter fault detection and response initiation delay

In this case the penetration level of the converter-interfaced source is fixed at 100%, and the delay of the converters' response to the fault is assumed to be 1ms, 5ms, 10ms and 15ms. A solid three phase fault at 70% of the line length is applied and the relay response monitored as previously using a dynamic model of the distance relay. The results are shown in Fig. 7 below.
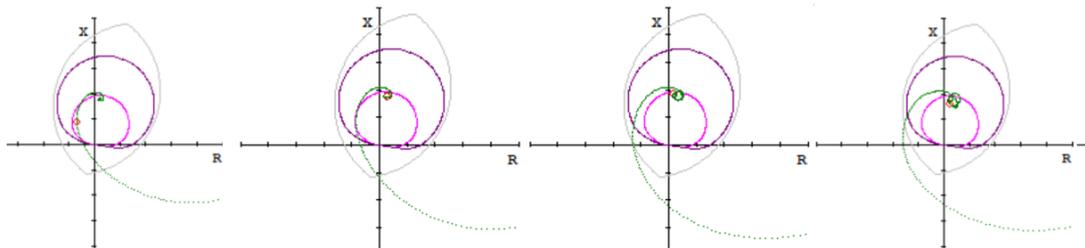

Fig. 7. Impedance loci as measured by the relay (from left to right: 1ms, 5ms, 10ms and 15ms converter initial delay)

The corresponding tripping times are: 19.5ms; 28.0ms; 59.6ms; 41.6ms. It can be seen that the operation of the relays is significantly affected due to the delays in converter response, with a 10ms response delay resulting in approximately 40ms of delay in relay tripping time (assuming the correct response is 20ms). This could have serious consequences for protection and system stability, and further work and more comprehensive testing will be carried out to analyse this in more detail. More results will be reported at the conference.

C. Case study 3: impact of varying converter output current increase ramp rate

In this, the case initiation delay is fixed at 1ms, but the ramp rate of the current is varied with rates of 0.0035 pu/ms, 0.00245 pu/ms, 0.00175 pu/ms and 0.00112 pu/ms. A solid three phase fault at 70% of the line length is applied and the relay response monitored as previously using the dynamic relay model. Results are presented in Fig. 8.
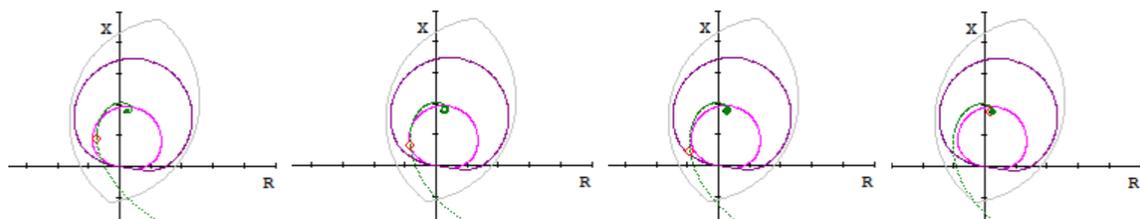

Fig. 8 Impedance loci for varying ramp rates (from left to right, 0.0035, 0.00245, 0.00175, 0.00112 pu/ms)

The corresponding tripping times are: 20ms; 19.8ms; 19.7ms; 19.5ms. In each case the relay trips effectively instantaneously with the minimum delay. As can be seen from Fig.8 the impedance locus does not change significantly as the ramp rate of the current varies. Therefore it may be concluded that the converter output current ramp rate may not have a significant effect on the performance of the distance relay. However, more work and studies of different fault scenarios remain to be carried out before confident conclusions can be drawn from this.

D. Case study 4: impact of varying converter output fault current level

In this case the penetration level of the converter-interfaced source fixed to be 100%, the initiation delay is fixed to be 1ms, and the ramp rate of the current is fixed at 0.00112pu/ms. The maximum sustained fault current is set to be 1.1pu, 1.4pu, 1.8pu, and finally 2.2pu. Solid three phase faults at 70% length of the line are applied and the relay response recorded. Responses are shown in Fig. 9.
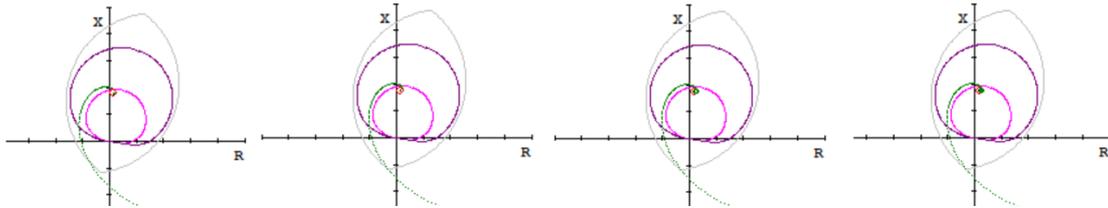

Fig. 9 .impedance loci for varying converter fault current levels (left to right, 1.1pu 1.4pu 1.8pu 2.2pu fault current)

The corresponding tripping time are: 29ms; 19.5ms; 19.5ms; 19.5ms. In each case the relay trips effectively instantaneously with the minimum delay – although there is a 10ms increase in tripping time for the lowest fault current magnitude. As can be seen from Fig.9 the impedance locus does not change significantly as the ramp rate of the current varies. Therefore it may be concluded initially that the converter output fault current level rate may not have a significant effect on the performance of the distance relay. However, more work and studies of different fault scenarios remain to be carried out before confident conclusions can be drawn from this.

V. CONCLUSIONS AND FUTURE WORK

Converter-interfaced power sources possess very different characteristics from conventional rotating power sources. The most up-to-date grid codes in GB and EU do not yet state the detailed requirements for the response of converters during faults, with requirements specified but no quantified responses being mandated. These are planned to be defined during implementation of the European Netwrok Codes at national level during forthcoming years. This paper has introduced and described a model of a VSC, with an appropriate controller, which is capable of producing configurable responses in response to faults on the supplied AC power system. The response of a particular distance protection scheme to three-phase faults on an AC system with a range of converter infeed penetration levels and a variety of converter fault responses (in terms of initial response delays, output current ramp rates and output current magnitudes) has been studies and the results presented. It is clear that while the protection performs well under a variety of circumstances, there are clearly instances where protection performance may be compromised. This is work from the relatively early stages of a research project, and work is on-going to refine and extend the range of studies being conducted.

Accordingly, future work will investigate the protection performance for different fault locations, especially around zone boundaries (to verify potential over or under reach), different fault resistances, and with different types of relays (both modelled and actual devices), including a range of different distance, differential and overcurrent schemes. The performance of main and backup protection schemes will also be analysed. The converter model will be further refined and validated against actual field/test data. The work will evolve from using relay models to employment of secondary injection equipment to evaluate the responses of actual protection relays to faults in converter-dominated systems. This will allow more precise quantification of the "tipping point", with respect to converter penetration level, at which protection devices and schemes will be seriously impacted. It will also reveal detailed information relating to the nature of the experienced problems and allow solutions to be investigated.

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