

Mixed cells modular multilevel converter

G.P. Adam, K.H[†]. Ahmed* and B.W. Williams[†]

University of Strathclyde, Glasgow, UK[†]

University of Aberdeen, Aberdeen, UK*

Email: [†]grain.adam@strath.ac.uk, *khaled@abdn.ac.uk and [†]barry.williams@strath.ac.uk

Abstract—This paper uses a scaled down version of the mixed cells modular multilevel converter (MMC) to discuss its modulation and capacitor voltage balancing method, and investigates its AC and DC fault ride-through capability. It has been found that the mixed MMC is resilient to both AC and DC network faults, which are necessary for next generations of highly meshed multi-terminal HVDC grids. The power losses comparison conducted in this paper has shown that the mixed cells MMC and three-level cells MMC achieve DC fault reverse blocking capability at reduced on-state losses than full-bridge MMC and alternative arm MMC.

Key words— DC fault reverse blocking capability; high-voltage DC transmission systems; hybrid cascaded multilevel converter; and modular multilevel converter.

I. INTRODUCTION

In the last ten years, voltage source converter based DC transmission systems have evolved from that built around conventional two-level and neutral-point clamped converters to that use true multilevel converters, which are scalable to high voltage[1-10]. This evolution is motivated by an attempt to increase DC operating voltage in order to achieve higher power transfer capacity at reduced semiconductor and transmission losses, and without exposing converter transformers to increased voltage stresses. This in addition to elimination of ac side filters, benefiting from improved quality of the multilevel converter output voltage and current waveforms[6, 11-16]. At the Present, there are number of competing voltage source converter topologies being considered for next generation of DC transmission systems, including DC grids [4, 5, 9, 17-19]. Most of these converters have DC short circuit proof feature, which is essential for reliable operation of complex DC grids. Some of these converters achieve DC short circuit proof feature at reduced semiconductor losses, while others with small footprint. Based on [6], alternative arm modular converter provides a good compromised as it offers DC short circuit proof at relatively low semiconductor losses and small footprint. However, its main drawback is that converter switching devices are exposed to high inrush currents during current commutation between converter arms[4, 6]. Three-level and five-level cells MMCs discussed in [17] achieve DC short

circuit proof feature, with competitive level of semiconductor loss when compared to alternative arm modular converter, but with larger footprint. Recently, mixed cells MMC is introduced as a viable alternative to the above converter that offers DC short circuit proof feature, while maintaining the elegance of the conventional HB and FB MMC in terms of circuit structure and simplicity of the modulation strategies.

This paper describes operating principle of mixed cells MMC, and explores its steady state and dynamics response to AC and DC network faults. By comparing its on-state losses to that of the recent state of art multilevel converter topologies, it has been found that the mixed cells MMC and three-level cells MMC offer DC fault reverse blocking capability at lower semiconductor losses than FB MMC and alternative arm MMC. But alternative arm MMC is perceived to be superior from footprint prospective.

II. MIXED CELLS MODULAR MULTILEVEL CONVERTER

Fig. 1 shows one-phase leg of generic mixed cells modular multilevel converter, with N cells per arm. Its circuit structure, operational principle and modulation method are similar to that of the half and full-bridge modular converters, except 50% of cells are half-bridge (HB) cells and remaining 50% are full-bridge (FB) cells. Adoption of mixed cells in this version of modular converter is motivated by achieving DC short circuit fault reverse blocking at reduced semiconductor loss, while avoiding the problem of inrush current experienced in alternative arm MMC discussed in [4, 6] during current commutation between upper and lower arms, despite insertion of the overlap period being suggested. This paper controls mixed cell modular converter in Fig. 1 on per arm basis, where the modulation functions of the upper and lower arms of the phase ‘a’ are defined as: $v_u = \frac{1}{2}(1 - M \sin \omega t)$ and $v_l = \frac{1}{2}(1 + M \sin \omega t)$. Recall that the modulation index M is defined as ($M = V_m / \frac{1}{2} V_{dc}$), and V_m is the peak phase voltage and V_{dc} is the input DC link voltage. In attempt to simplify the overall control of the mixed cells MMC being considered, implementation of the modulation and capacitor voltage balancing strategy is separated into two parts. The first part uses the modulation functions above, with staircase modulation or carrier based pulse width modulation

to identify the cell capacitors to be inserted into the power path and those to be bypassed regardless of cell type. This part uses cell capacitor voltage magnitudes and arm current polarities to send a signature of ‘1’ for the cells their capacitors to be inserted in power path and signature of ‘0’ to the cells their capacitors to be bypassed. The second part places special logic at individual cell level, which is responsible for generation of gating signals depending on cell type. Observe that this approach is intended not to fully exploit bi-polar capability of the full-bridge cells in order to reduce cell capacitor size in favour of reducing effective switching frequency at cell level. Thus, low switching losses are maintained. However, this paper uses pulse width modulation (PWM) with phase disposition (PD) carriers instead of amplitude modulation due to adoption of the mixed cells modular converter with only four cells per arm.

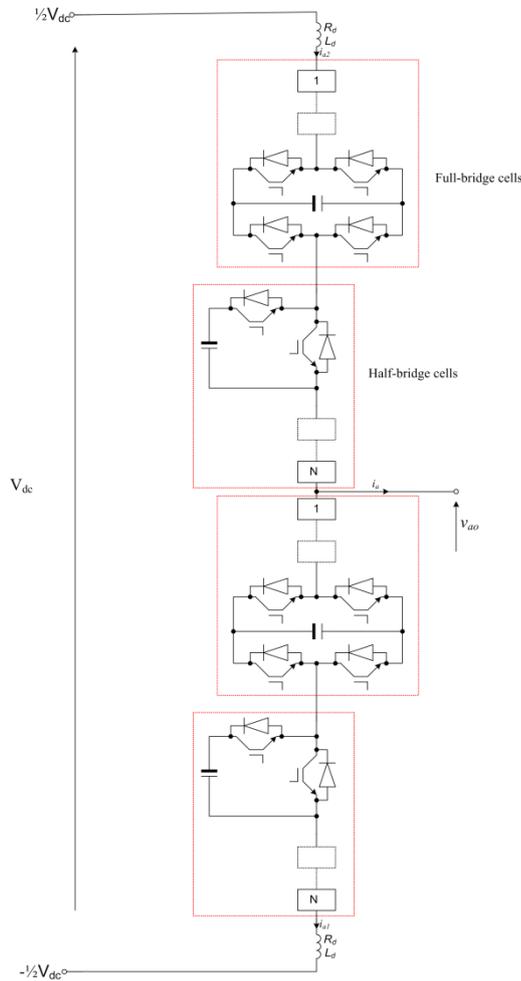


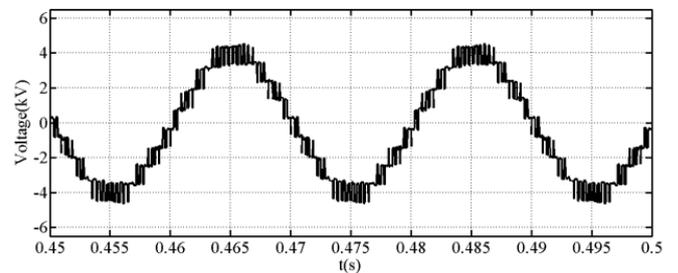
Fig. 1: Mixed cells modular multilevel converter

III. SIMULATIONS

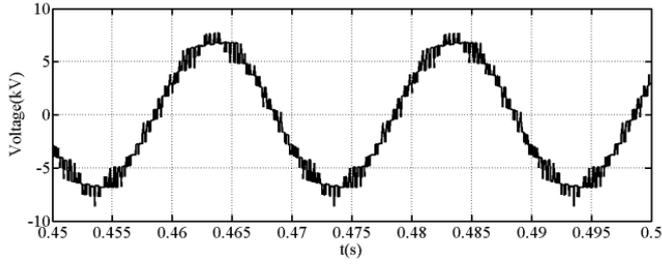
A) Steady state and loss evaluation of the mixed cells MMC

This section uses three-phase version of the mixed cells modular converter in Fig. 1 rated at 6MVA with 10kV input dc link voltage to illustrate its steady state and dynamic response during AC and DC network faults. Number of cells per arm is four, evenly divided between HB and FB cells. Sinusoidal pulse width modulation (SPWM), with 1.35kHz carrier frequency is adopted for open and closed operation. Converter cell capacitance and arm inductance are 4mF and 2.5mH respectively. Additional controller is incorporated to manipulate AC and DC components of the converter upper and lower arms modulating signals in order to minimize arm current 2nd harmonic content.

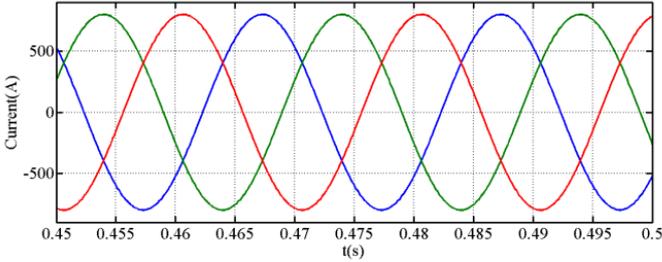
Fig. 2 displays simulation results obtained from the mixed cells MMC when it supplies a passive load of 3.83MW and 2.88MVar. Fig. 2 (a), (b) and (c) show a mixed cells MMC being studied generates high quality phase and line voltages, and output phase currents similar to that of conventional HB and FB MMCs. Fig. 2 (d) shows that the arm currents of the mixed cells MMC adhere to the same relationships of the traditional MMCs such as output phase current ‘ i_a ’ is equal to differential mode current ($i_a = i_{a1} - i_{a2}$); and arm current dc plus circulating harmonic currents is equal to the common-mode current i_{com} (where $i_{com} = i_{a1} + i_{a2}$). Fig. 2 e shows the cell capacitor voltages of the six converter arms remain balanced and settled around the desired set-point. The above results have shown that the steady state performance of the mixed cells MMC is similar to standard HB MMC. Additionally, mixed cells MMC is attractive because it uses a proven power circuit structure, with similar modulation and capacitor voltage balancing as that of the traditional MMCs. Despite adoption of the two different cells architecture, no undesired voltage spikes or inrush currents observed in the converter output voltage or arm current as that normally experienced in most of the hybrid topologies.



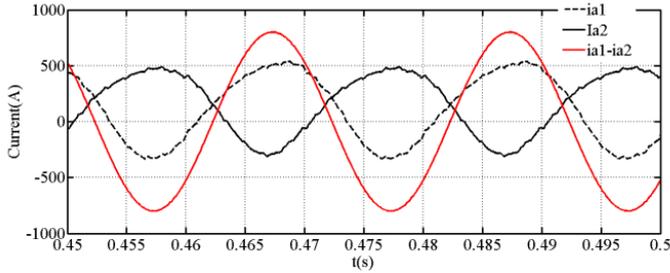
a) Phase voltage v_{a0}



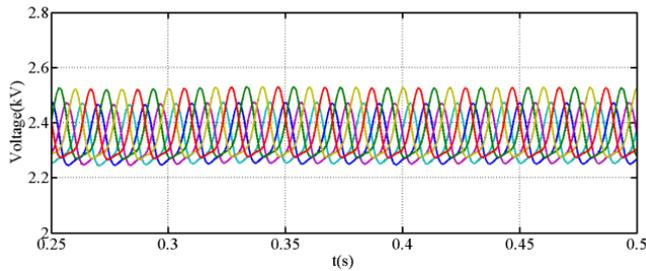
b) Line-to-line voltage at converter terminal



c) Three-phase load currents



d) Samples of upper and lower arm currents (i_{a1} and i_{a2}), and differential mode current $i_{a1}-i_{a2}$ (phase a)



e) Cell capacitor voltages of the three phases

Fig. 2: Waveforms obtained when three-phase mixed cells modular converter is operated in open loop, supplying a load of 3.83MW and 2.88MVar at 0.9 modulation index

Conduction loss is much larger than switching loss in most of the recent state of art multilevel converters that are developed for HVDC applications. On this ground, it has been used to compare the semiconductor loss of mixed cells modular converter to that of the other selected converter topologies. Since each converter topology presents specific

number of switching devices in conduction path for given voltage stress per devices and dc link voltage, converter conduction loss can be computed as:

$$P_c = P_{IGBT} + P_D \quad (1)$$

where, P_{IGBT} and P_D represent conduction losses in the IGBTs and anti-parallel diodes. P_{IGBT} and P_D are computed as:

$$P_{IGBT} = N \left[V_{0,IGBT} \bar{I}_{IGBT} + R_{on,IGBT} I_{rms,IGBT}^2 \right] \quad (2)$$

$$P_D = N \left[V_{0,D} \bar{I}_D + R_{on,D} I_{rms,D}^2 \right] \quad (3)$$

where, $R_{on,IGBT}$ and $R_{on,D}$, and $V_{0,IGBT}$ and $V_{0,D}$ represent on-state resistance and threshold voltage drop per IGBT and anti-parallel diode; and N is the number of switching devices in conduction path. With arm current polarities shown in Fig. 1, IGBTs and anti-parallel diodes average and root mean square currents are calculated as:

$$\bar{I}_{IGBT} = \frac{1}{2\pi} \left[I_d (\pi + 2\alpha) + 2\sqrt{I_0^2 - I_d^2} \right] \quad (4)$$

$$\bar{I}_D = \frac{1}{2\pi} \left[I_d (\pi - 2\alpha) - 2\sqrt{I_0^2 - I_d^2} \right] \quad (5)$$

$$I_{rms,IGBT}^2 = \frac{1}{2\pi} \left[\left(I_d^2 + \frac{1}{2} I_0^2 \right) (\pi + 2\alpha) + 3I_d \sqrt{I_0^2 - I_d^2} \right] \quad (6)$$

$$I_{rms,D}^2 = \frac{1}{2\pi} \left[\left(I_d^2 + \frac{1}{2} I_0^2 \right) (\pi - 2\alpha) - 3I_d \sqrt{I_0^2 - I_d^2} \right] \quad (7)$$

where, I_d and I_0 represent DC and peak fundamental components of the arm currents; and $\alpha = \sin^{-1} \frac{I_d}{I_0}$. Recall that

$I_d = \frac{1}{3} I_{dc}$ (I_{dc} is the dc link current) and $I_0 = \frac{1}{2} I_m$ (where, I_m represent peak of the output phase current). Equations (4) to (7) are valid for on-state losses estimation in HB-MMC, FB-MMC, mixed cells MMC and 3-level cells MMC, provided the dominant low-order harmonic components of the arm currents are eliminated. This approach may under estimate converter on-state losses, if some of the low-order harmonics in the converter arm currents are not completely eliminated as the case when complex modulation methods are used. Equations used to calculate average and root mean square currents in the IGBTs and anti-parallel diodes of the alternative arm MMC are:

$$\bar{I}_{av_IGBT} = \frac{I_m}{2\pi} [1 + \cos \varphi] \quad (8)$$

$$I_{rms_IGBT}^2 = \frac{I_m^2}{4\pi} \left[\pi - \varphi + \frac{1}{2} \sin 2\varphi \right] \quad (9)$$

$$\bar{I}_{av_D} = \frac{I_m}{2\pi} [1 - \cos \varphi] \quad (10)$$

$$I_{rms_D}^2 = \frac{I_m^2}{4\pi} \left[\varphi - \frac{1}{2} \sin 2\varphi \right] \quad (11)$$

where, φ is the power factor angle in rad.

Using 4.5kV IGBT data provided in[6], the calculated conduction losses for mixed cells MMC, HB-MMC, FB-MMC, three-level cells MMC, alternative arm MMC are summarized in Table 1. These losses are computed assuming 687MVA converter with 600kV dc link voltage and rated ac voltage of 300kV (line-to-line rms). Assume the voltage stress across each switching devices must not exceed 2.25kV, number of cells per arm is 270 for mixed cells MMC. Numbers of semiconductor switches in conduction path (N) for each converter topology being compared are shown in Table 1. Observe that the HB-MMC offers the lowest loss as expected. However, it lacks short circuit proof feature. Among converter topologies that offer short circuit proof, mixed cells MMC and 3-level cells MMC have the lower on-state losses. FB-MMC has the highest on-state loss in applications that involve large active power transfer. This is due to combination of large number of semiconductor in conduction path, and arm current DC component.

Table 1: Comparison of semiconductor losses of state of art multilevel converter topologies that offer short circuit proof feature (for mixed cell MMC, 3-level cells MMC and alternative MMC number switching devices in conduction path per arm N=405, N=270 for HB-MMC and N=540 for FB-MMC).

Converter type	On-state losses		
	P=600MW and Q=0	P=0 and Q=600MVAr	P=600MW and Q=300MVAr (lagging)
Mixed cells MMC	4.03MW (0.67%)	3.51MW (0.58%)	4.26MW (0.71%)
HB-MMC	2.69MW (0.45%)	2.34MW (0.39%)	2.84MW (0.47%)
FB-MMC	5.38MW (0.90%)	4.68MW (0.78%)	5.69MW (0.95%)
3-level cells MMC	4.03MW (0.67%)	3.51MW (0.58%)	4.26MW (0.71%)
Alternative arm MMC	4.43MW (0.74%)	4.43MW (0.74%)	4.78MW (0.80%)

B) AC and DC fault ride-through capability

For AC and DC fault ride-through demonstration, a medium-voltage mixed cells MMC is simulated as a grid connected inverter as shown in Fig. 3. In this demonstration, the following controllers are incorporated: fundamental current controller in d-q, 2nd harmonic current suppression in phase variables, active power and ac voltage.

Fig. 4 displays simulation waveforms obtained when the test system in Fig. 3 is subjected to three-phase AC fault at location F₁ and cleared after 200ms. Active power matching presented in [20] is used during AC fault to minimize the over-charging of the cell capacitors. Plots for active and reactive powers and voltage magnitude in Fig. 4 (a) and (b) show the mixed cells MMC is able to recover from three-phase AC fault near to PCC, with currents in converter switches and cell capacitor voltages are tightly controlled, see Fig. 4 (c) and (d). These results have shown that the mixed

cells MMC inherent the resiliency of the conventional MMCs to AC network faults.

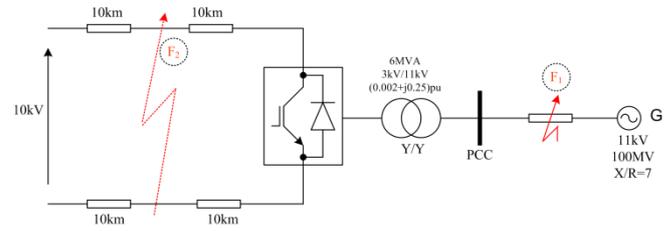
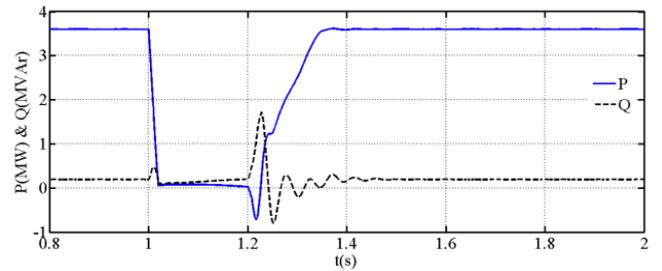
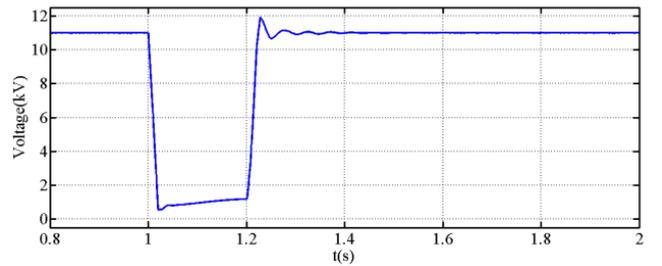


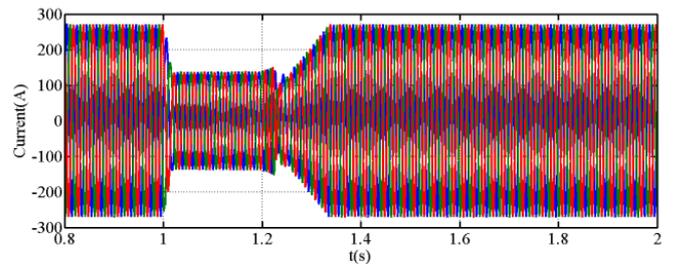
Fig. 3: Test system used for ac and dc fault ride-through capability of the mixed cells modular multilevel converter



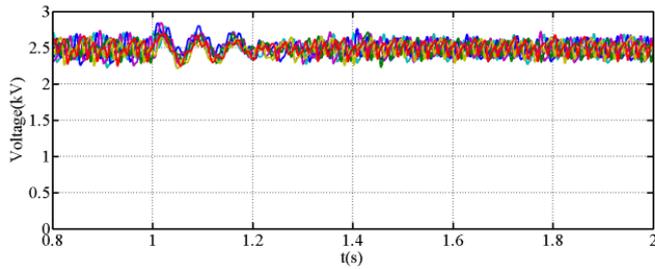
a) Active and reactive power converter exchanges with PCC



b) Voltage magnitude at PCC

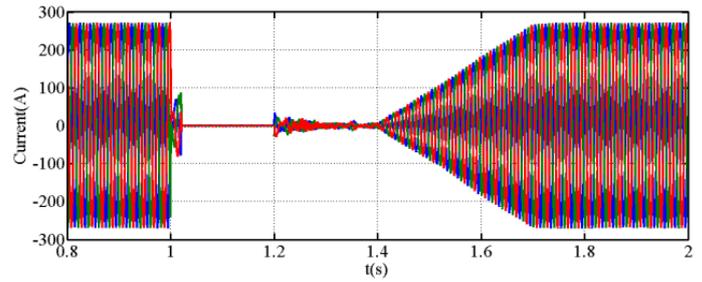


c) Current waveforms converter injects into PCC

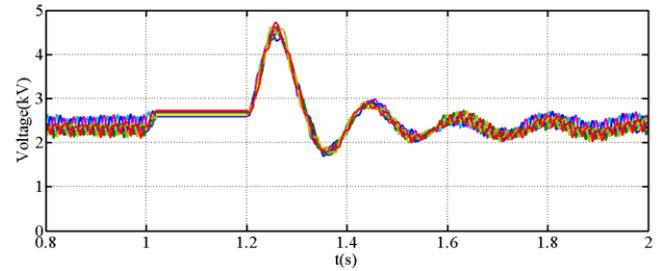


d) Cell capacitor voltages of the three phases

Fig. 4: Waveforms demonstrate ac fault ride-through capability of the mixed cells MMC



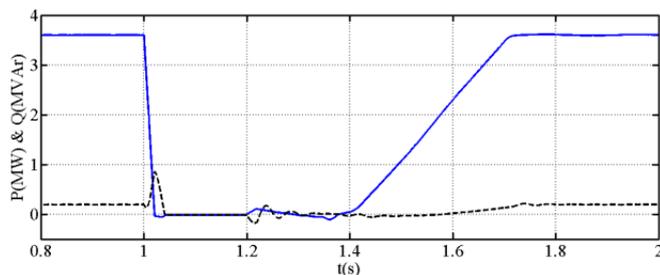
b) Current waveforms converter injects into PCC



c) Cell capacitor voltages of the three phases

Fig. 5: Waveforms demonstrate dc fault ride-through capability of the mixed cells MMC

Fig. 5 displays simulation waveforms obtained when the test system in Fig. 3 is subjected to DC fault at location F_2 and cleared after 200ms. Gating signals to converter switches are blocked during the fault period and restored immediately when the fault is cleared. When DC fault is initiated at $t=1s$, converter active power output is reduced to zero and slowly restored at $t=1.4s$ (200ms after fault is cleared). This is to minimize the transients during brief period of uncontrolled recharging of the DC line stray capacitor when converter switches are unblocked. Plots for active and reactive powers and AC current waveforms in Fig. 5 (a) and (b) show the mixed cells MMC is able to recover from the solid pole-to-pole DC fault at the middle of the DC link. Observe that during the entire fault period, current waveforms converter exchange with the AC grid drop to zero, indicating that the AC grid contribution to DC fault current is completely eliminated. Moreover, notice that the cell capacitor voltages become flat, with no ripple as converter switches are blocked during DC fault period, see Fig. 5 (c). These results have shown that the mixed cells MMC is resilient to DC network faults as the FB-MMC, alternative arm MMC and hybrid cascaded multilevel converter in[6, 9]. These results have confirmed the DC fault reverse blocking capability can be achieved with only 50% of the converter cells need to be full-bridge cells, without the need for circuit topology modification as that leads to alternative arm modular converter.



a) Active and reactive power converter exchanges with PCC

IV. CONCLUSIONS

This paper presented detailed discussion of the mixed cells MMC modulation and capacitor voltage balancing method, and studied its steady state in open loop and closed loop response to AC and DC network faults. Device and system level studies carried out have shown that the mixed cells MMC is promising for multi-terminal HVDC DC grids as it combines the low loss of HB cells MMC with the short circuit proof feature of the FB cells MMC. However, its footprint remains the same as the HB and FB MMCs, which may favour the use of alternative arm MMC in applications with confined space.

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