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Half and Full-Bridge Modular Multilevel Converter Models for Simulations of Full-Scale HVDC Links and Multi-terminal DC grids

G.P. Adam, IEEE Member, and B.W. Williams

***Abstract*—This paper presents an improved electromagnetic transient (EMT) simulation models for the half and full-bridge modular multilevel converters that can be used for full-scale simulation of multilevel high-voltage dc transmission systems, with hundreds of cells per arm. The presented models employ minimum software overhead within their electromagnetic transient parts to correctly represent modular multilevel converters (MMC) behaviour during dc network faults when converter switching devices are blocked. The validity and scalabilities of the presented models are demonstrated using open loop simulations of the half and full-bridge MMCs, and closed loop simulation of a full-scale HVDC link, with 201 cells per arm that equipped with basic HVDC controllers, including that for suppression of the 2nd harmonic currents in the converter arms. The results obtained from both demonstrations have shown that the presented models are able to accurately simulate the typical behaviour of the MMC during normal, and ac and dc network faults.**

***Key words*—electromagnetic transient simulation; high-voltage dc transmission system; half and full-bridge modular multilevel converter; and hybrid multilevel converters.**

I. INTRODUCTION

Increased operational flexibilities of the voltage source converter based high-voltage dc (VSC-HVDC) transmission system within ac power systems in the last decade have encouraged its universal acceptance by the power system utilities worldwide[1-12]. Additionally, its evolution from that build around the two-level and neutral-point clamped converter topologies to that built using true multilevel converters, with low semiconductor losses and improved ac side waveforms quality have accelerated its adoption in many of the recent HVDC transmission systems projects[13-19]. Replacing of the traditional concept of voltage source converter that uses concentrated reservoir capacitors at the converter dc input by that uses distributed capacitors such as that in modular multilevel converter has improved the resiliency of the VSC-HVDC transmission systems to ac and dc network faults[20-27]. For aforementioned reasons, modular multilevel converter has become the preferred technology for large-scale HVDC links and dc grids that could ensure safe and reliable operation during ac and dc network disturbances.

Full-scale modelling of the VSC-HVDC links that use half or full bridge cell modular converters, with hundreds of cells per arm is computationally intensive task that requires machines with high computing power and large memory, and takes long time to simulate. The traditional switching models that use power electronic building blocks with full capabilities of mimicking conduction of the physical devices (such as IGBT and its anti-parallel) are proven to be inefficient for full-scale modelling of the MMC based HVDC links as simulation times become prohibitively long. Despite the above shortcomings, this approach remains widely used, where transient response of the MMC based HVDC links to ac and dc network faults are studied using reduced number of cells. This is because the switching model is extremely useful when comes to capturing of the MMC internal dynamics in great details during ac and dc network faults. In attempt to reduce simulation time, the authors in [28, 29] presented an averaged model of the MMC based HVDC link where the ac component of the MMC upper and lower arms modulation functions are obtained directly from the inner current controller and appropriate dc offsets are added. These modulating functions are used as inputs to the two controlled voltage sources that mimicked the voltage developed across MMC upper and lower arms. The main weakness of this approach is that it does not allow natural development of the arm current dc component and circulating current, thus not able to naturally developed dc power as in real world MMC. For this reason, the authors in [28, 29]included additional stage that artificially injects dc components into converter arms, estimated based on power balance principle, and also this stage has been used to mimic MMC converter operation during gate blocking as required during dc network fault. Additionally, injection of the dc components into converter arm currents as in [28, 29] results in instantaneous balance between MMC ac and dc powers, and this deprives the approach presented in [28, 29] from accurately reproduce the dc power dynamics due to MMC inertia and propagation delays due to arm and dc line inductances (inductances in the dc current paths). Although, the approach in [28, 29] provides an efficient way of modelling MMC based HVDC link for general system level studies, it cannot reproduce MMC internal dynamics at microscopic levels as required in design stage and for protection purposes during ac and dc network faults.

Reference [30] presented an efficient method for full-scale modelling of the MMC based HVDC link that uses electromagnetic transient approach. The authors in [30] use Dommel's Norton and Thevenin equivalent circuits of the MMC cell capacitors, and two-state resistor representation of the switching devices to reduce the entire arm of the MMC to a simple Thevenin equivalent circuit, with two terminals. This approach significantly reduces computation burden that arises from solution of the power circuit, while that due to modulation and capacitor voltage balancing is retained as in detail switching models. Despite above simplification, this approach is able to capture some of the MMC internal dynamics that associated with the cell capacitor voltages and arm currents, and also allow natural development of the dc and circulating current components of the MMC arms, hence, it is able to reproduce the dynamics of the dc power. However, the electromagnetic transient approach as discussed in reference [30] cannot reproduce dynamic interaction between ac and dc sides during dc network fault.

The accelerated model of the MMC presented in [31] is developed in similar theoretical basis as that in [30], except

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the authors unknowingly have treated each individual MMC cell as a primitive circuit that share the same current injection equal to the arm current, and this assumption permits application of the generalized circuit theory by Kron [32-34] . Additionally, this allows Kron connection matrix to be constructed using relationships between arm current and individual cell currents, and such connection matrix can be used to prove that validity of the approach presented in [31]. The accelerated MMC model in its present form has the same attributes and limitations of that presented in [30]. Nevertheless, they remain the only practical ways to simulate full-scale MMC based HVDC link, with hundreds of cells per arm.

The authors in [35] presented two simplified MMC fundamental average models for slow dynamic studies that deliberately ignore converter switching actions and dynamics of the cell capacitors, while considering that of the ac side in order to enable the use of large time step and reduce simulation time. Reference [35] has shown that this approach is suitable for transient and small signal stability studies where manipulation of the converter output active and reactive powers are useful for improving stability of the ac parts of the power systems; but it is inappropriate for use in any studies that concern with the dc side and fast transient. Furthermore, both MMC models proposed in [35] are unable to naturally developed dc current components of the arm currents; thus, unable to produce dc power naturally.

The authors in [36, 37] proposed an interesting approach that uses a factitious network known as Surrogate to model full-scale MMC based HVDC link. This approach replaces the actual MMC cells in each converter arm by their Surrogate equivalents that produce the same computational results as the true cells. Surrogate network for each arm of the half or full-bridge MMC contains three sub-networks that represent converter blocking state, sub-modules bypass state, and positive and negative sub-modules insertion states. This approach is appeared to be promising for large-scale modelling of the multi-terminal HVDC networks where MMC internal dynamics are less important. References [36, 37] have demonstrated the suitability of Surrogate network modelling approach of the MMC for real-time simulation and hardware in loop, with much smaller time step than other commercially available real-time digital simulators. However, its ability to accurately simulate dc fault is yet to be seen.

This paper improves the MMC modelling approach presented in [31] to be able to simulate the performance of full-scale MMC based HVDC links during ac and dc network faults, and to capture its internal dynamics to microscopic levels (cell capacitor voltages, arm currents, current stresses in switching devices, and dynamics of ac and dc powers). The ability to simulate dc fault is achieved by setting values of the two-state resistors that represent the MMC switching devices to mimic exactly the physical operation of gate insulated bi-polar transistors(IGBT) and their anti-parallel diodes during gate blocking, taking into account arm currents polarities. The first part of this paper presents an open loop demonstrations of the half and full-bridge MMC, including validation of the presented half-bridge MMC model against its switching counterpart, and scalability of the full-bridge MMC model. The second part of this paper presents a closed loop demonstration that uses a full-scale model of the half-bridge MMC based HVDC to simulate its performance during normal operation, and ac and dc network faults. The results obtained from both demonstrations have shown that the presented MMC model is able to reproduce the typical behaviour of MMC based HVDC links to microscopic level in all the above studies. This qualifies the presented MMC model to be used for detailed studies of the MMC based HVDC links at design stage such as fine tuning of MMC passive parameters, and validation of the control and protection systems.

II. REVIEW OF THE MODULAR MULTILEVEL CONVERTER

Figure 1 shows three-phase generic modular multilevel converter with N cells per arm. For input dc link voltage 'V_{dc}', voltage stress across each switching devices is V_{dc}/N, provided that the voltage across each cell capacitor is maintained at V_{dc}/N [38-41]. In each instant, *K* and *N-K* cell capacitors from the upper and lower arms must be inserted in the power path in order synthesize different output voltage levels. This ensures that $v_{a1}+v_{a2}=V_{dc}\pm\Delta v$; where v_{a1} and v_{a2} represent voltages across the upper and lower arms of phase 'a', and ΔV represents ac plus dc voltage drop in the internal resistance (R_d) and inductance (L_d) of the arm reactors. In other words, from *2N* available cell capacitors in each phase (upper and lower arms) of the modular converter, only *N* cell capacitors must be switched into the power path while the *N* remaining cell capacitors must be bypassed. Such restriction necessitates complementary operation of the upper and lower arms of the modular converter[42]. Since modular converter synthesizes the amplified version of the modulating signals (sinusoidal output voltage) by insertion of its cell capacitors into power path sequentially, flow of fundamental current through these capacitors plus voltage drop across arm reactors will cause the cell capacitor voltages to oscillate around fixed dc component. The exact value of the cell capacitor voltages dc component is influenced by power flow direction, and can be determined by $(V_{dc}\pm 2R_dI_d)/N$; where I_d is the arm current dc component. Oscillation of the upper cell capacitor voltages against that of the lower arm, and that of individual phase against main dc link voltage cause additional current components to flow in the modular converter arms (inrush plus circulating currents). The inrush currents are cause by switching of the cell capacitor in and out of the power path for the purpose of maintaining capacitor voltage balancing, and oscillation of the upper arm against the lower arm. The circulating currents are caused by oscillation of individual phase arm voltages such as $v_{a1}+v_{a2}$, $v_{b1}+v_{b2}$ and $v_{c1}+v_{c2}$ against the main dc link voltage (V_{dc}); where v_{b1} and v_{b2}, and v_{c1} and v_{c2} are the voltage developed across the upper and lower arm cell capacitors of the phases b and c.

Unlike conventional voltage source converters, the upper and lower arms of the modular converter conduct simultaneously, and this result in each arm contributes half of the output phase current, thus, half of the ac power per phase converter exchanges with the ac side. The power exchange between each phase and dc side is achieved through dc power, which is related to I_d (dc component of the arm current). Flow of the three current components in the semiconductor switches cause modular converter to have higher on-state loss when compared to traditional voltage source converters such as two-level and neutral-point clamped[43]. Since fundamental and dc components of the arm currents are necessary for power exchange between ac and dc sides, the inrush and circulating current component of the arm current must be minimized in

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order to reduce modular multilevel converter on-state loss as discussed in [44-46]. However, active suppression of the 2nd harmonic in the arm current, which is the dominant component of the circulating current as suggested in [47-52] is associated with additional switching losses, and also limits the maximum attainable modulation index (hence, results in smaller converter P-Q envelope). Method that uses passive filter to suppress arm current circulating in the modular converter is proposed in [53]. This method avoids the shortcoming of the previous method that actively suppresses arm circulating current, but its downside is that it requires additional passive component, which may slightly increase converter station footprint and losses. For more details on the modulation and cell capacitor voltage balancing adopted in this paper, refer to [41, 42, 44, 54-60].

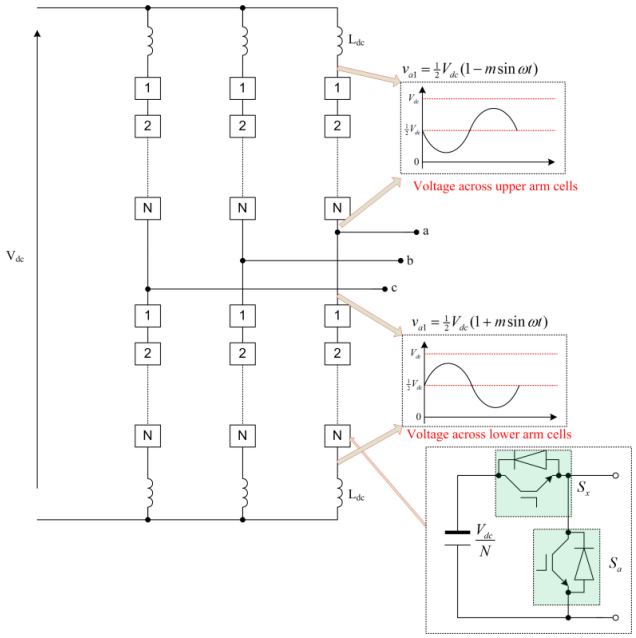

Figure 1: Schematic diagram of generic three-phase modular multilevel converter

III. GENERIC ELECTROMAGNETIC TRANSIENT MODELLING OF MODULAR MULTILEVEL CONVERTER

A) Half-bridge MMC model

Figure 2 (a) and (b) show half-bridge cell version of the modular multilevel converter and its electromagnetic transient representation based on Dommel trapezoidal method. Switching devices S_{xi} and S_{ai} in Figure 2(a) are replaced by switched resistances R_{xi} and R_{ai} in the electromagnetic transient simulation equivalent circuit in Figure 2(b). The cell capacitor in Figure 2(a) is replaced by its trapezoidal Norton equivalent circuit in Figure 2(b). When switching devices S_{xi} or S_{ai} are on their corresponding switched resistances are set to R_{on1} or R_{on2} (on-state resistances of the switches S_{xi} and S_{ai}). When S_{xi} or S_{ai} are off their corresponding switched resistances are set to R_{off1} or R_{off2} (off-state resistances of the switches S_{xi} and S_{ai}). Switched resistances R_{xi} and R_{ai} are set to mimic operation of typical switches of the modular converter when they receive gating signals from the modulator. Thus, during normal operation, R_{xi} and R_{ai} are set on and off in complementary manner as in typical operation of S_{xi} and S_{ai} in MMC [41, 42, 61]. To mimic MMC operation during gate signal blocking as happens during dc short circuit faults, R_{xi} and R_{ai} are set based on the arm current polarity and peak of line-to-line voltages. Line-to-line voltages at converter terminals are used to mimic diode rectifier operation of the typical MMC when gate signals are inhibited. Arm currents polarities are used to mimic conduction of the anti-parallel diodes of the switching devices S_{xi} and S_{ai}. For example, assume arm current I_{mi} in Figure 2 (a) and (b) is positive, when $I_{mi}<0$, R_{ai} for all cells in the upper and lower arms that expose maximum line-to-line voltage are set on, and all remaining switches must set to off-state (typical diode rectifier operation). When $I_{mi}>0$, and R_{xi} for the entire arm must be on to mimic the gate blocking condition in typical MMC operation when the conduction path is through anti-parallel diodes of S_{xi} and cell capacitors. In this manner, the electromagnetic transient representation of the MMC cell mimics the exact operation of the physical half-bridge MMC cell operation in all operating modes.

For full MMC representation, this paper adopted per arm representation of the MMC in [31] that considers each arm of MMC comprises of N individual cells driven by one current source its value equal to arm current, and each cell generates voltage v_{mi} between its terminals (x_i relative to imaginary ground). The total voltage developed across each converter arm is assumed to be equal to sum of the cell voltages ($V_{arm}=\sum_{i=1}^{N}V_{mi}$), where N is the number of cells per arm. Assuming the imaginary ground of each cell is located at its zero voltage level, the nodal equation that describes dynamics of each cell within each time step Δt can be expressed as follow:

$$\begin{bmatrix} \frac{1}{R_{xi}}+\frac{1}{R_{ai}} & -\frac{1}{R_{xi}} \\ -\frac{1}{R_{xi}} & \frac{1}{R_{xi}}+\frac{2C}{\Delta t} \end{bmatrix}\begin{bmatrix} V_{xi} \\ V_{yi} \end{bmatrix}=\begin{bmatrix} I_{mi} \\ I_{hci} \end{bmatrix} \quad (1)$$

Where V_{xi} and V_{yi} represent the nodal voltages of the node y and x in the i^{th} cell measured relative to virtual ground of the same cell. Observe that V_{xi} and V_{yi} represent the i^{th} cell output and capacitor voltages respectively. Therefore, $V_{mi}=V_{xi}$ and $V_{ci}=V_{yi}$. The current of each cell is defined based on Dommel trapezoidal integration method as:

$$I_{hci}=I_{ci}(t-\Delta t)+\frac{2C}{\Delta t}V_c(t-\Delta t) \quad (2)$$

Instantaneous currents in the composite switches S_{xi} and S_{ai} (IGBT plus anti-parallel diode) are:

$$I_{Sxi}=\frac{V_{xi}-V_{yi}}{R_{xi}} \quad (3)$$

$$I_{Sxi}=\frac{V_{xi}}{R_{ai}} \quad (4)$$

However, this paper does not formulate nodal equation matrix for the entire arm as in [31], instead it computes the cell output and capacitor voltages for N cells directly from (1) as:

$$V_{mi}(t)=V_{xi}(t)=\frac{1}{\Omega}\left[\left[\frac{1}{R_{xi}}+\frac{2C}{\Delta t}\right]I_{mi}+\frac{1}{R_{xi}}I_{hci}\right] \quad (5)$$

$$V_{ci}(t)=V_{yi}(t)=\frac{1}{\Omega_i}\left[\frac{1}{R_{xi}}I_{mi}+\left[\frac{1}{R_{xi}}+\frac{1}{R_{ai}}\right]I_{hci}\right] \quad (6)$$

Where $\Omega_i=\frac{1}{R_{xi}}\times\left[\frac{1}{R_{ai}}+\frac{2C}{\Delta t}\right]+\frac{2C}{\Delta t}\times\frac{1}{R_{ai}}$; and observe that for N cells, equations (5) and (6) need to be solved N times single

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time step, without the need for matrix inversion, and voltage developed across converter arm is computed as explained above. In this manner, computation intensity of the model is greatly reduced. Figure 2(e) and (f) show typical MMC arm and its electromagnetic transient equivalent circuit, and Figure 3 shows one phase leg of the MMC, including interfacing of the electromagnetic transient part into Simulink SimPower building blocks.

B) Full-bridge MMC model

Figure 2 (c) and (d) show typical full-bridge MMC cell and its electromagnetic transient equivalent circuit. Observe that the switching devices S_{i1} through S_{i4} are replaced by the switched resistances R_{i1} through R_{i4}, and cell capacitor by its Norton equivalent. During normal operation, R_{i1} and R_{i3} are set on and off to produce cell output voltage V_{mi} equal to V_{ci}, 0 and $-V_{ci}$ at node x_i relative to cell virtual ground, and operation of switched resistances R_{i2} and R_{i4} are complementary to that of R_{i1} and R_{i3} respectively. $V_{mi}=V_{ci}$ is achieved by setting $R_{i1}=R_{on}$ and $R_{i3}=R_{off}$; $V_{mi}=-V_{ci}$ is achieved by setting $R_{i1}=R_{off}$ and $R_{i3}=R_{on}$; and $V_{mi}=0$ can be achieved either by setting $R_{i1}=R_{on}$ and $R_{i3}=R_{on}$ or vice versa. During gate blocking, arm current polarity is used to set the switched resistances of the equivalent cell in the entire arm simultaneously. For example, assuming I_{mi} in Figure 2(d) is positive, $R_{i1}=R_{on}$ and $R_{i3}=R_{off}$ for $I_{mi}>0$, and $R_{i1}=R_{off}$ and $R_{i3}=R_{on}$ for $I_{mi}<0$. Observe that because as the total voltage across cell capacitors is greater than the peak of line voltage, the cell capacitors will oppose the current flow in the arm, and there is no direct path for the current to flow through the switched resistances as in half-bridge cell case. Additionally, in case the total voltage across the cell capacitors of the all three phases happen to be smaller than the peak line voltage during the gate blocking, the cell capacitors of the full-bridge MMC will be charged for positive and negative arm currents. The nodal equation that describes the dynamics of Dommel electromagnetic transient model of the full-bridge MMC in Figure 2 (d) within each time step is:

$$\begin{bmatrix} \frac{1}{R_{i1}}+\frac{1}{R_{i2}} & -\frac{1}{R_{i1}} & -\frac{1}{R_{i2}} \\ -\frac{1}{R_{i1}} & \frac{1}{R_{i1}}+\frac{1}{R_{i3}}+\frac{2C}{\Delta t} & -\frac{2C}{\Delta t} \\ -\frac{1}{R_{i2}} & -\frac{2C}{\Delta t} & \frac{1}{R_{i2}}+\frac{1}{R_{i4}}+\frac{2C}{\Delta t} \end{bmatrix} \begin{bmatrix} V_{xi} \\ V_{yi} \\ V_{zi} \end{bmatrix} = \begin{bmatrix} I_{mi} \\ I_{hci} \\ -I_{hci} \end{bmatrix} \tag{7}$$

Where, each cell output and capacitor voltages are defined as:

$$\begin{aligned} V_{mi} &= V_{xi} \\ V_{ci} &= V_{yi} - V_{zi} \end{aligned} \tag{8}$$

Currents in the switching devices of each cell can be expressed as explained in the half-bridge MMC case. The voltage develops across each converter arm is expressed as the sum of the individual cell output voltage.

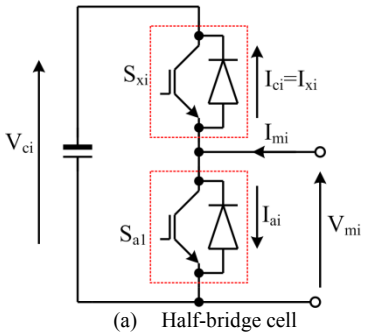
For large number of cell as will be considered later in this paper, matrix inversion must be avoided to reduce computation burden on the processor (intensity) by pre-calculation of the node voltages as:

$$\begin{aligned} V_{xi} &= \frac{1}{\Omega_i}\left[\alpha_{11} I_{mi} + (\alpha_{12}-\alpha_{13}) I_{hci}\right] \\ V_{yi} &= \frac{1}{\Omega_i}\left[\alpha_{21} I_{mi} + (\alpha_{22}-\alpha_{23}) I_{hci}\right] \\ V_{zi} &= \frac{1}{\Omega_i}\left[\alpha_{31} I_{mi} + (\alpha_{32}-\alpha_{33}) I_{hci}\right] \end{aligned} \tag{9}$$

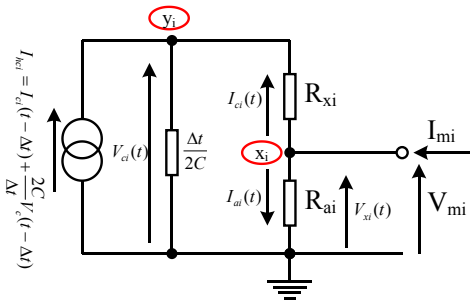
Where: $\alpha_{11} = \Delta t(R_{i1}+R_{i3})(R_{i2}+R_{i4}) + 2R_{i2}R_{i4}(R_{i1}+R_{i3})C + 2R_{i1}R_{i3}(R_{i2}+R_{i4})C$; $\alpha_{12} = \alpha_{21} = R_{i3}\left[\Delta t(R_{i2}+R_{i4}) + 2R_{i4}C(R_{i2}+R_{i1})\right]$,

$\alpha_{13} = \alpha_{31} = R_{i4}\left[\Delta t(R_{i3}+R_{i1}) + 2R_{i3}C(R_{i2}+R_{i1})\right]$; $\alpha_{22} = R_{i3}\left[\Delta t(R_{i1}+R_{i2}+R_{i4}) + 2R_{i4}C(R_{i2}+R_{i1})\right]$; $\alpha_{23} = \alpha_{32} = R_{i3}R_{i4}\left[\Delta t + 2C(R_{i2}+R_{i1})\right]$;

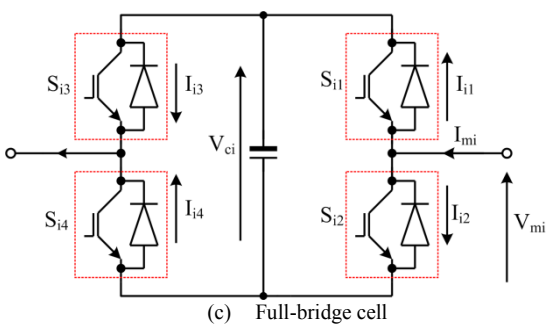
$\alpha_{33} = R_{i4}\left[\Delta t(R_{i1}+R_{i2}+R_{i3}) + 2R_{i3}C(R_{i2}+R_{i1})\right]$; and $\Omega_i = \Delta t\left[R_{i1}+R_{i2}+R_{i3}+R_{i4}\right] + 2C\left[R_{i1}R_{i3}+R_{i2}R_{i3}+R_{i1}R_{i4}+R_{i2}R_{i4}\right]$.



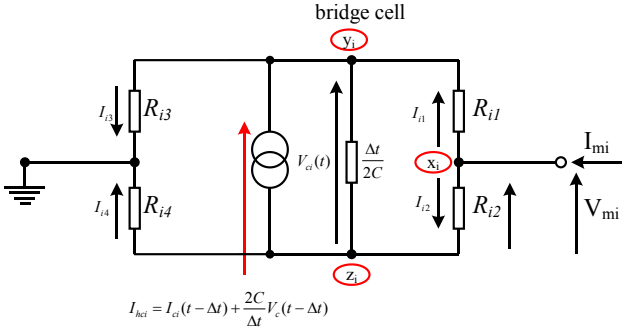
(a) Half-bridge cell



(b) Dommel electromagnetic transient representation of the half-bridge cell



(c) Full-bridge cell



(d) Dommel's electromagnetic transient representation of the full-bridge MMC cell

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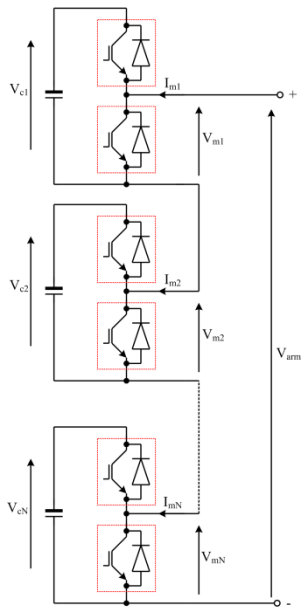
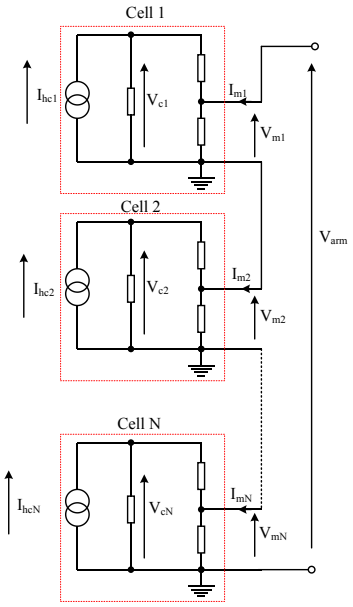


(e) One arm of the generic modular multilevel converter



(f) Dommel electromagnetic transient representation of the generic modular multilevel converter arm

Figure 2: Cell and arm of the generic modular multilevel converter and their Dommel electromagnetic transient representation

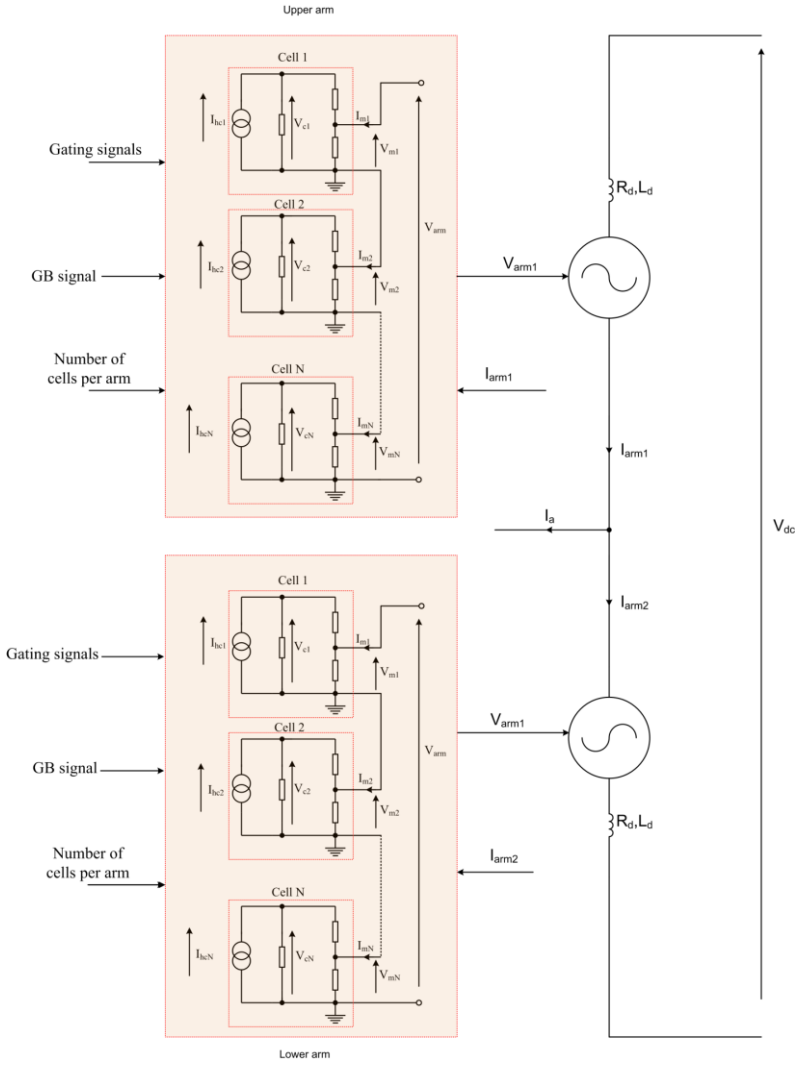


Figure 3: Illustration of the interfacing of the electromagnet transient model of the modular converter arms to SimPower System building blocks on a single-phase

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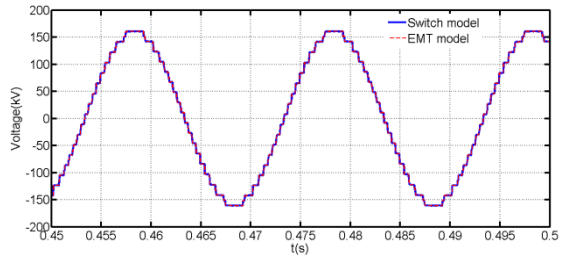
IV. MODEL VALIDATION

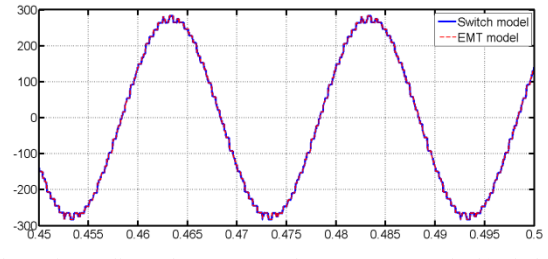
This section presents a validation of the generalized electromagnetic transient model of the MMC discussed in section III-A against its switching counterpart. In this validation, both models are built in Simulink; use the same circuit parameters shown in Table 1, and generalized modulator based on staircase modulation and capacitor voltage balancing; and proportional-integral controller for suppression of the arm currents 2nd harmonic. For validation only, both models are operated in open load at 0.8 modulation using sinusoidal references. Figure 4 display simulation waveforms obtained from both models. Figure 4 (a), (b) and (c) show pre-filter phase and line-to-line voltages at converter terminal, and three-phase load currents that obtained from MMC EMT model superimposed over that obtained from the MMC switching model, and observe that both model agree to smallest details as seen from the ac side. Figure 4 (d) and (e) present upper and lower arms cell capacitor voltages obtained from MMC switching and EMT models, and observe that both results are identical. Figure 4 (f) shows the sample of the upper and lower arm currents obtained from both models are identical as they coincide to microscopic level. Despite the level of agreements shown in Figure 4 (a) to (f), sample of the common-mode current of the phase 'a' that obtained as $i_{a1}+i_{a2}$ from the MMC switching and EMT models shows high level of agreement, with noticeable minor differences between the results of the two models. Based on these results it can be concluded that the presented EMT model of the MMC is sufficiently accurate since it is able to match its switching counterpart in every details to microscopic level. This validation is carried out when both models are simulated in discrete domain, with 5μs time step, and cell capacitor voltage measurements for the capacitor voltage balancing are updated on regular space of 500μs. Further validations of the presented EMT model versus its detailed switching counterpart during ac and dc faults are presented in the appendix.

Table 1: Summary of converter parameters used for validation

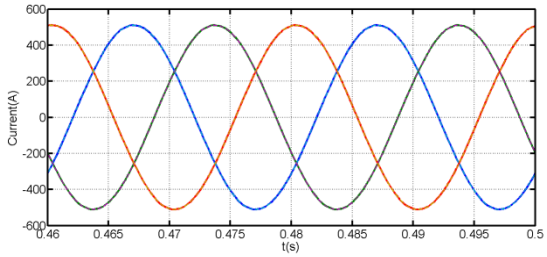
Parameter	Value
dc link voltage V_{dc} (kV)	400
cell capacitance C_m (mF)	1.4
arm inductance L_d (mH)	50
Arm inductance internal resistance R_d(Ω)	0.1
Load resistance R_L (Ω)	250
Load inductance L_L (mH)	597
Number of cell per arm (N)	21



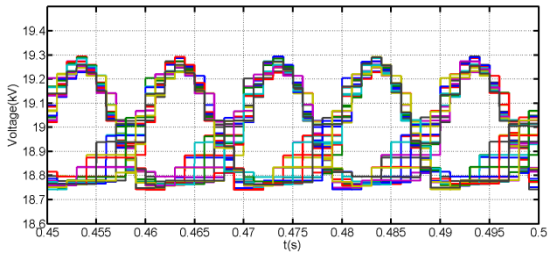
(a) Phase voltage measured converter terminal relative to supply mid-point (switch model superimposed on that obtained from EMT model)



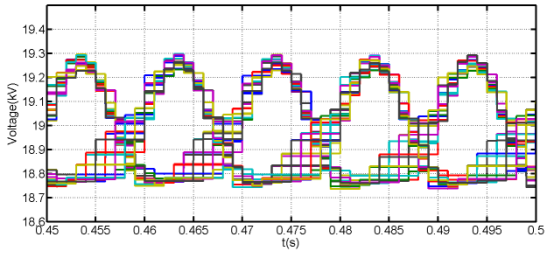
(b) Line-to-line voltage measured at converter terminal(switch model superimposed on that obtained from EMT model)



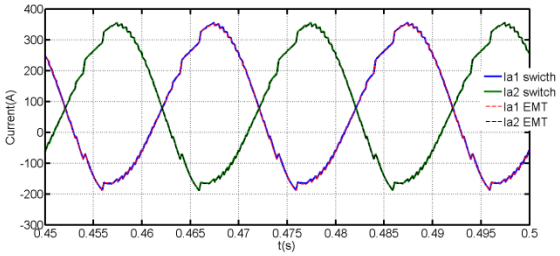
(c) Three-phase currents (switch model superimposed on that obtained from EMT model)



(d) Sample of the cell capacitor voltages of the phase A that obtained from switch model



(e) Sample of the cell capacitor voltages that obtained from electromagnetic transient model



(f) Sample of the upper and lower arm currents of the phase A (switch model superimposed on that obtained from EMT model)

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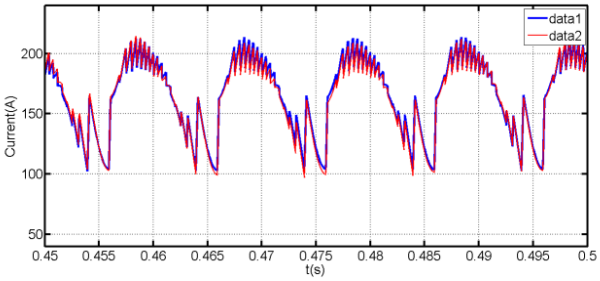
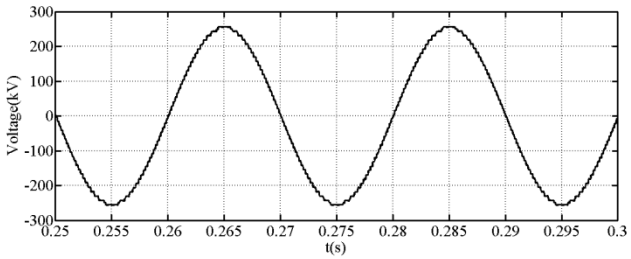


(g) Sample of the common mode current of the phase A (I_{a1}+I_{a2})

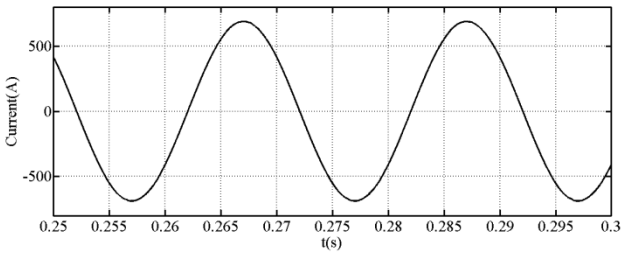
Figure 4: Waveforms presented aim to validate the MMC generalized model based on electromagnetic transient simulation approach against switch model that uses Simulink power electronics building blocks from SimPowerSystems library

In attempt to illustrate the scalability of the full-bridge model presented in this paper while restraining paper length, only sample results obtained from open loop operation of a single-phase full-bridge MMC with 51 and 301 cells per arm, ±320kV dc link voltage, 0.8 modulation index, and 300Ω and 690mH load are presented. Figure 5 presents selected waveforms obtained when number of cells per arm is 51. Figure 5 (a) and (b) samples of the phase and line voltage obtained with 51 full-bridge cells per arm, and observe that the converter being studied generates nearly pure sinusoidal output with only 51 cells per arm. This clearly justifies the reduced cell approach adopted in cascaded two-level converter presented in [53] that significantly reduces the complexity of the power circuit and modulation. Figure 5 (c) shows the upper and lower arm currents obtained for phase 'a', and notice that with the suppression of the 2nd harmonic in the arm currents, the upper and lower arm currents (i_{a1} and i_{a2})tend be dominated by the fundamental plus dc components, which are responsible from the power transfer between converter ac and dc sides. Figure 5 (d) shows the voltage balance of the cell capacitor voltages of the upper and lower arms are maintained tightly around V_{dc}/N (640kV/51≈12.55kV). Figure 5 (c) to (h) samples of the currents in the switching devices of one full-bridge MMC cell (top cell of the upper arm). Observe that the switching devices of the full-bridge cells MMC operate more frequently compared to that of the half-bridge cells MMC as will be shown later. This is due to exploitation of the extra redundancies offered by the bi-polar capability of the full-bridge cells that have been used to maintain cell capacitor voltage, and reduce the cell capacitance size. Additionally, it must be noticed that the switching devices S_{a12} and S_{a13} are used only to balance the capacitor voltages using redundant switch states that permit insertion of some the cell capacitor with the opposite polarities when synthesizing intermediate voltage levels between $½V_{dc}$ and $-½V_{dc}$. This indicates that the usage of switching devices S_{a11} and S_{a14} are much higher than that of the S_{a12} and S_{a13}, hence higher rated heat sinks may be required for S_{a11} and S_{a14}.

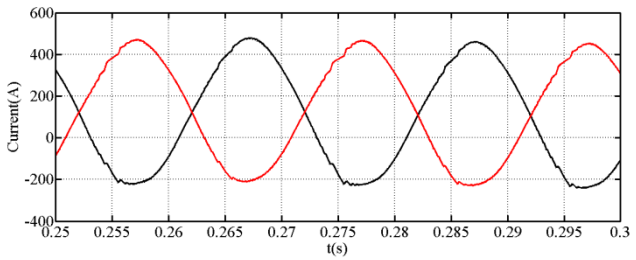
The results obtained when number of cells per is increased to 301 per arm are presented in Figure 6. Figure 6 (a) and (b) show the phase voltage obtained with 301 cells per arm is pure sinusoidal, and cell capacitor voltages of the upper and lower arms are maintained tightly around 2.13kV as anticipated. Figure 6 (c) shows the upper and lower arm currents are pure sinusoidal plus dc components. The samples of the currents in the switching devices of one full-bridge MMC cell in Figure 6 (d) and (e) show the switching frequency per device is not significantly reduced despite large increase in the number of cells per arm compared to the case presented in Figure 5 (e) and (g). Based on the results presented in Figure 5 and Figure 6, it can be concluded that the presented model in III-B is able to reproduce the typical behaviour full-bridge MMC in similar way of traditional switching model.



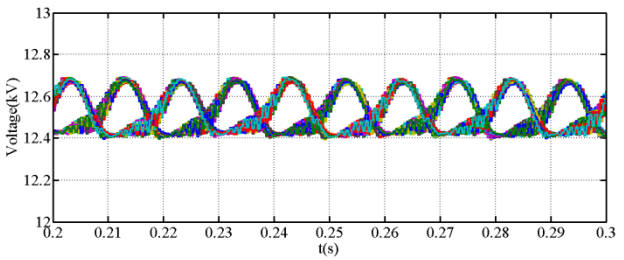
(a) Full-bridge MMC output phase relative to dc link mid-point



(b) Output phase current



(c) Current waveforms in the upper and lower arms of the full-bridge MMC



(d) Cell capacitor voltages of the upper and lower arms

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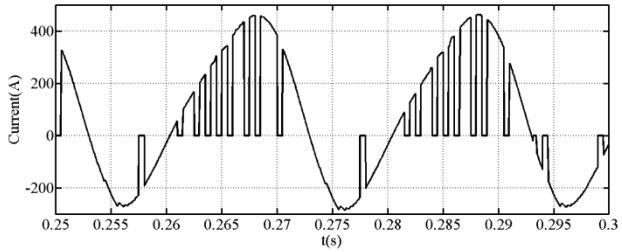
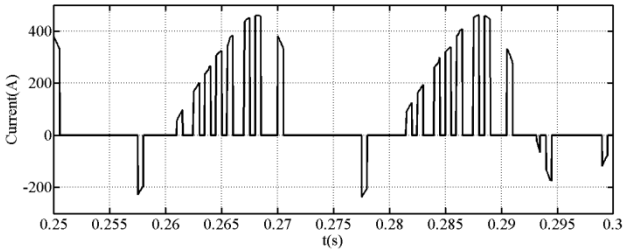
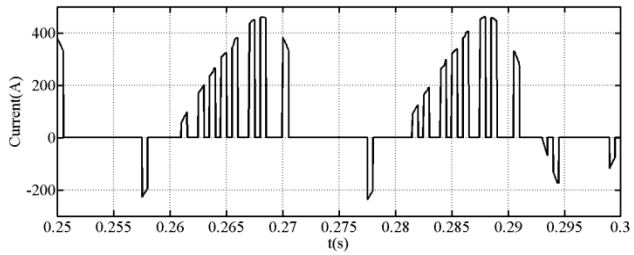


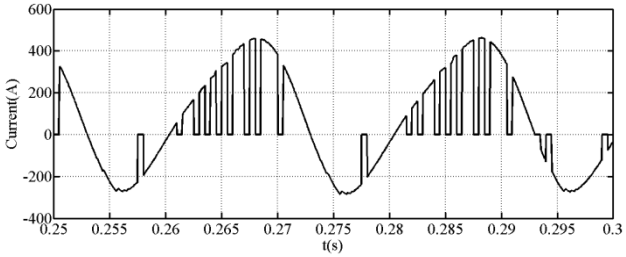
(e) Current in switching device (S_{a11})



(f) Current in switching device (S_{a12})

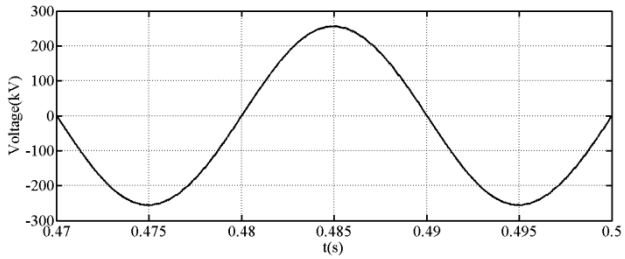


(g) Current in switching device (S_{a13})

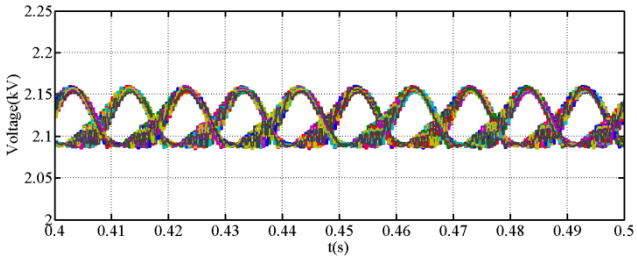


(h) Current in switching device (S_{a14})

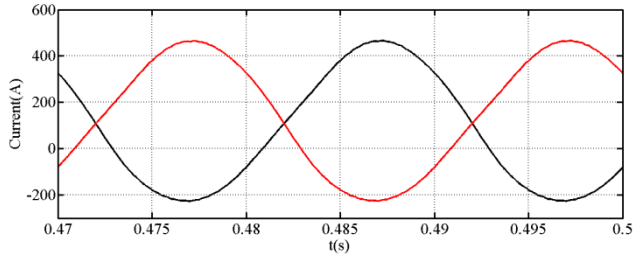
Figure 5: Waveforms obtained from EMT model of the full-bridge MMC discussed in section III-B, with 51 cells per arm when 2nd harmonic suppression of the arm currents controller is incorporated (cell capacitance=5mF, R_d=0.05Ω and L_d=50mH)



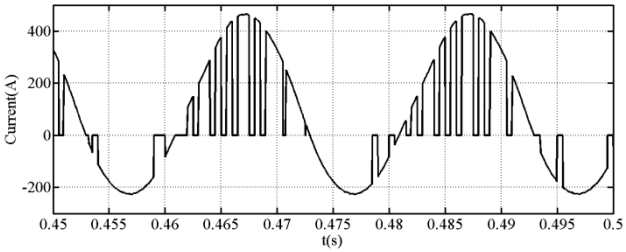
(a) Full-bridge MMC output phase voltage



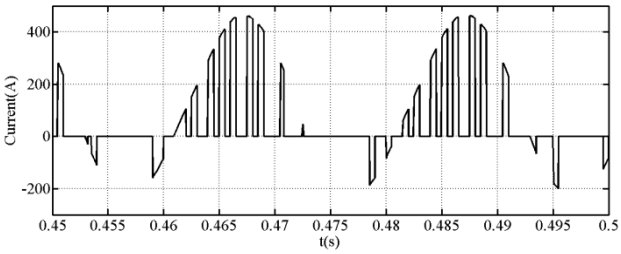
(b) Cell capacitor voltages



(c) Upper and lower arm currents



(d) Sample current waveforms in switching devices S_{a11}



(e) Sample current waveforms in switching devices S_{a13}

Figure 6: Waveforms obtained from EMT model of the full-bridge MMC discussed in section III-B, with 301 cells per arm and 2nd harmonic suppression of the arm currents controller is incorporated (cell capacitance=14mF, R_d=0.05Ω and L_d=50mH)

V. CONTROL SYSTEMS DESIGN

For the purpose of the control design, considers the simplified representation of the grid connected modular multilevel converter in Figure 7, where 'o' represents the ground (dc link mid-point of the symmetrical mono-polar as normally set by the stray capacitance of the dc line). Considering the upper and lower arms of the generic modular converter in Figure 7 when the total voltage developed across the upper and lower arms are replaced by their low-frequency components, the following equations are obtained for phase '*a*':

$$\tfrac{1}{2}V_{dc} - v_{ao} - R_d i_{a1} - L_d \frac{di_{a1}}{dt} - v_{a1} = 0 \tag{10}$$

$$\tfrac{1}{2}V_{dc} + v_{ao} - R_d i_{a2} - L_d \frac{di_{a2}}{dt} - v_{a2} = 0 \tag{11}$$

Converter terminal voltage v_{ao} can be expressed in terms of output current i_a and grid voltage v_{ga} as:

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$$v_{ao} = R_T i_a + L_T \frac{di_a}{dt} + v_{ga} \tag{12}$$

After subtracting (11) from (10) and combine with (12), the following equation is obtained:

$$\begin{aligned} &v_{a2} - v_{a1} - R_d(i_{a1} - i_{a2}) - L_d \frac{d}{dt}(i_{a1} - i_{a2}) \\ &-2R_T i_a - 2L_T \frac{di_a}{dt} - 2v_{ga} = 0 \end{aligned} \tag{13}$$

Recall that $i_a = i_{a1} - i_{a2}$, $v_{a1} = \frac{1}{2}V_c\left[1 - m\sin(\omega t + \delta)\right]$ and $v_{a2} = \frac{1}{2}V_c\left[1 + m\sin(\omega t + \delta)\right]$, where V_c presents the mean dc voltage of the upper and lower arms cell capacitors, m is the modulation index, v_{ga} is the grid voltage, and δ is the angle between converter terminal v_{ao} and grid voltage v_{ga}. With these assumptions, equation (13) can be reduced to:

$$(\tfrac{1}{2}L_d + L_T)\frac{di_a}{dt} + (\tfrac{1}{2}R_d + R_T)i_a = \tfrac{1}{2}mV_c\sin(\omega t + \delta) - v_{ga} \tag{14}$$

From (14), differential equations that describe fundamental currents for all three phases in the modular converter can be deduced as:

$$\begin{aligned} &(\tfrac{1}{2}L_d + L_T)\frac{di_a}{dt} + (\tfrac{1}{2}R_d + R_T)i_a = \tfrac{1}{2}mV_c\sin(\omega t + \delta) - v_{ga} \\ &(\tfrac{1}{2}L_d + L_T)\frac{di_b}{dt} + (\tfrac{1}{2}R_d + R_T)i_b = \tfrac{1}{2}mV_c\sin(\omega t + \delta + \tfrac{4}{3}\pi) - v_{gb} \\ &(\tfrac{1}{2}L_d + L_T)\frac{di_c}{dt} + (\tfrac{1}{2}R_d + R_T)i_c = \tfrac{1}{2}mV_c\sin(\omega t + \delta + \tfrac{2}{3}\pi) - v_{gc} \end{aligned} \tag{15}$$

Assuming, the d-axis is aligned with the phase '*a*' of the grid voltage, equation (15) is transformed into d-q synchronous reference frame as:

$$\begin{aligned} &(\tfrac{1}{2}L_d + L_T)\frac{di_d}{dt} - \omega(\tfrac{1}{2}L_d + L_T)i_q + (\tfrac{1}{2}R_d + R_T)i_d = \tfrac{1}{2}mV_c\sin\delta - v_{gd} \\ &(\tfrac{1}{2}L_d + L_T)\frac{di_q}{dt} + \omega(\tfrac{1}{2}L_d + L_T)i_d + (\tfrac{1}{2}R_d + R_T)i_q = \tfrac{1}{2}mV_c\cos\delta - v_{gq} \end{aligned} \tag{16}$$

For current control design, equation (16) is re-arranged as:

$$\frac{di_d}{dt} = -\frac{(\frac{1}{2}R_d + R_T)}{(\frac{1}{2}L_d + L_T)}i_d + \frac{v_{cd} - v_{gd} + \omega(\frac{1}{2}L_d + L_T)i_q}{(\frac{1}{2}L_d + L_T)} \tag{17}$$

$$\frac{di_q}{dt} = -\frac{(\frac{1}{2}R_d + R_T)}{(\frac{1}{2}L_d + L_T)}i_q + \frac{v_{cq} - v_{gq} - \omega(\frac{1}{2}L_d + L_T)i_d}{(\frac{1}{2}L_d + L_T)} \tag{18}$$

With the following change of variables: $u_d = v_{cd} - v_{gd} + \omega(\frac{1}{2}L_d + L_T)i_q$ and $u_q = v_{cq} - v_{gq} - \omega(\frac{1}{2}L_d + L_T)i_d$, u_d and u_q are obtained by forcing i_d and i_q to follow i_d^* and i_q^* using proportional-integral controller as: $u_d = k_p(i_d^* - i_d) + k_i\int(i_d^* - i_d)dt$ and $u_q = k_p(i_q^* - i_q) + k_i\int(i_q^* - i_q)dt$, where k_p and k_i represent the proportional and integral gains. After manipulations of equations (17) and (18), and definitions given for u_d and u_q, where the integral parts of u_d and u_q are replaced by λ_d and λ_q the following equation is obtained:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ \lambda_d \\ i_q \\ \lambda_q \end{bmatrix} = \begin{bmatrix} -\frac{(\frac{1}{2}R_d + R_T + k_p)}{(\frac{1}{2}L_d + L_T)} & \frac{1}{(\frac{1}{2}L_d + L_T)} & 0 & 0 \\ -k_i & 0 & 0 & 0 \\ 0 & 0 & -\frac{(\frac{1}{2}R_d + R_T + k_p)}{(\frac{1}{2}L_d + L_T)} & \frac{1}{(\frac{1}{2}L_d + L_T)} \\ 0 & 0 & -k_i & 0 \end{bmatrix}\begin{bmatrix} i_d \\ \lambda_d \\ i_q \\ \lambda_q \end{bmatrix} + \begin{bmatrix} \frac{k_p}{(\frac{1}{2}L_d + L_T)} & 0 \\ k_i & 0 \\ 0 & \frac{k_p}{(\frac{1}{2}L_d + L_T)} \\ 0 & k_i \end{bmatrix}\begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix} \tag{19}$$

After Laplace manipulation of (19), the initial gains of the inner current controller can be selected using $k_p = 2\omega_n\zeta(\frac{1}{2}L_d + L_T) - (\frac{1}{2}R_d + R_T)$ and $k_i = \omega_n^2(\frac{1}{2}L_d + L_T)$, and natural frequency ω_n can be selected assuming settling time 'T_s' and damping factor 'ζ' from $\omega_n = \frac{4}{\zeta T_s}$. However, the final gains must be fined tune to ensure that satisfactory performance is achieved over the entire system operating range, including ac and dc network faults. From definitions of the u_d and u_q, where u_d and u_q are the outputs of current controller in the d and q channels, the block diagram for the inner current controller in Figure 8 is obtained.

For design of the supplementary current controller that responsible for suppression of the 2nd harmonic component of the common mode current, add equations (10) and (11), and the following equation is obtained:

$$V_{dc} - (v_{a1} + v_{a2}) - R_d(i_{a1} + i_{a2}) - L_d\frac{d}{dt}(i_{a1} + i_{a2}) = 0 \tag{20}$$

Recall that the common mode current of the upper and lower arms can be defined as $i_{com}=i_{a1}+i_{a2}$, therefore equation (20) can be reduced to:

$$\frac{di_{com}}{dt} = -\frac{R_d}{L_d}i_{com} + \frac{V_{dc} - V_c}{L_d} \tag{21}$$

Since flow of the ac current components of the i_{a1} and i_{a2} in the arm reactors and cell capacitors cause capacitor voltages of the upper and lower arms to oscillate (thus, V_c), the common mode current i_{com} contains dc and ac components. Therefore, equation (21) is written as in (22) and broken into (23) and (24):

$$\frac{di_h}{dt}(I_d + i_h) = -\frac{R_d}{L_d}(I_d + i_h) + \frac{1}{L_d}(V_{c0} + v_h) \tag{22}$$

$$\frac{dI_d}{dt} = -\frac{R_d}{L_d}I_d + \frac{1}{L_d}V_{c0} \tag{23}$$

$$\frac{di_h}{dt} = -\frac{R_d}{L_d}i_h + \frac{1}{L_d}v_h \tag{24}$$

Observe that equation (23) describes dynamics of the arm current dc component I_d, which is responsible for power transfer between converter and dc side. Equation (24) describes dynamics of the ac component of the common mode current i_h, which is dominantly 2nd order harmonic plus other harmonics, depending on the modulation strategy employed; where v_h represents the cell capacitor voltage ripple. In attempt to reduce the semiconductor losses due to 2nd harmonic of the arm current, this paper favours the use of a simple PI controller over the proportional resonance to minimize 2nd harmonics in the MMC arm currents (or i_h). This requires i_h to be passed through a band pass filter (BPF), tuned at 100Hz with high quality factor in order to extract only the 2nd harmonic component i_{2h} from i_h. Considering 2nd harmonic only, equation (24) becomes:

$$\frac{di_{2h}}{dt} = -\frac{R_d}{L_d}i_{2h} + \frac{1}{L_d}v_{2h} \tag{25}$$

The voltage v_{2h} needed to minimize the 2nd harmonic in the MMC arm current is estimated from PI controller as:

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$$v_{2h} = \alpha_p (i_{2h}^* - i_{2h}) + \alpha_i \int (i_{2h}^* - i_{2h}) dt \quad (26)$$

After replacing the integral part in (26) by z_{2h}, and algebraic manipulations of (25) and (26), the following equation is obtained:

$$\frac{d}{dt}\begin{bmatrix} i_{2h} \\ z_{2h} \end{bmatrix} = \begin{bmatrix} -(R_d + \alpha_p)/L_d & 1/L_d \\ -\alpha_i & 0 \end{bmatrix} \begin{bmatrix} i_{2h} \\ z_{2h} \end{bmatrix} + \begin{bmatrix} \alpha_p/L_d \\ \alpha_i \end{bmatrix} i_{2h}^* \quad (27)$$

After Laplace manipulations of (27), the following closed loop transfer function for the 2nd harmonic suppression is obtained:

$$\frac{i_{2h}(s)}{i_{2h}^*(s)} = \frac{\alpha_p/L_d\, s + \alpha_i/L_d}{s^2 + (\alpha_p + R_d)/L_d\, s + \alpha_i/L_d} \quad (28)$$

From (28), the PI gains are : $\alpha_p = 2\zeta\omega_n L_d - R_d$ and $\alpha_i = \omega_n^2 L_d$, where ζ and ω_n are damping factor and controller natural frequency in rad/s. To accommodate BPF dynamics and avoid interference with the main power flow controllers, the gains for the 2nd harmonic suppression controller must be selected to be as slow as possible, and its output is limited to 5% of modulation index. This indicates that inclusion of such supplementary controller reduces converter dc link utilization and P-Q envelope if compared to the approach that uses passive filter for arm current 2nd harmonic suppression as demonstrated in.[53, 62, 63]. Figure 8 summarises the overall control system that has been used in the MMC_1 and MMC_2, which includes all expected HVDC basic controllers and supplementary controller for suppression of the arm currents 2nd harmonic component.

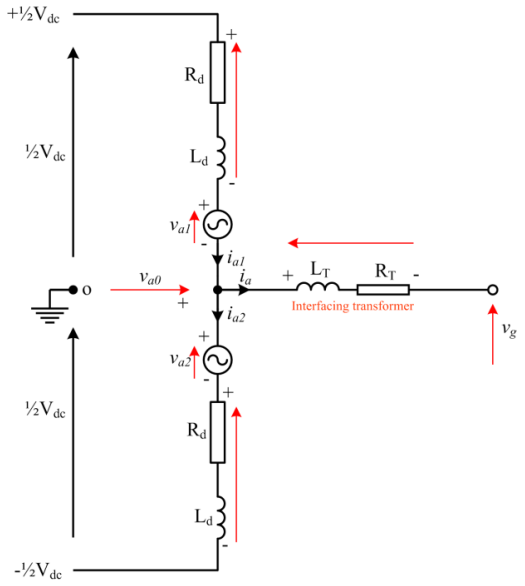

Figure 7: Simplified illustration of generic modular multilevel converter connected to grid

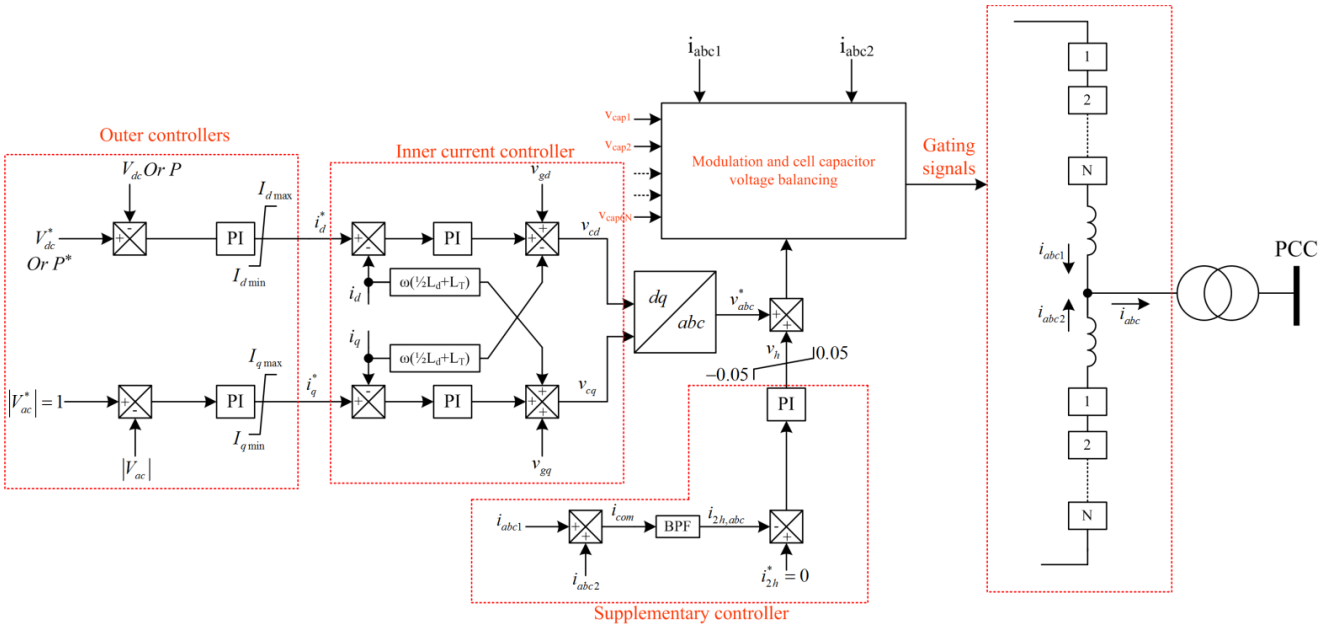

Figure 8: Block diagram illustrates generic control systems used in both converter stations MMC_1 and MMC_2

VI. SIMULATION OF FULL-SCALE HVDC LINK

To demonstrate the effectiveness of the electromagnetic transient (EMT) modelling approach discussed in section III when used to simulate full-scale VSC-HVDC links, an example link in Figure 9 is built in Simulink environment with converter stations MMC_1 and MMC_2 modelled with 201 half-bridge cells per arm, with parameters listed in Table 2. MMC_1 is configured to regulate active power exchange between AC systems 1 and 2, and provides voltage support at PCC_1. MMC_2 regulates dc link voltage level at 400kV (pole-to-pole), and supports ac voltage at PCC_2. Both MMC_1 and MMC_2 employ staircase modulation, with sinusoidal references. Small time step of 5μs is used throughout this section to show the computational efficiency of the presented MMC when simulating HVDC links with large number of cells per converter (1206 cells per converter, and 2412 cells per model).

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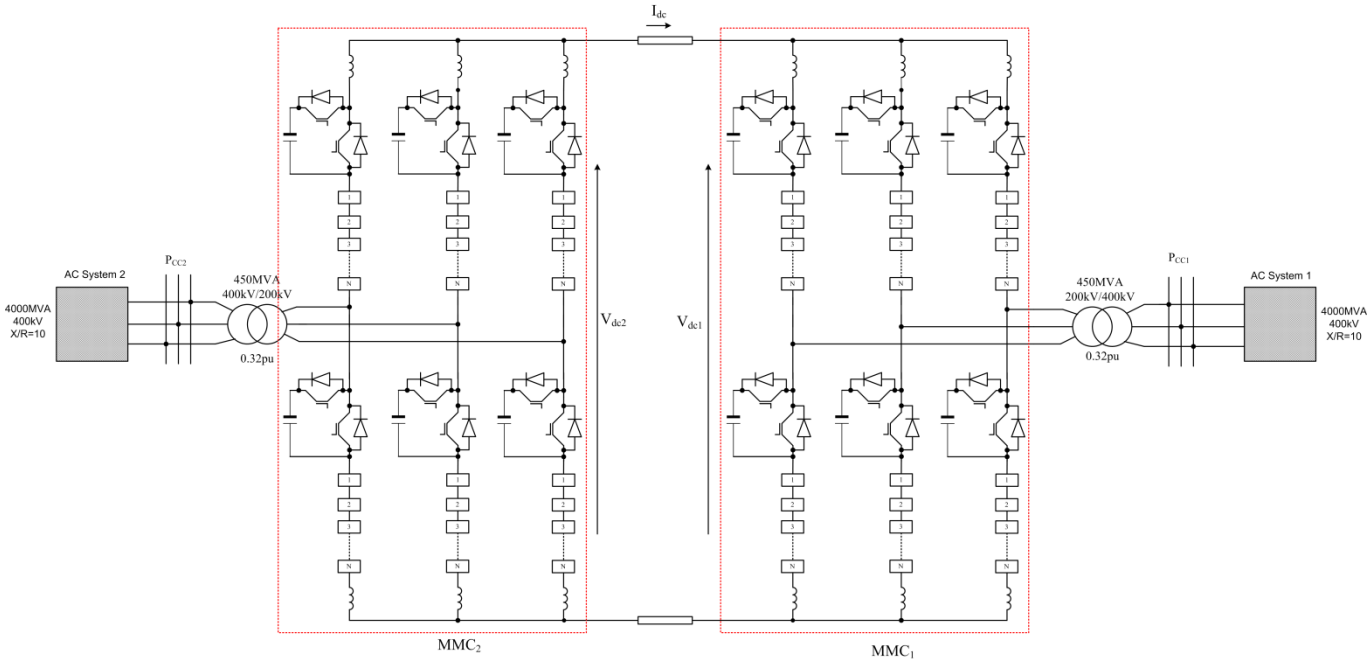


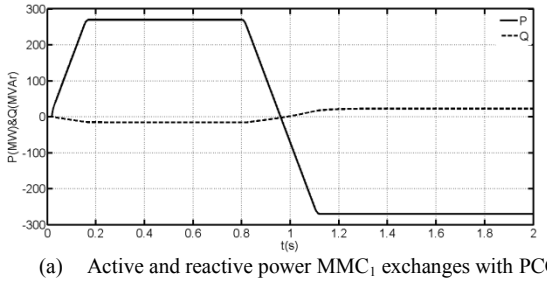
Figure 9: Simulink model of full-scale VSC-HVDC

Table 2: Parameters of the full-scale MMC based HVDC link in Figure 9

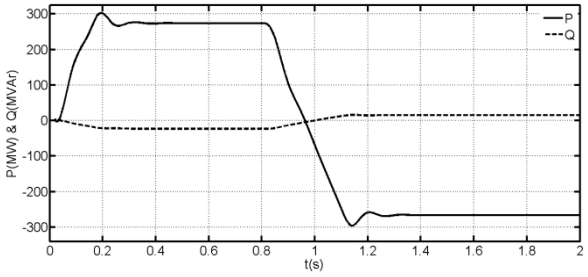
Converters MMC1 and MMC2		interfacing transformer	200kV/400kV
DC link voltage	±200kV	Interfacing transformer leakage reactance	0.32pu
Rated apparent power	450MVA	Resistance of the interfacing transformer	0.00015pu
Maximum active power capability	400MW	AC systems 1 and 2	4000MVA, 400kV and X/R=10
Maximum reactive power capability	±206MVAr	DC line resistance (R_{dc})	10mΩ/km
Inductance of the arm reactor (L_d)	31mH	DC line capacitance (C_{dc})	0.15μF/km
Resistance of the arm reactor (R_d)	0.015Ω	DC line inductance (L_{dc})	0.6mH/km
Cell capacitance (Cm)	6mF	DC line length	100km
Number of cells per arm	201		

A) Normal Operation

This section presents simulation results obtained when converter station MMC_1 of the full-scale HVDC link in Figure 9 ramps its output power from 0 to 0.7pu (315MW) in order to export power from *ac* system 2 to 1. At time t=0.8s, MMC_1 reverses the power flow by gradually ramping down its output power from 0.7pu to -0.7pu. Observe that the selected waveforms in Figure 10 reproduce the typical behaviour of the MMC based HVDC link in great detail than similar works presented in [28, 30, 31]. Figure 10(a) and (b) show active and reactive power at ac sides of the MMC_1 and MMC_2. Figure 10(c) and (d), and (e) and (f) show ac current waveforms MMC_1 and MMC_2 inject into PCC_1 and PCC_2, and their arm currents. Notice that the shape of the arm currents in Figure 10 (e) and (f) are typical to the SIEMENS HVDC PLUS presented in [64] as the power flow direction changes. Figure 10 (g) and (h) show dc link current, and converter line-to-line terminal voltage. Figure 10 (h) shows that with such large number of cells, MMC presents pure sinusoidal voltage to the interfacing transformer. Figure 10(i) and (j) show the dc link voltage of the MMC_1 and MMC_2. Figure 10 (k) and (l) display cell capacitor voltages of both converter stations, and observe that they are balanced and settled around 1.99kV as expected. Figure 10(m) shows zoomed version of the cell capacitor voltage of the MMC_1, phase '*a*'. Figure 10 (n) and (o) present sample of the current waveforms in the switching devices of one cell (top cell in the phase '*a*' upper arm). The results in Figure 10 have shown that the presented modelling approach is able to reproduce the typical behaviour of full-scale MMC based HVDC link in great detail, including access to all internal variables of the modular converters which are of great importance from system design prospective.



(a) Active and reactive power MMC_1 exchanges with PCC_1



(b) Active and reactive power MMC_2 exchanges with PCC_2

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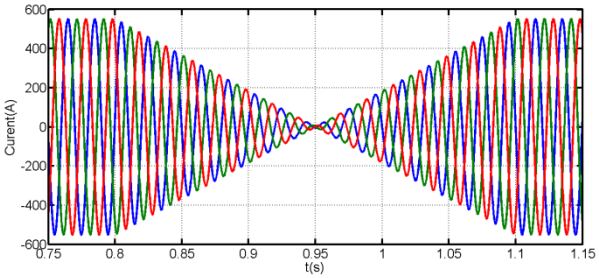
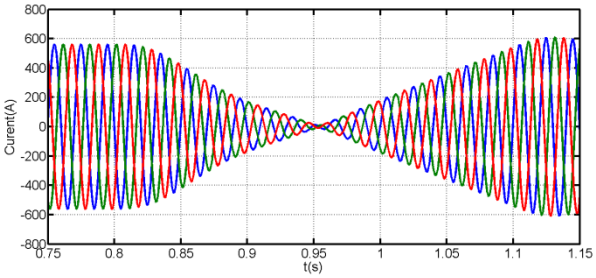
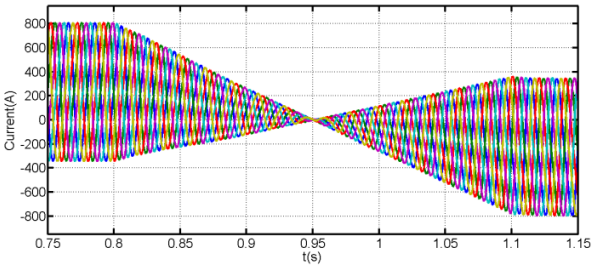


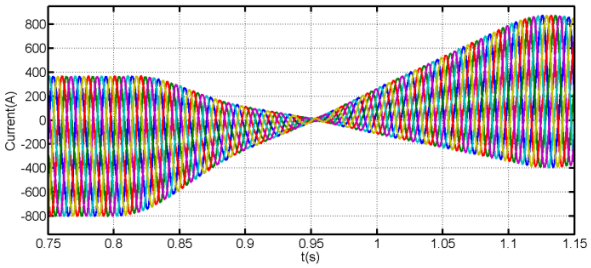
(c) Current waveforms MMC_1 injects into PCC_1



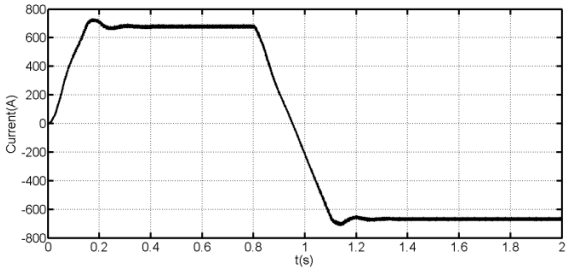
(d) Current waveforms MMC_2 injects into PCC_2



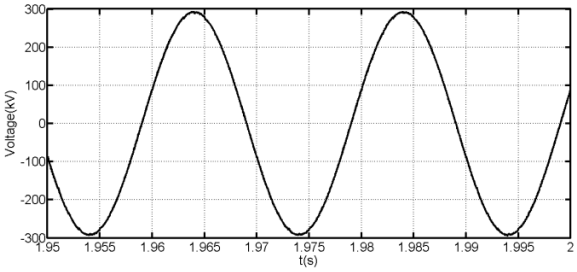
(e) MMC_1 six arm currents zoomed around power reversal



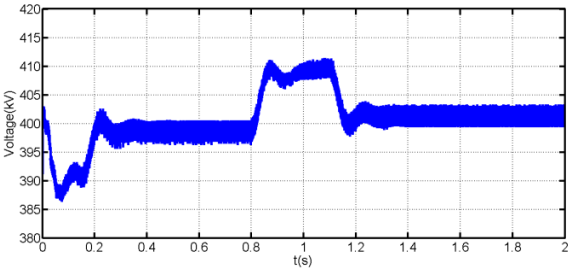
(f) MMC_2 six arm currents zoomed around power reversal



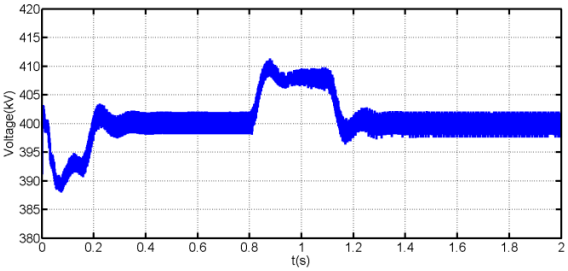
(g) DC link current



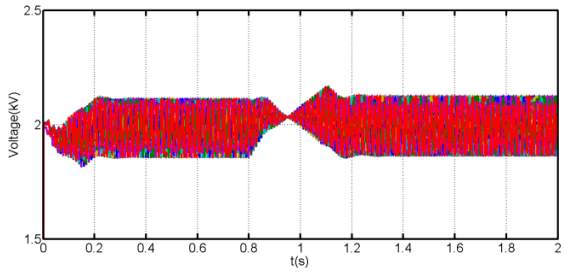
(h) Sample of the line-to-line voltage MMC_1 presents to its interfacing transformer (measured at converter terminal before interfacing transformer)



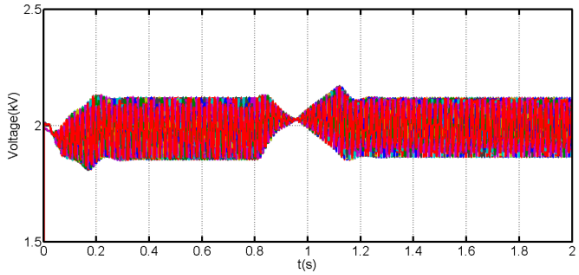
(i) VSC_1 DC link voltage



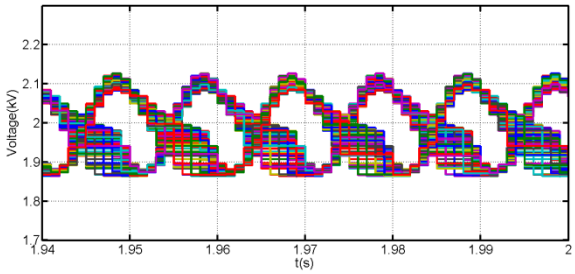
(j) VSC_2 DC link voltage



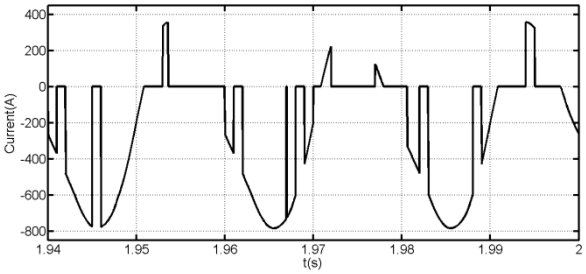
(k) Voltage across 402 cell capacitors of the MMC_1 (phase A)



(l) Voltage across 402 cell capacitors of the MMC_2 (phase A)



(m) Zoomed version of the 402 cell capacitors of the MMC_1 (phase A)



(n) Current in the swicthing device S_{a1} (MMC_1)

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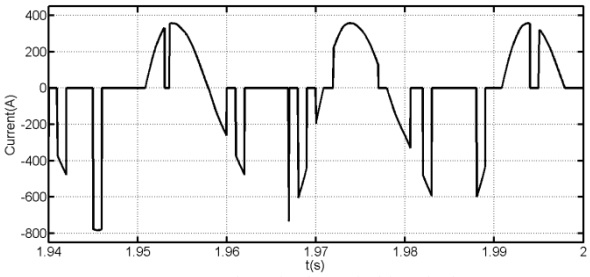
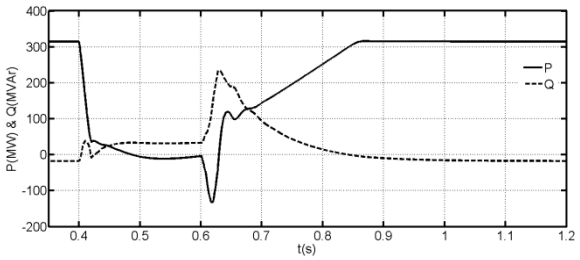


(o) Current waveform in the swicthing device S_{x1} (MMC_1)

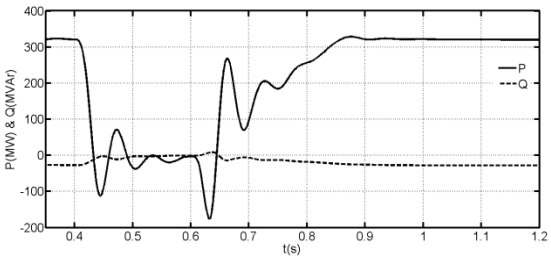
Figure 10: Selected waveforms that demonstrate the suitability of the EMT approach discussed in section III for full-scale modelling of the MMC based VSC-HVDC link

B) AC fault

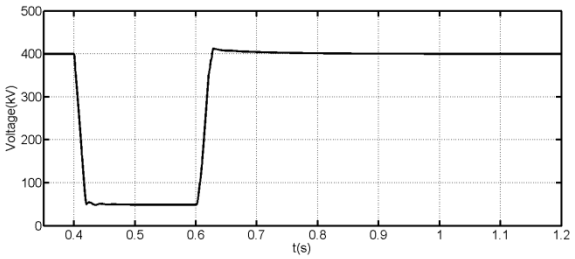
To examine the suitability of the presented MMC modelling approach for studying ac network faults, the full-scale Simulink model of the HVDC link in Figure 9 is subjected to a three-phase ac fault at PCC_1, through 2Ω fault resistance at time t=0.4s and cleared after 200ms. After ac fault is detected, MMC_1 active output is reduced immediately to 0 and restored when the fault is cleared. Figure 11 displays selected waveforms obtained from the full-scale Simulink model when it is subjected to a three-phase fault at PCC_1. Figure 11 (a) and (b) show active and reactive powers MMC_1 and MMC_2 exchange with their point of common couplings PCC_1 and PCC_2. Observe that although the active power of the MMC_1 is reduced to zero immediately when ac fault is detected, the active power at the ac side of the MMC_2 that regulates dc link voltage takes longer time to fall to zero. This is because the dynamics of the dc power (or dc component of the arm currents) is strongly link to the change in the cell voltages, which take several fundamental cycles to adjust following power order at MMC_1. The results in Figure 11 (a) and (b) indicate that the MMC based HVDC link has relative slow dynamic response when compared with conventional VSC-HVDC links that use two-level or neutral-point clamped converters. Figure 11 (c) and (d) show the voltage magnitude and ac current waveforms at PCC_1, and notice that although the voltage at PCC_1 collapses to less than 30% of the rated voltage, the current contribution of the MMC_1 to the ac fault is limited and less than the pre-fault currents. The dc link voltages of the MMC_1 and MMC_2 in Figure 11 (e) and (f) exhibit slight increase during brief period of ac and dc powers mismatch as a result of ac fault and sudden reduction in MMC_1 power order; thanks to the large energy storage capacity of 1206 cell capacitors per converter. Figure 11 (g) and (h) show the cell capacitor voltages of the MMC_1 and MMC_2 experience some disturbances during ac fault, with the cell capacitor voltages of the MMC_1 (near to the fault) experience larger voltage ripples than that of the MMC_2 (remote converter). These results have demonstrated the ability of the presented model to capture the behaviour of typical MMC based HVDC link, including internal converter station dynamics and interactions between ac and dc sides. Therefore, it can be concluded that the presented model is qualified to be used for ac network faults studies, and other detailed systems studies at design stage, including design of the link and converter protection systems.



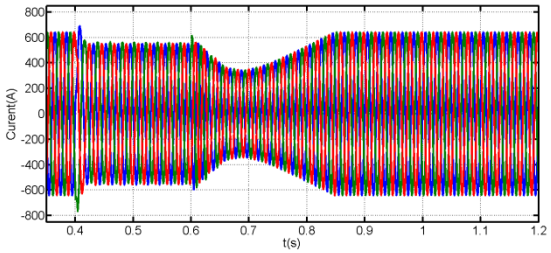
(a) Active and reactive MMC_1 exchanges with PCC_1



(b) Active and reactive MMC_2 exchanges with PCC_2



(c) Voltage magnitude at PCC_1



(d) Current waveforms MMC_1 injects into PCC_1

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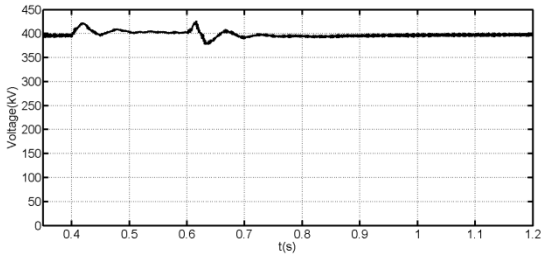
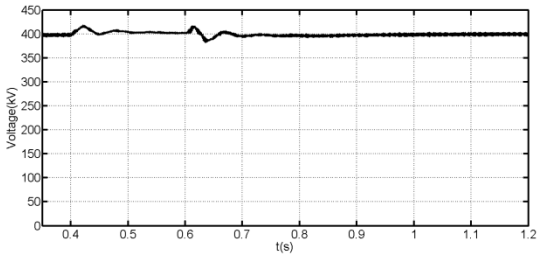
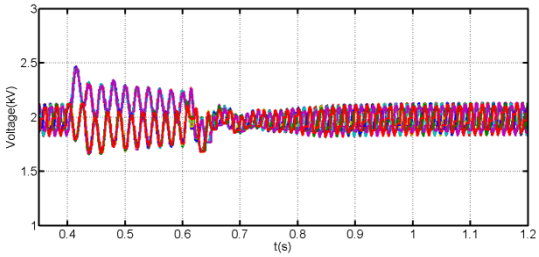


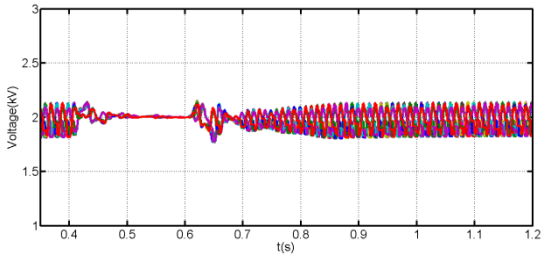
(e) MMC_1 DC link voltage (V_{dc1})



(f) MMC_2 DC link voltage (V_{dc2})



(g) Voltage across cell capacitors of phase 'A' in the MMC_1

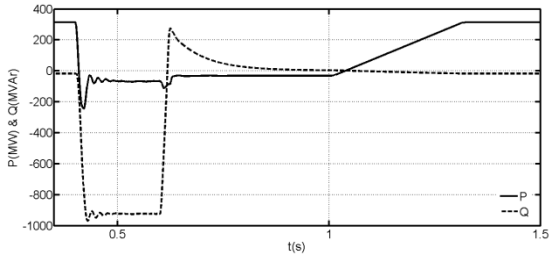


(h) Voltage across cell capacitors of phase 'A' in the MMC_2

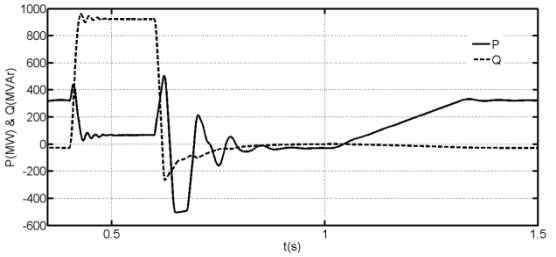
Figure 11: Waveforms obtained from full-scale Simulink model in Figure 9 when it has been subjected to three-phase ac fault at PCC_1, with 200ms fault duration

C) DC fault

To assess the suitability of the presented full-scale MMC based HVDC link for dc faults studies, the Simulink model of HVDC link in Figure 9 is subjected to a solid pole-to-pole dc short circuit fault at the middle of the dc line between MMC_1 and MMC_2 at t=0.4s, with 200ms fault duration. When dc fault is detected, converter switches are blocked immediately. In pre-fault condition, the link exports 315MW (0.7pu) from ac system 2 to 1. When dc fault is detected at t=0.4s, power command to MMC_1 is reduced immediately to zero and its restoration to pre-fault value is delayed until t=1s to allow all transients associated with the fault and converter de-blocking at t=0.6s to die out. Figure 12 (a) and (b) show the HVDC link being studied is able to recover with increased reactive power consumptions due to current in-feed through anti-parallel diodes of MMC_1 and MMC_2 as expected in typical half-bridge MMC based HVDC link. Current waveforms in Figure 12 (c) and (d) show large current in-feeds at ac sides of the MMC_1 and MMC_2 during fault period as previously mentioned. Figure 12 (e) and (f) display dc currents at the terminals of the MMC_1 and MMC_2. Observe that due to the concept of distributed cell capacitors of the MMC the transient component of the dc fault that associated with discharge of dc line distributed capacitors is much smaller than the steady, which is mainly due to grid contribution through converter anti-parallel diodes. Figure 12 (g) shows the collapse of the MMC_1 DC link voltage during pole-to-pole DC fault at the middle of the HVDC link (as a sample). Figure 12 (h) and (i) display current waveforms in six arms of the MMC_1 and MMC_2, and observe that the arm currents of both converters tend to be negative, and this confirms that the in-feed currents from the ac to dc sides during dc fault are flowing through anti-parallel diodes as expected in typical MMC link. Figure 12 (j) and (k) show the current waveforms in the switching devices S_{a1} and S_{x1} (top cell in the phase '*a*', upper arm of the MMC_1), and observe that there is no current in the switching device S_{x1} which is in series with the cell capacitor as anticipated in typical MMC link during dc fault when converter switches are blocked. Whilst the current in the main switch S_{a1} is naturally commutated as in typical diode rectifier, but with large overlap which is caused by present of large inductances in the conduction path (converter transformer leakage inductances plus arm reactors) when converter switching devices are gated off. Figure 12 (l) and (m) present the cell capacitor voltages of the MMC_1 and MMC_2, and observe that the cell capacitor voltages of the MMC_1 and MMC_2 become flat when they are blocked as no currents are following through the cell capacitors as previously shown in Figure 12 (k). Results presented in Figure 12 have shown that the full-scale model of the MMC based HVDC link being simulated using converter model discussed in III-A) is able to reproduce the typical behaviour of the HVDC links that employ half-bridge modular multilevel converters.



(a) Active and reactive power MMC_1 exchanges with PCC_1



(b) Active and reactive power MMC_2 exchanges with PCC_2

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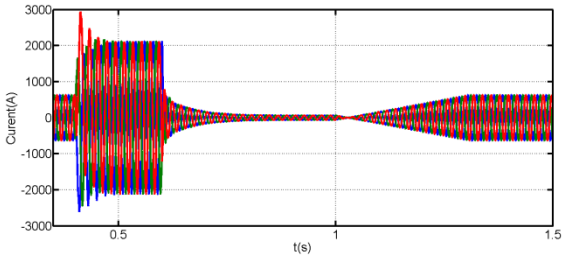
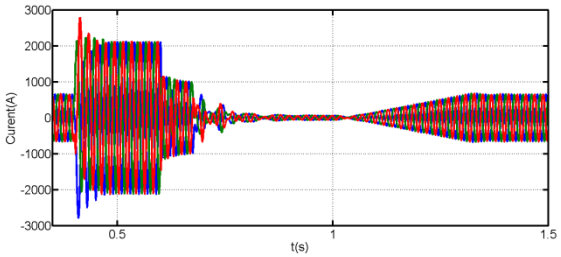
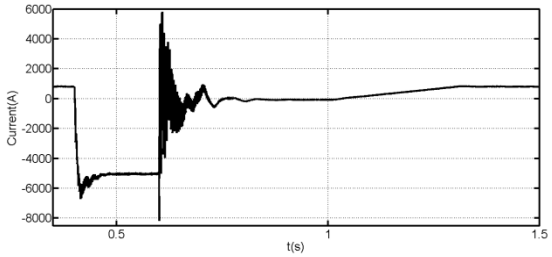


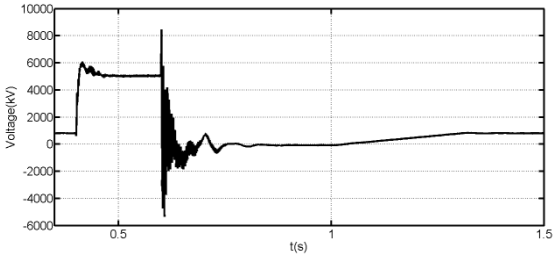
(c) Current waveforms MMC_1 injects into PCC_1



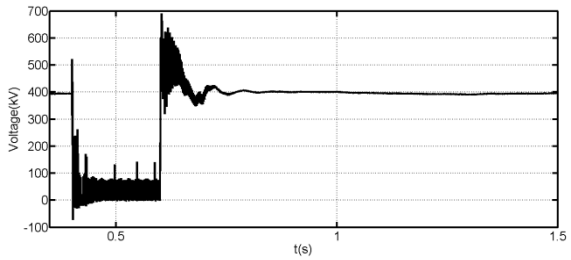
(d) Current waveforms MMC_2 injects into PCC_2



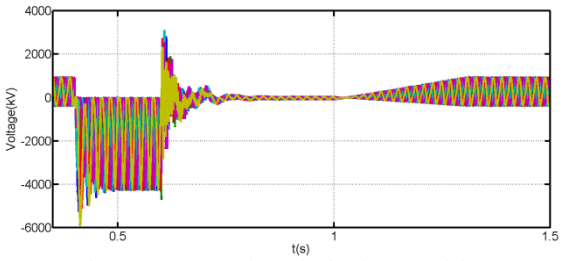
(e) MMC_1 dc link current



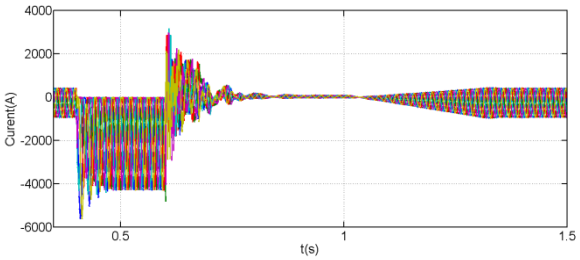
(f) MMC_2 dc link current



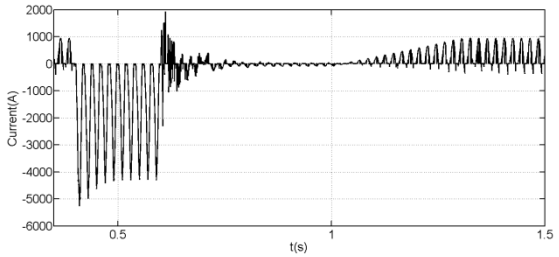
(g) Sample of the dc link voltage measured at the terminal of MMC_1 (V_{dc1})



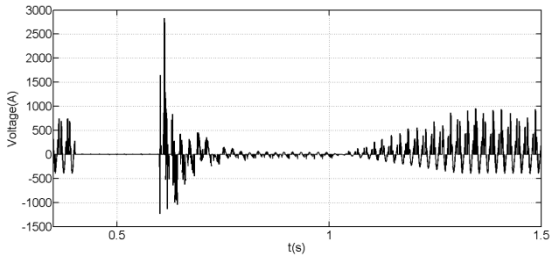
(h) Current waveforms in the six arms of the MMC_1



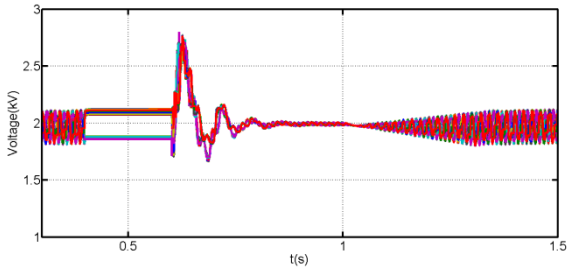
(i) Current waveforms in the six arms of the MMC_2



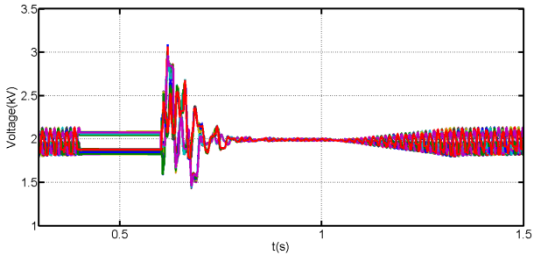
(j) Sample of the current waveform in the switching device S_{a1} (1^{st} cell in upper arm of MMC_1, phase 'a')



(k) Sample of the current waveform in the switching device S_{x1} (1^{st} cell in upper arm of MMC_1, phase 'a')



(l) Voltage across cell capacitor 402 cell capacitors of phase A of the MMC_1



(m) Voltage across cell capacitor 402 cell capacitors of phase A of the MMC_2

Figure 12: Waveforms obtained when a full-scale Simulink model of the MMC based HVDC link in Figure 9 is subjected to a pole-to-pole dc short circuit fault

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VII. CONCLUSIONS

This paper presented improved electromagnetic transient models for the half and full MMC that can be used to simulate normal and transient responses of the full-scale HVDC links that employ modular multilevel converters, hundreds cells per arm. Additionally, it provides comprehensive qualitative and quantities discussions of the half and full-bridge MMCs that cover device and system aspects, which are of great importance for correct modelling of the MMC based HVDC links. It has been shown that the presented models can reproduce the typical behaviour of the half and full bridge MMCs as that normally obtained from the switching model. Scalabilities of both MMC models presented in this paper have demonstrated the suitability of this approach for modelling of full-scale HVDC links and multi-terminal dc grids. Unlike the previous works which are platform dependent, this paper has shown that the presented generic MMC model can be implemented in any platform.

VIII. APPENDIX

This appendix presents validations of the EMTP model discussed in section III-A against its switching counterpart during ac and dc faults, considering the test system in Figure 13. Figure 13 represents one terminal of the HVDC link which is configured to regulate active power and ac voltage at PCC_1. Both models are simulated with reduced number of cells per arm (21 cells per arm), with the same control systems as depicted in Figure 8.

Figure 14 displays selected waveforms obtained when the test system in Figure 13 is subjected to a temporary three-phase fault at PCC_1, at t=0.4s and cleared after 200ms. Figure 14 (a) shows that the three-phase currents both MMC models inject into ac grid during steady state and ac fault are closely matched. Figure 14(b) presents the error between the three-phase currents of the two models shown Figure 14(a), calculated as $\Delta i_{abc} = i_{abc}^{swicth} - i_{abc}^{EMTP}$. Observe that the peak percentage errors during steady-state and ac fault are 2A/644A×100%=0.3% and 7A/551A×100%=1.27% when converter output active power is reduced to zero. Figure 14(c) and (d) show sample of the upper and lower arm currents (phase 'A') obtained from both models and their corresponding error. Observe that the results of the EMTP model agree to that of switch model to the finest details, with some limited errors during fast transient initiated by the ac fault as depicted in Figure 14 (d). Additionally, notice that as the error in Figure 14 (d) fluctuates between positive and negative, which indicates oscillations of the EMTP currents around that of the switching model. Figure 14 (d) indicates that the average error between the two models is expected to be sufficiently small. Figure 14 (e) and (f) show the common mode current $I_{a1}+I_{a2}$ obtained from both models and their corresponding error, and notice that both models agree to great details during steady state and ac fault, with small average error. Figure 14 (g) and (h) display sample of the cell capacitor voltages and their zoomed version around the fault period. Observe that the EMTP model is able to reproduce similar results as that of the switching model, with sufficiently small error. Based on the results in Figure 14 it can be concluded that the presented EMTP model is able to reproduce the output of its switching counterpart, with high level of accuracy. Therefore, it qualifies for any kind of detailed studies of the ac network faults.

To further validate the dc fault performance of the presented EMTP model against its switching equivalent, the test system in Figure 13 is subjected to temporary solid pole-to-pole dc short circuit at the middle of the dc link at t=0.4, with 200ms fault duration, and results obtained are displayed in Figure 15. During dc fault period, the gating signals to converter switches are blocked, and active power command is reduced immediately to zero. Figure 15 (a) shows the snapshot of the three-phase currents converter injects into PCC_1, zoomed around the fault period. Observe that both models produce almost identical results, with small relative error of less than 4% ($\frac{I_{abc}^{switch} - I_{abc}^{EMTP}}{I_{arm}^{switch}} \times 100\% = \frac{2600A - 2700A}{2600A} \approx -3.85\%$) during dc fault. Such level of error is conceivable as the switch model uses relative complex model for the switching devices (IGBT and anti-parallel diode), while EMTP approach uses only two-state resistance to mimic on and off states of the switching devices. Figure 15(b) displays the snapshot of the upper and lower arm currents for phase 'A'. Observe that the presented EMTP model is able to reproduce the output of the switching model, with small relative error of less than 4% ($\frac{I_{arm}^{switch} - I_{arm}^{EMTP}}{I_{arm}^{switch}} \times 100\% = \frac{5300A - 5500A}{5300A} \approx -3.77\%$ 200A) during dc fault when converter switches are gated-off. This confirms the validity of the modifications introduced in the setting of the MMC two-state resistors when gating signals are inhibited as previously discussed in section III-A. Figure 15(c) displays the zoomed version of the cell capacitors (first three cell capacitor voltages from the upper and lower arms of the phase 'A'). Notice that the cell capacitor voltages obtained from the EMTP model are similar to that of the switching model, with some small error of less than 1% during dc fault period.

Simulation waveforms presented in Figure 14 and Figure 15 have shown that the presented EMTP model is sufficiently accurate to be used for wide range of the detailed studies of full-scale HVDC links and multi-terminal HVDC networks, including ac and dc faults.

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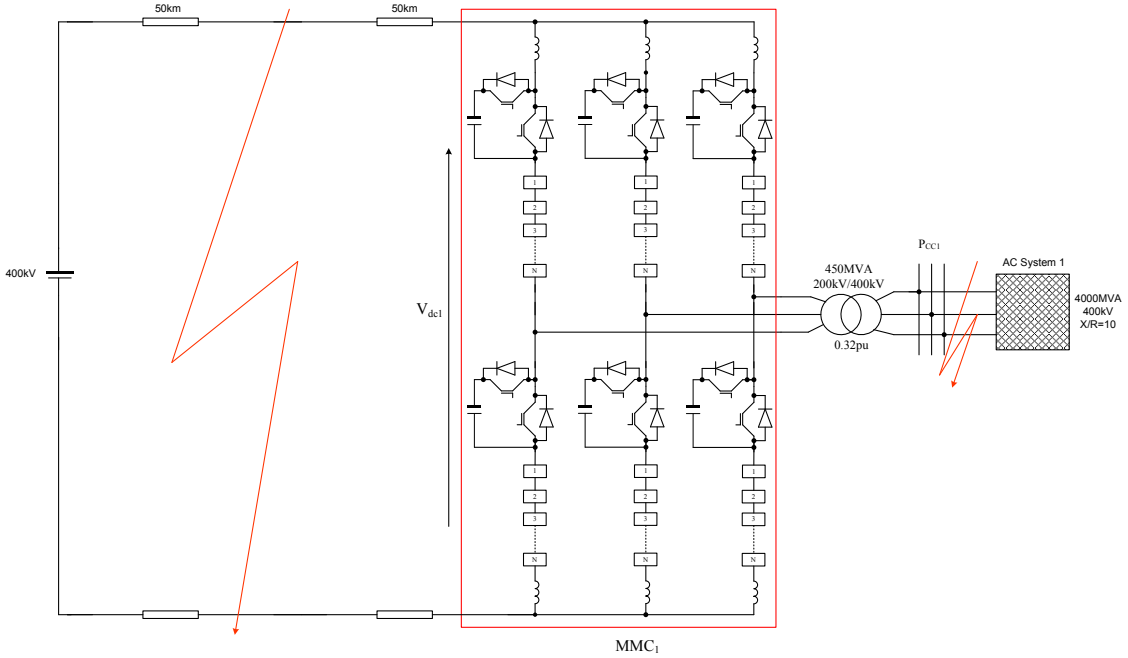
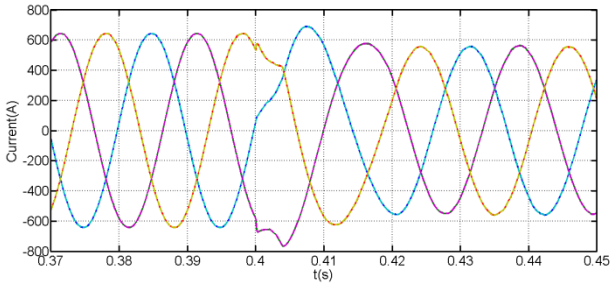
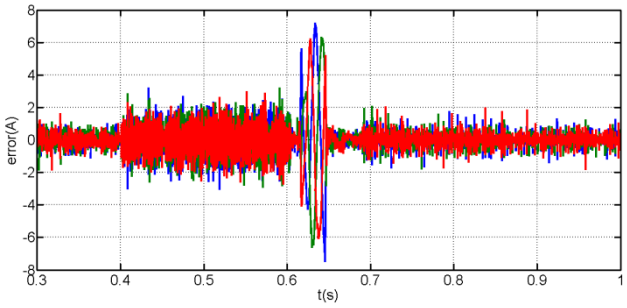


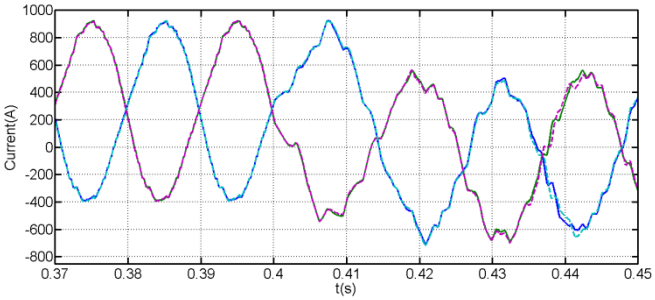
Figure 13: One terminal of the MMC HVDC link used to validate the present EMTP against its switching counterpart, with number of cells per arm is reduced to 21 and cell capacitance 1.4mF



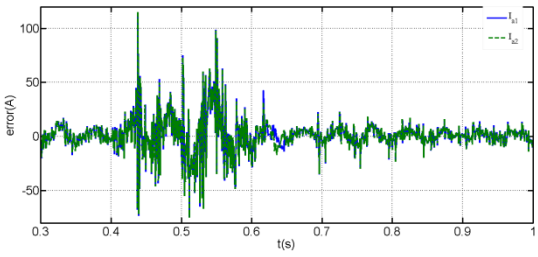
(a) Snapshot of the three-phase currents converter injects into grid zero around the time where the fault is initiated (switch model superimposed on that obtained from EMT model)



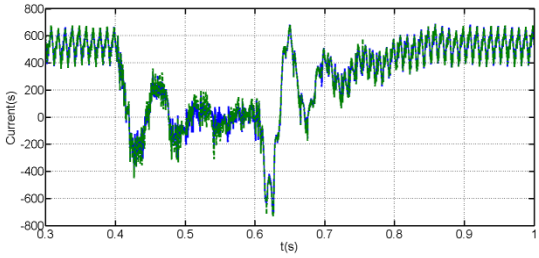
(b) Errors between the two models in the currents converter station injects into ac grid



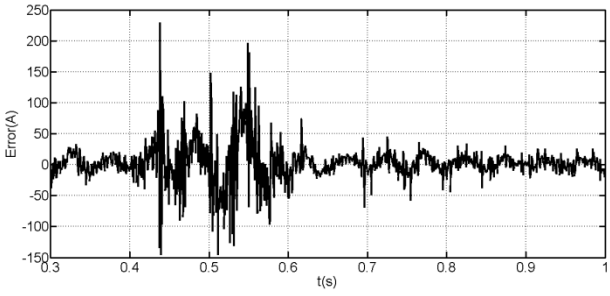
(c) Snapshot of the upper and lower arm currents zoomed around the instant where the ac fault is initiated (phase 'A', switch model superimposed on that obtained from EMT model)



(d) Errors in the arm currents between the two models



(e) Common mode currents $I_{a1}+I_{a2}$ (phase 'A', switch model superimposed on that obtained from EMT model)



(f) Error in common mode current

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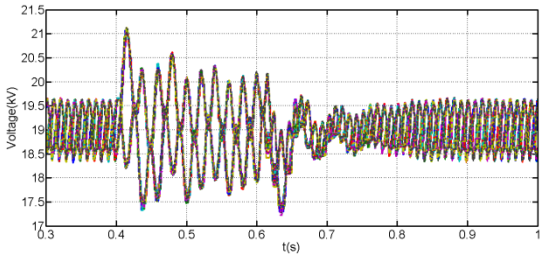
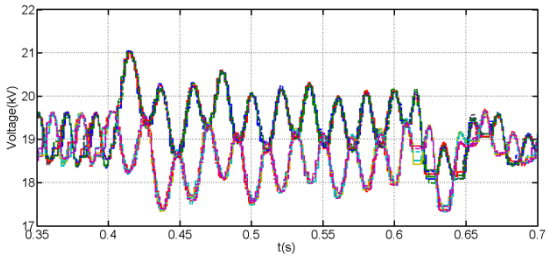
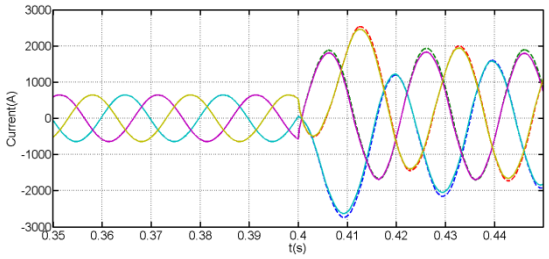


(g) Sample of cell capacitor voltages (phase 'A' upper and lower arms, switch model superimposed on that obtained from EMT model)

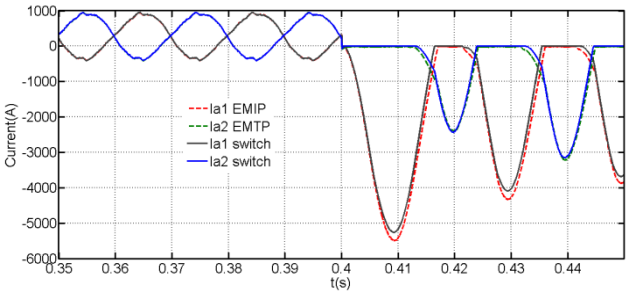


(h) Detailed view of the cell capacitor voltages zoomed around the instant where the fault is initiated (three first cells from the upper and lower arms of phase 'A', switch model superimposed on that obtained from EMT model)

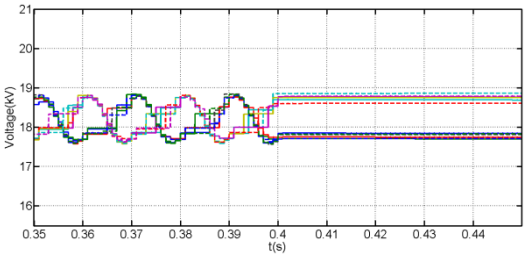
Figure 14: Waveforms aim to validate the presented EMTP model versus its switching equivalent during three-phase ac fault at PCC_1(21 cells per arm, 450MVA converter with 400kV dc link voltage)



(a) Snapshot of the three-phase currents measured at the converter transformer high-voltage side (400kV, grid side), zoomed around instant when dc fault is initiated



(b) Phase 'A' upper and lower arm currents (switch model superimposed on that obtained from EMT model), zoomed around instant when dc fault is initiated



(c) Detailed view of the cell capacitor voltages zoomed around the instant where the fault is initiated (three first cells from the upper and lower arms of phase 'A', switch model superimposed on that obtained from EMT model)

Figure 15: Waveforms aim to validate the presented EMTP model versus its switching equivalent during solid pole-to-pole dc short circuit fault at F_2(21 cells per arm, 450MVA converter with 400kV dc link voltage, dc cable)

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